M66271FP

OPERATION PANEL CONTROLLER

DESCRIPTION

The M66271FP is a graphic display-only controller for displaying a high duty dot matrix type LCD which is used widely for PPC,FAX and multi-function telephones.
It is capable of controlling a monochrome STN LCD system of up to 320 x 240 dots.
The IC has a built-in 9600-byte VRAM as a display data memory.
All of the VRAM addresses are externally opened. Address mapping in the MPU memory space allows direct addressing of all display data from the MPU,thus providing efficient display data processing such as drawing.
The built-in arbiter circuit (cycle steal system) which gives priority to display access allows timing-free access from MPU to VRAM, preventing display screen distortion.
The IC provides interface with a 8-bit/16-bit MPU with a READY($\overline{\text{WAIT}}$) pin.
And this IC has a function for LCD module built-in system by lessening connect pins between MPU.

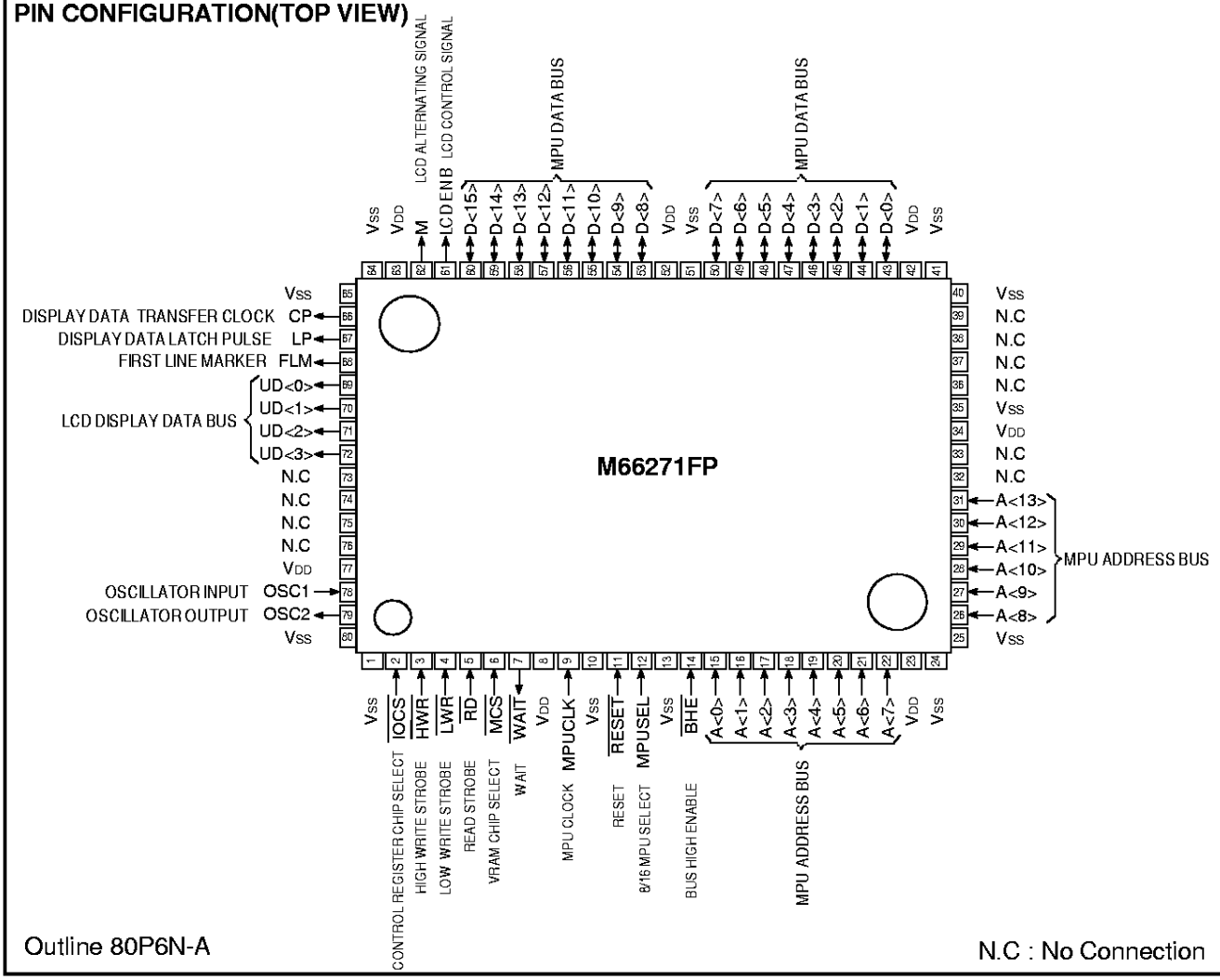
FEATURES

- Displayable LCD
  - •Monochrome STN dot matrix type LCD of up to 76800 dots (equivalent to 320 × 240 dots)
  - •Maximum display duty : 1/240 (set to 240 Line)
    : 1/255 (Max)
- Display memory
  - •Built-in 9600-byte(76800-bit)VRAM (equivalent to one screen of 320 × 240 dots LCD)
  - •All addresses of built-in VRAM are externally opened.
- Interface with MPU
  - •Capability of switching 8-bit type MPU/16-bit type MPU
  - •With $\overline{\text{WAIT}}$ output pin (Accessing register from MPU without $\overline{\text{WAIT}}$ output. Accessing VRAM from MPU with $\overline{\text{WAIT}}$ output.)
  - •Capability of controlling $\overline{\text{BHE}}$ or $\overline{\text{LWR}}$/ $\overline{\text{HWR}}$ at the interface with a 16-bit MPU.
- Interface with LCD
  - •LCD display data are 4-bit parallel output
  - •4 kinds of control signals: CP,LP,FLM and M
- Display functions
  - •Graphic display only (characters drawn graphically)
  - •Binary display only (without tone display function)
  - •Vertical scrolling is allowed within memory range (small size LCD only)
- Additional function for LCD module built-in system
  - •15 kinds of interface with MPU : A<4:1>,D<7:0>,$\overline{\text{IOCS}}$,$\overline{\text{LWR}}$,$\overline{\text{RD}}$
  - •Accessing VRAM from MPU through I/O register
  - •Capability of interfacing with 8-bit type MPU only
- 5V single power supply
- 80-pin QFP

APPLICATION

- •PPC/FAX operation panel,display/operation panel of other OA equipment
- •Multi-function/public telephones
- •PDA/electronic notebook/information terminal
- •Other applications using LCD of 76800 dots or less

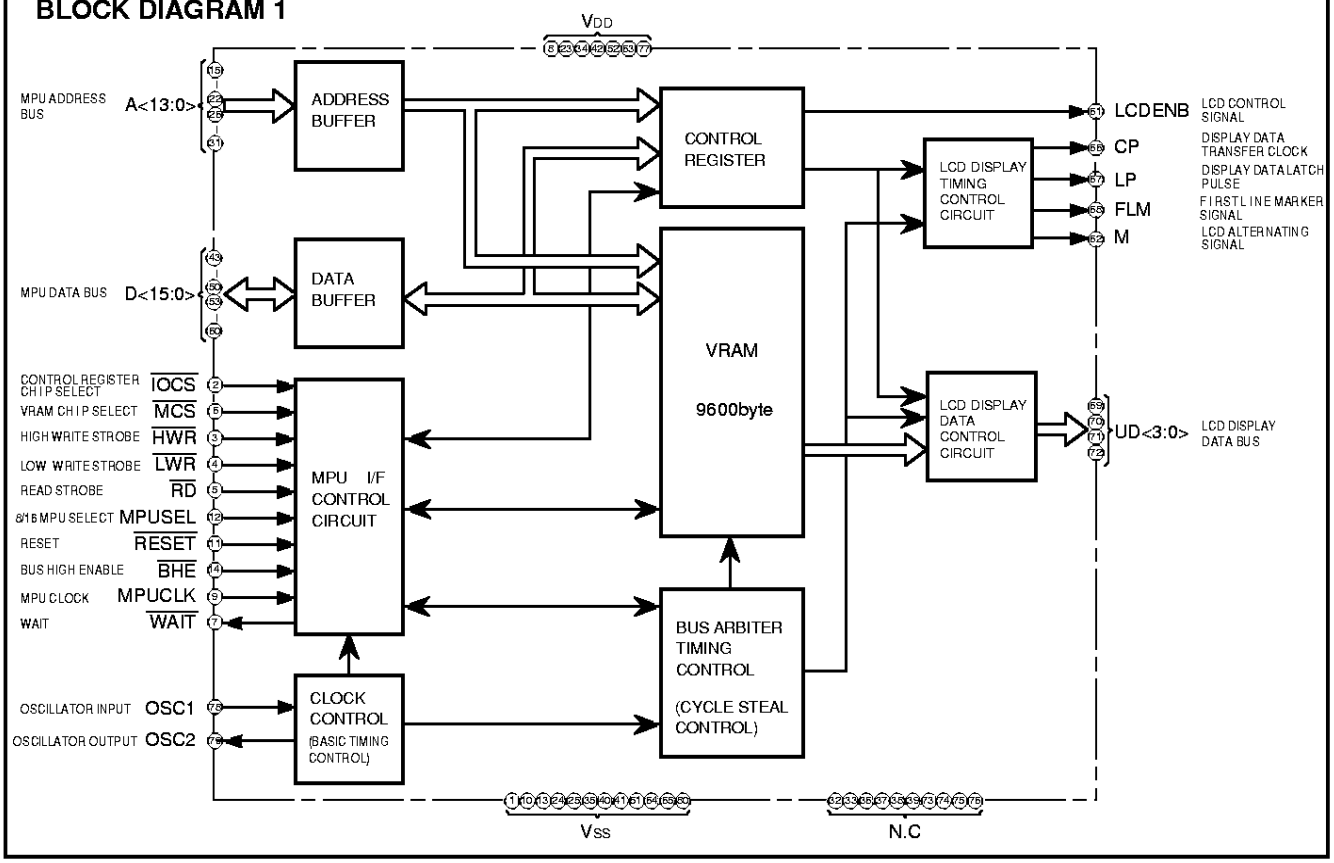
PIN CONFIGURATION(TOP VIEW)



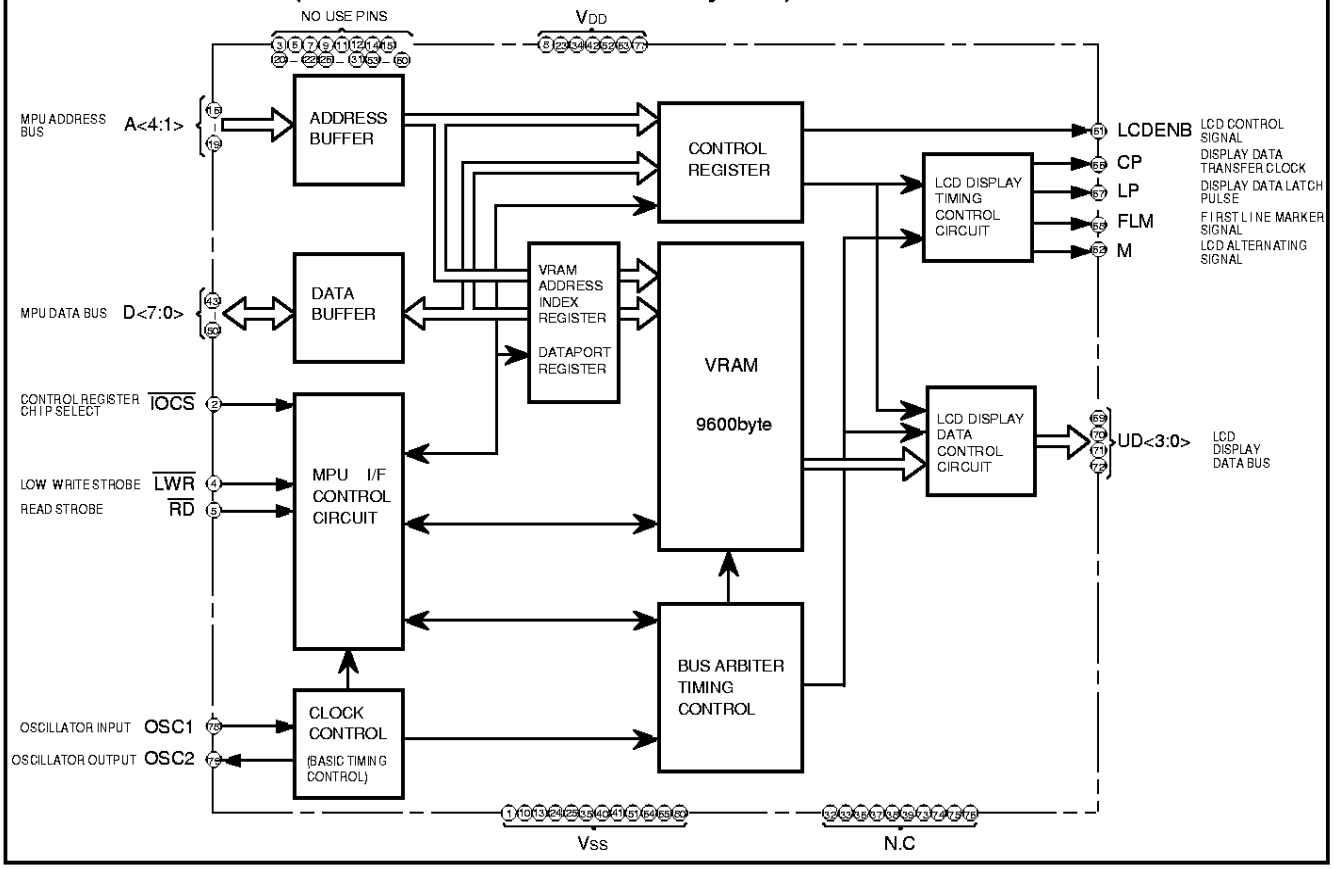
Outline 80P6N-A

N.C : No Connection

BLOCK DIAGRAM 1



BLOCK DIAGRAM 2 (In case of LCD module built-in system)



PIN DESCRIPTIONS

Item	Pin name	Input/ Output	Function	Number of pins
MPU interface	D<15:0>	Input/ Output	MPU data bus Connect to MPU data bus. Selecting 8bit MPU by MPUSEL input, D<15:8> connect to V_{DD} or V_{SS}.	16
	A<13:0>	Input	MPU address bus Connect to MPU address bus. When selecting 8-bit MPU, use A<13:0>. And selecting 16-bit MPU, use A<13:1> for the address bus with combining A<0> and $\overline{BHE}$ by the method of access to internal VRAM (Refer to Figure-1). Use A<4:0> for selecting address of control register.	14
	$\overline{IOCS}$	Input	Chip select input of control register When this pin is "L", select the internal control register. Assign to I/O space of MPU.	1
	$\overline{MCS}$	Input	Chip select input of VRAM When this pin is "L", select the internal VRAM. Assign to memory space of MPU.	1
	$\overline{HWR}$	Input	High-Write strobe input When this pin is "L", data write to the internal VRAM. $\overline{HWR}$ is valid only in using 16-bit MPU controlled byte access by $\overline{LWR}$ and $\overline{HWR}$. (Refer to Figure-1)	1
	$\overline{LWR}$	Input	Low-Write strobe input When this pin is "L", data write to the internal control register or VRAM. (Refer to Figure-1)	1
	$\overline{RD}$	Input	Read strobe input When this pin is "L", data read from the internal control register or VRAM.(Refer to Figure-1)	1
	MPUSEL	Input	8/16-bit MPU select input According to MPU, set "V_{SS}" for 8bit MPU and set "V_{DD}" for 16bit MPU.	1
	$\overline{RESET}$	Input	Reset input Use reset signal of MPU.When this pin is "L", initialize all internal control register and counter.	1
	MPUCLK	Input	MPU clock Input of MPU clock.	1
	$\overline{BHE}$	Input	Bus-High-Enable input This pin is valid when using 16-bit MPU controlled byte access by A<0> and $\overline{BHE}$ (Refer to Figure-1). Connect to "V_{DD}" when using 8-bit MPU. Set to "L" when using the additional function for the LCD Module built-in system.	1
	$\overline{WAIT}$	Output	WAIT output for MPU This signal makes WAIT for MPU. Change $\overline{WAIT}$ "L" at timing of falling edge of overlapping with $\overline{MCS}$ and ($\overline{RD}$ or $\overline{LWR}$ or $\overline{HWR}$). And return to "H" at synchronizing with the rising edge of MPUCLK after internal processing. (Output $\overline{WAIT}$ only when requested access from MPU to VRAM during cycle steal access.)	1
LCD interface	UD<3:0>	Output	Display data bus for LCD Transfer the LCD display data with 4-bit parallel signal. Mutually output upper/lower data every CP output.	4
	CP	Output	Display data transfer clock Shift clock for the transfer of display data to LCD. Take the display data of UD<3:0> to LCD at falling edge of CP.	1
	LP	Output	Display data latch pulse This clock use both as the latch pulse of display data for LCD and the transfer of scanning signal. LP output when finish the transfer of display data of a line. Latch of display data and the transfer of scanning signal at falling edge of LP.	1
	FLM	Output	First line marker signal Output the start pulse of scanning line. This signal is "H" active,the IC for driving scanning line catch FLM at falling edge of LP.	1
	M	Output	LCD alternating signal output Signal for driving LCD by alternating current.	1
	LCDENB	Output	LCD(ON/OFF) control signal output Output data which is set at bit"0 " of mode register(R1) in control register. This signal can use for controlling the LCD power supply, because LCDENB set to "L" byRESET.	1
Oscillator	OSC1	Input	Input pin for oscillator Generate an internal clock. For crystal oscillator or external clock signal.	1
	OSC2	Output	Output pin for oscillator	1
Others	V_{DD}	——	Power supply.(source +5V)	7
	V_{SS}	——	Ground	12
	N.C	——	No connection	10

OUTLINE

M66271FP is graphic display only controller for displaying a dot matrix type LCD. This IC has a built-in display data memory (VRAM) which is equivalent to 320×240 dots LCD.

● Control register

When access the control register from MPU side, use $\overline{IOCS}$, $\overline{LWR}$,$\overline{RD}$,A<4:0> and D<7:0>. Refer to Table-1,when set control type inputs.

Control registers are R1 – R8 for the normal mode function and R9 – R11 for the exclusive register for the LCD module built-in system.

● VRAM

When access VRAM from MPU side, use $\overline{MCS}$,$\overline{HWR}$,$\overline{LWR}$, $\overline{RD}$,$\overline{BHE}$, A<13:0> and D<15:0>. And enable to correspond to both 8-bit and 16-bit MPU by using MPUSEL input. Refer to Figure-1 and Table-2 – 6 for a form of VRAM and input setting for 8/16-bit MPU.

● Cycle steal system

Cycle steal is interact method of transferring display data for LCD from VRAM and accessing VRAM from MPU on the basic cycle of OSC.

Basic timing is two clocks of OSC,and assign first clock to the access from MPU to VRAM and second clock to the transfer of display data from VRAM to LCD.

In accessing VRAM from MPU,output $\overline{WAIT}$. Change $\overline{WAIT}$ to "L" at the timing of the falling edge of overlapping with $\overline{MCS}$ and ($\overline{RD}$ or $\overline{LWR}$/$\overline{HWR}$). And return to "H" at synchronizing with rising edge of MPUCLK after internal processing.

Cycle steal system can transfer data with more efficient. This function access with the cycle steal method as taking $\overline{WAIT}$ for MPU during the display term with necessity for the display data transfer from built-in VRAM to LCD. On other side, don't output $\overline{WAIT}$ for keeping throughput of MPU during horizontal synchronous term with no necessity for the display data transfer from VRAM to LCD side.

Refer to the following description of cycle steal.

● Output to LCD side

LCD display data UD<3:0> output synchronized with the rising edge of CP output per 4bits.

LP output synchronized with the falling edge of OSC when finish the transfer of display data for a line.

Enable to adjust the fittest value of the frame frequency requested by the LCD PANEL side with adjusting pulse width by LPW register.

FLM output, when finish the transfer of display data of 1st line.

M output is the LCD alternating signal which is signal for driving LCD by alternating current.

M-cycle enable to set variably by M-cycle variable register in line unit, and enable to utilize for preventting LCD from being inferior.

Difference in VRAM between 8-bit and 16-bit MPU

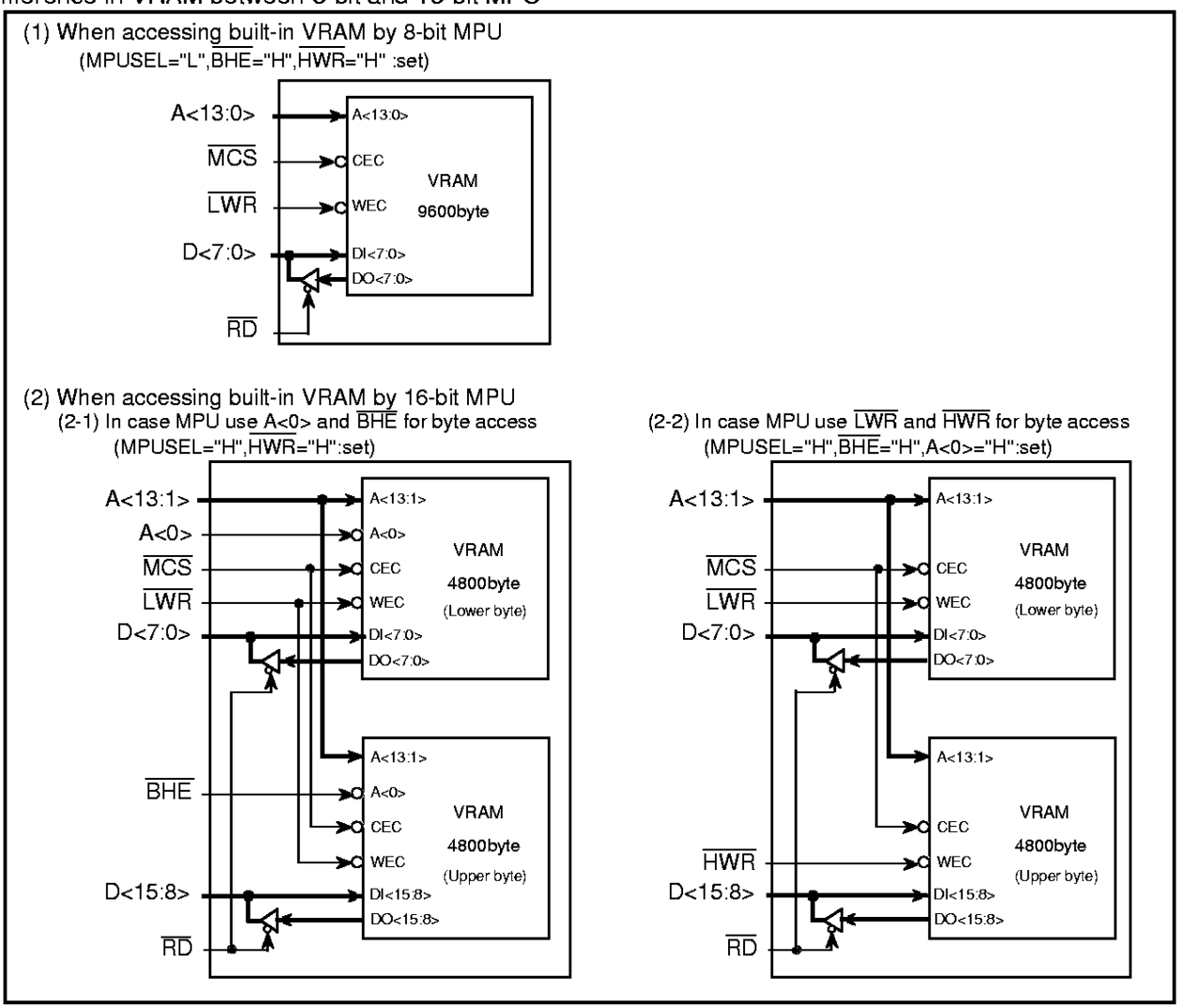


Figure-1 Difference in VRAM between 8-bit and 16-bit MPU

Combination of control input pins for MPU interface

Table-1 – 6 show conditions of input setting when access the control register and VRAM from MPU

(1) Access control register (Use address=A<4:0>,Data=D<7:0>)

Table-1

$\overline{IOCS}$	$\overline{LWR}$	$\overline{RD}$	Operation
L	L	H	Write to control register
L	H	L	Read from control register
H	X	X	Invalid

(2) Writing to VRAM

(2-1) When use 8-bit MPU (MPUSEL="L",$\overline{BHE}$=$\overline{HWR}$="H":set)

Table-2

MPU SEL	$\overline{MCS}$	$\overline{BHE}$	A<0>	$\overline{HWR}$	$\overline{LWR}$	Odd address	Even address	Valid data bus width of MPU
L	L	H	L	H	L	Invalid	Write	8-bit
			H			Write	Invalid	
			X		H	Invalid	Invalid	
	H		X		X			

(2-2) When use 16-bit MPU (In MPU controls byte access with A<0> and $\overline{BHE}$. MPUSEL=$\overline{HWR}$="H":set)

Table-3

MPU SEL	$\overline{MCS}$	$\overline{BHE}$	A<0>	$\overline{HWR}$	$\overline{LWR}$	Upper byte	Lower byte	Valid data bus width of MPU
H	L	L	L	H	L	Write	Write	16-bit
					H	Invalid	Invalid	
			H		L	Write	Invalid	Upper 8-bit
					H	Invalid	Invalid	
		H	L		L	Invalid	Write	Lower 8-bit
					H	Invalid	Invalid	
			H		L	Invalid	Write	Lower 8-bit
					H	Invalid	Invalid	
	H	X	X		X			

← Even if A<0>="H", enable to write

(2-3) When use 16-bit MPU (In MPU controls byte access with $\overline{LWR}$ and $\overline{HWR}$. MPUSEL=$\overline{BHE}$=A<0>="H":set)

Table-4

MPU SEL	$\overline{MCS}$	$\overline{BHE}$	A<0>	$\overline{HWR}$	$\overline{LWR}$	Upper byte	Lower byte	Valid data bus width of MPU
H	L	H	H	L	L	Write	Write	16-bit
					H	Write	Invalid	Upper 8-bit
				H	L	Invalid	Write	Lower 8-bit
					H	Invalid	Invalid	
	H			X	X			

(3) Reading from VRAM

(3-1) When use 8-bit MPU (MPUSEL="L",$\overline{BHE}$="H":set)

Table-5

MPU SEL	$\overline{MCS}$	$\overline{BHE}$	A<0>	$\overline{RD}$	Odd address	Even address	Valid data bus width of MPU
L	L	H	L	L	Invalid	Read	8-bit
			H		Read	Invalid	
			X	H	Invalid	Invalid	
	H			X			

(3-2) When use 16-bit MPU (MPUSEL="H":set)

Table-6

MPU SEL	$\overline{MCS}$	$\overline{BHE}$	A<0>	$\overline{RD}$	Upper byte	Lower byte	Valid data bus width of MPU
H	L	X	X	L	Read	Read	16-bit
				H	Invalid	Invalid	
	H			X			

Note:Avoid setting combination except above,as cause of error action
:X="L" or "H"

Description of cycle steal

BASIC TIMING

Basic timing of M66271FP is two clocks of OSC (internal clock after dividing OSC1 input).
Assign first clock to accessing from MPU to VRAM and second clock to transferring of display data from VRAM to LCD

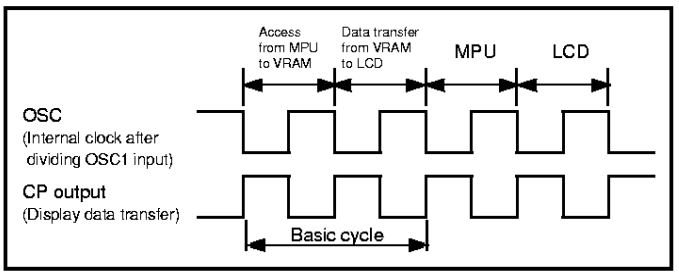


Figure-2 BASIC TIMING

Operation cycle of MPU access(during $\overline{WAIT}$ output)

Writing or Reading operation for VRAM during cycle steal needs 1 cycle in best case or 3 cycles in worst case, according to the condition of the internal cycle steal at staring access requested from MPU.

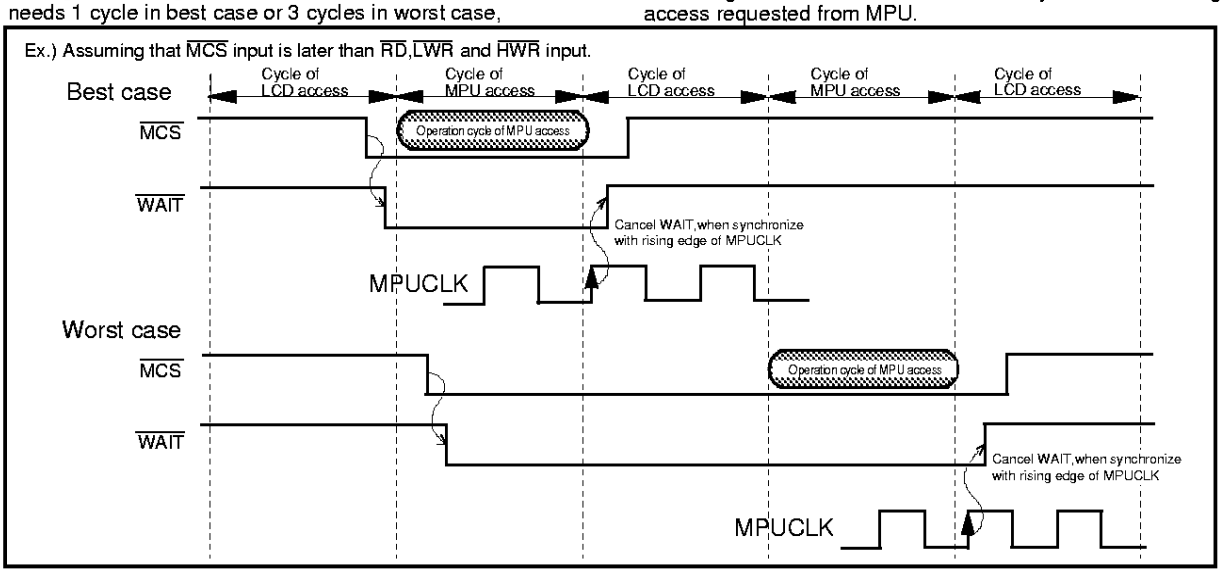


Figure-3 Operation cycle of MPU access

Function of cycle steal control

M66271FP has a function for processing data of a line with more efficient. This function access with the cycle steal method as taking $\overline{WAIT}$ for MPU during the display term with necessity for the display data transfer from built-in VRAM to LCD.
On other side, don't output $\overline{WAIT}$ for keeping throughput of MPU during the horizontal synchronous term with no necessity for the display data transfer from VRAM to LCD side.
But certainly set a term of accessing with the cycle steal method by CSW register, for controlling an error action near the end of horizontal synchronous term.

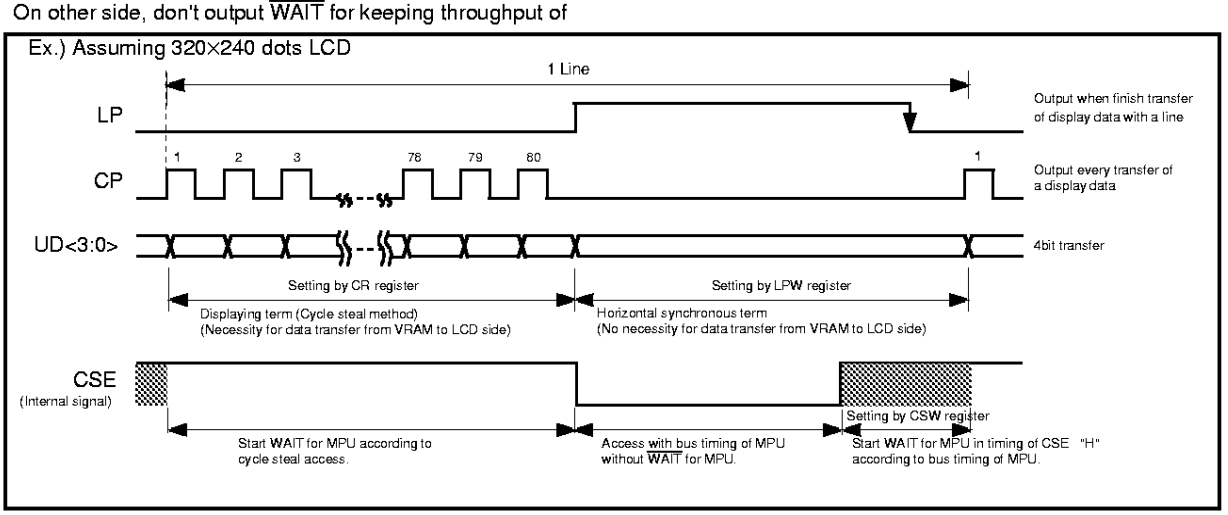


Figure-4 Function of cycle steal control

Handling of oscillator pin

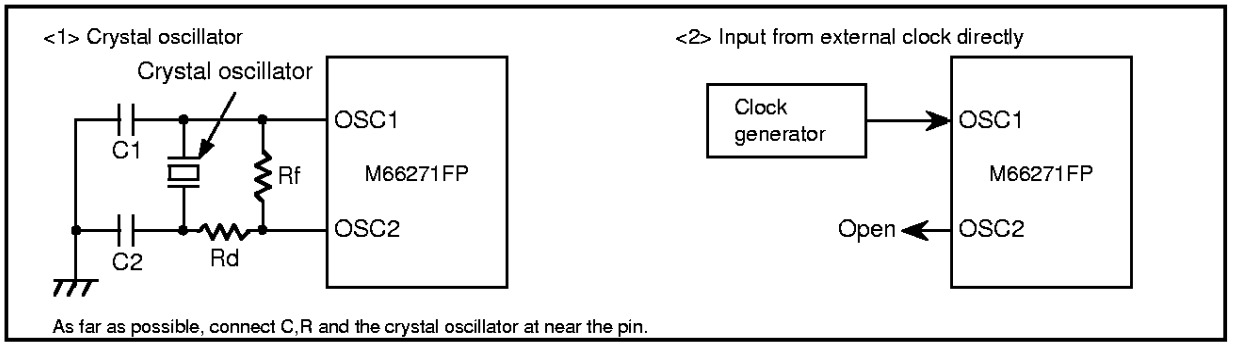


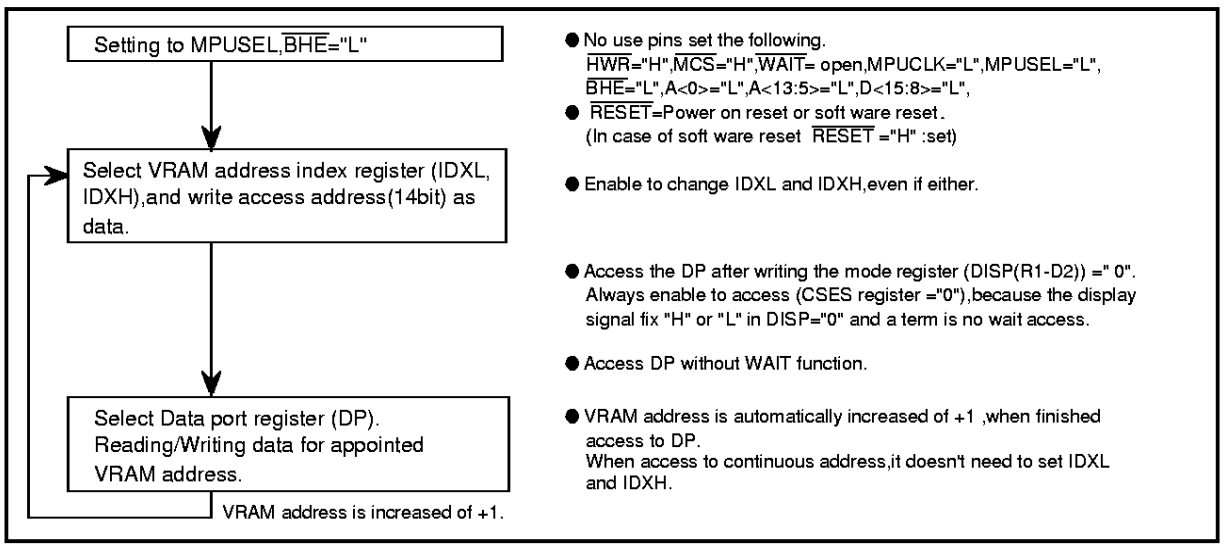
Figure-5 Oscillator pin

Additional function for LCD module built-in system

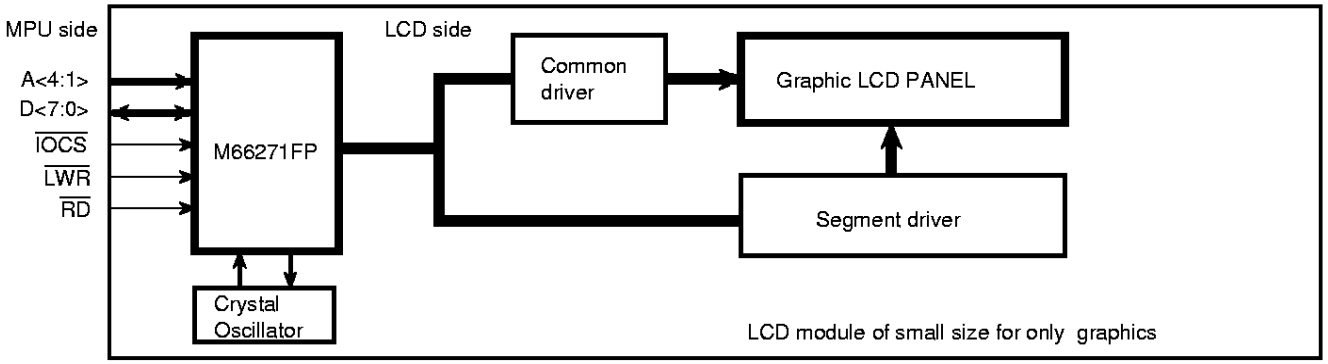
As all of the VRAM address in M66271FP are externally opened for addressing VRAM from MPU directly.
When consider the LCD module built-in system,connect pins are increased.
But M66271FP has an additional function for the LCD module built-in system by lessening connect pins.

Outline of the additional function for the LCD module built-in system

- Interface pins with MPU
  15 kinds of Interface with MPU:A<4:1>,D<7:0>,$\overline{IOCS}$,$\overline{LWR}$,$\overline{RD}$
- Method of accessing the internal VRAM
  Access the internal VRAM through the VRAM address index register (IDXL,IDXH) and the Data port register (DP) which are used for I/O register.
  The following show the process of accessing VRAM.



Application



Control register

M66271FP has 9 kinds of control register.
To set mode from MPU to control register,use $\overline{IOCS}$,
$\overline{LWR}$,$\overline{RD}$,A<4:0> and D<7:0>.

(1) Kind of control register

Control register Table

Kind of register		Address					Data								Functions of register	R/W
No.	Name	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0		
R1	Mode register	0	0	0	0	0	CSES	RESET	← OSCC →			DISP	REV	LCDE	D6 – D0 set the basic mode. D7 is the status register of cycle steal state.	R/W D7=Only "R"
R2	Horizontal display character number register	0	0	0	1	0	/	/	← CR →						Set the number of horizontal display characters per line.	W
R3	Horizontal synchronous pulse width register	0	0	1	0	0	← LPW →								Set the pulse width of LP per line.	W
R4	Cycle steal enable width register	0	0	1	1	0	← CSW →								Set the term of cycle steal enable access during horizontal synchronous term.	W
R5	Vertical line number register	0	1	0	0	0	← SLT →								Set the number of display line of vertical direction.	W
R6	Display start address register	0	1	0	1	0	← SAL →								Set the display start address of VRAM. Set lower 8-bit to SAL and upper 6-bit to SAH. Max=257FH	R/W
R7		0	1	1	0	0	/	/	← SAH →							
R8	M cycle variable register	0	1	1	1	0	← MT →								Set the cycle of LCD alternating signal from M .	W
R9	Data port register	1	0	0	0	0	← DP →								Data port register for accessing VRAM through the register.	R/W
R10	VRAM address index register	1	0	0	1	0	← IDXL →								Set the address for accessing VRAM. Set lower 8-bit to IDXL and upper 6-bit to IDXH. Max=257FH And automatically increase in continuous address .	R/W
R11		1	0	1	0	0	/	/	← IDXH →							

Note:Data port register(DP) and VRAM address index register(IDXL,IDXH) are exclusive register,when using this IC for the LCD module built-in system.
When RESET,each register is initialize the setting which is assumed LCD size of 320×240 dots.
Then,even if each register has not setting,output the signal to LCD side ,it is possible to be alternation of LCD.

(2) Description of register

(2-1) Mode register [R1]

Address	R/W	Function	Reset
00000	R/W D7= Only "R"	**D7 CSES** 0 No wait access 1 Cycle steal access • Status register for identifying active or inactive in cycle steal function. • Set "1" during active with cycle steal function. • CSES is for only reading,not for writing.	0
		D6 RESET 0 Reset OFF 1 Reset ON • Software reset. • Surely return to reset off after reset on.	0
		OSCC (D5 D4 D3) — Division of OSC1 0 0 0 — 1 0 0 1 — 1/2 Division 0 1 0 — 1/4 Division 0 1 1 — 1/8 Division 1 0 0 — 1/16 Division • Set the division of OSC clock for internal operation from OSC1 input pin. • When reset,OSCC=000,OSC1 clock doesn't divide. • Don't set except left table.	000
		D2 DISP 0 Display OFF 1 Display ON • Control the displaying ON/OFF of LCD. • When reset,DISP=0,set display OFF. • REV(D1) set "1", and when DISP= "0" display data UD<3:0> output "1" in reversal mode.	0
		D1 REV 0 Normal display 1 Reversal display • Control normal/reversal of LCD display. • When reset,REV=0,set normal display . • In using LCD of permeation method,REV="1" has effect.	0
		D0 LCDE 0 LCDENB="0"output 1 LCDENB="1"output • Set the output data from LCDENB output pin. • When reset,LCDE=0,LCDENB output "0"(Vss potential). • This function is prepared for controlling the voltage of LCD. When the power supply is ON after finish each register setting ,LCDE="1",supply voltage of LCD. Conversely for setting power supply OFF,first LCDE="0",the voltage of LCD is OFF. Therefore enable to prevent LCD from being unusual voltage as DC. This function use for satisfy the need of LCD.	0

(2-2) Horizontal display characters number register [R2]

Address	R/W	Function	Reset
00010	W	CR (D7 D6 D5 D4 D3 D2 D1 D0) — Character number — Display dot number 0 0 0 0 0 0 — — 0 0 0 0 0 1 — 1 — 8 0 0 0 0 1 0 — 2 — 16 1 1 1 1 1 1 — 63 — 504 • The number of horizontal display characters per line can set to the extent of max=504 dots(=63 characters) • When reset,CR= "28H"(=40 characters =320 dots)	28H

Note: Definition of the number of display characters
The number of display characters means data which is corresponding with 1 byte of VRAM.
In case of binary,1 bit of VRAM corresponds to 1 dot of display,then 1 character means 8 dots of display.

(2-3) Horizontal synchronous pulse width register [R3]

Address	R/W	Function	Reset
00100	W	LPW: D7 D6 D5 D4 D3 D2 D1 D0 — Character number: 0 0 0 0 0 0 0 0 — ; 0 0 0 0 0 0 0 1 — 1 ; 0 0 0 0 0 0 1 0 — 2 ; ↓ ; 1 1 1 1 1 1 1 1 — 255 • Set the length of horizontal synchronous pulse width which appeared per line in character unit. Horizontal synchronous pulse output from LP output pin,and use for changing serial/parallel of displaying data. Adjusting this pulse width is possible to set frame frequency the fittest value. And the actual LP output pulse is (LPW setting value - 1CP) in consideration of timing with CP output. • When reset,LPW= "01H"(=1 character)	01H

(2-4) Cycle steal enable width register [R4]

Address	R/W	Function	Reset
00110	W	CSW: D7 D6 D5 D4 D3 D2 D1 D0 — Character number: 0 0 0 0 0 0 0 0 — ; 0 0 0 0 0 0 0 1 — 1 ; 0 0 0 0 0 0 1 0 — 2 ; ↓ ; 1 1 1 1 1 1 1 1 — 255 • During the horizontal synchronous term, set term of access by cycle steal method in character number unit. Setting value of CSW sets below LPW value. • When reset,CSW= "00H". Note: Be careful with first and second byte of display data UD<3:0> output indefinite data when setting value of CSW is still reset (00H). Surely CSW set over 01H. (When select 8-bit MPU,1 byte is indefinite. When 16-bit and SAL:D<0>=0, 2 byte are indefinite. When 16-bit and SAL:D<0>=1, 1 byte is indefinite.)	00H

(2-5) Vertical line number register [R5]

Address	R/W	Function	Reset
01000	W	SLT: D7 D6 D5 D4 D3 D2 D1 D0 — Vertical line number: 0 0 0 0 0 0 0 0 — ; 0 0 0 0 0 0 0 1 — 1 ; 0 0 0 0 0 0 1 0 — 2 ; ↓ ; 1 1 1 1 1 1 1 1 — 255 • SLT combine the setting of display driving duty of LCD. • Setting of SLT is sure to adjust to the number of display line of LCD. • When reset,SLT= "F0H"(=240 lines).	F0H

(2-6) Display start address register [R6,R7]

Address	R/W	Function	Reset
01010 SAL	R/W	See table below	0000H
01100 SAH			

SAH								SAL								Display start address
D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0	
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000H
		0	0	0	0	0	0	0	0	0	0	0	0	0	1	0001H
		0	0	0	0	0	0	0	0	0	0	0	0	1	0	0002H
		↓								↓						↓
		1	0	0	1	0	1	0	1	1	1	1	1	1	1	257FH

- D6 and D7 output "0" when read SAH.
- It is possible to set display start address to the extent of 257FH (=9600 address).
- Don't set over 2580H.
- When reset,SAL and SAH= "0000H".
- Display start address is established by the writing data to SAH register. Even if only change SAL, surely set SAH after SAL.
- When select 8-bit MPU,start address set in SAL <D7 – D0> + SAH <D5 – D0>.
  When select16-bit MPU,start address set in SAL <D7 – D1> + SAH <D5 – D0>.
- Even if selecting 16-bit MPU,enable to set display start address in character unit.
  In case the display reading data from VRAM start at D<15:12>,set SAL <D0>="0", and if start at D<7:4>,set SAL <D0>="1". (Refer to Figure-8)

(2-7) M cycle variable register [R8]

Address	R/W	Function	Reset
01110	W	See table below	00H

MT								Cycle of M
D7	D6	D5	D4	D3	D2	D1	D0	
0	0	0	0	0	0	0	0	Toggle change at every 1 frame.
0	0	0	0	0	0	0	1	Toggle change at every 1 line(1LP).
0	0	0	0	0	0	1	0	Toggle change at every 2 lines.
				↓				↓
1	1	1	1	1	1	1	1	Toggle change at every 255 lines.

- Set the cycle of M. In case of MT=01H,M repeat reversal(toggle) at every 1 line (at every 1 count of LP).
- When reset,MT="00H",toggle M signal at every 1 frame.
- We recommend this register set suitable value for user's LCD.

(2-8) Data port register [R9]

Address	R/W	Function	Reset
10000	R/W	See table below	XXH (indefinite)

DP								Data port (8bit)
D7	D6	D5	D4	D3	D2	D1	D0	

- Exclusive data port register for the LCD module built-in system.
  Reading or writing 8bit data between MPU and VRAM through this register.
- VRAM address index register (IDXL,IDXH) is increased of +1,when finished access to DP.
- Output indefinite data when reset.

(2-9) VRAM address index register [R10,R11]

Address	R/W	Function	Reset

	IDXH							IDXL								Accessing VRAM address
	D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0	
10010 IDXL			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000H
			0	0	0	0	0	0	0	0	0	0	0	0	0	1	0001H
			0	0	0	0	0	0	0	0	0	0	0	0	1	0	0002H
					↓						↓						↓
10100 IDXH			1	0	0	1	0	1	0	1	1	1	1	1	1	1	257FH

R/W

0000H

- Exclusive VRAM address index register for the LCD module built-in system.
- It is possible to change the register only one side,because IDXH and IDXL are independent each other.
- It is possible to set VRAM access address to the extent of 257FH (=9600 address).
- Don't set address over 2580H.
- D6 and D7 output "0" when read IDXH
- When reset,IDXL and IDXH="0000H".

Description of LCD display

Relation between setting of control register and LCD displaying

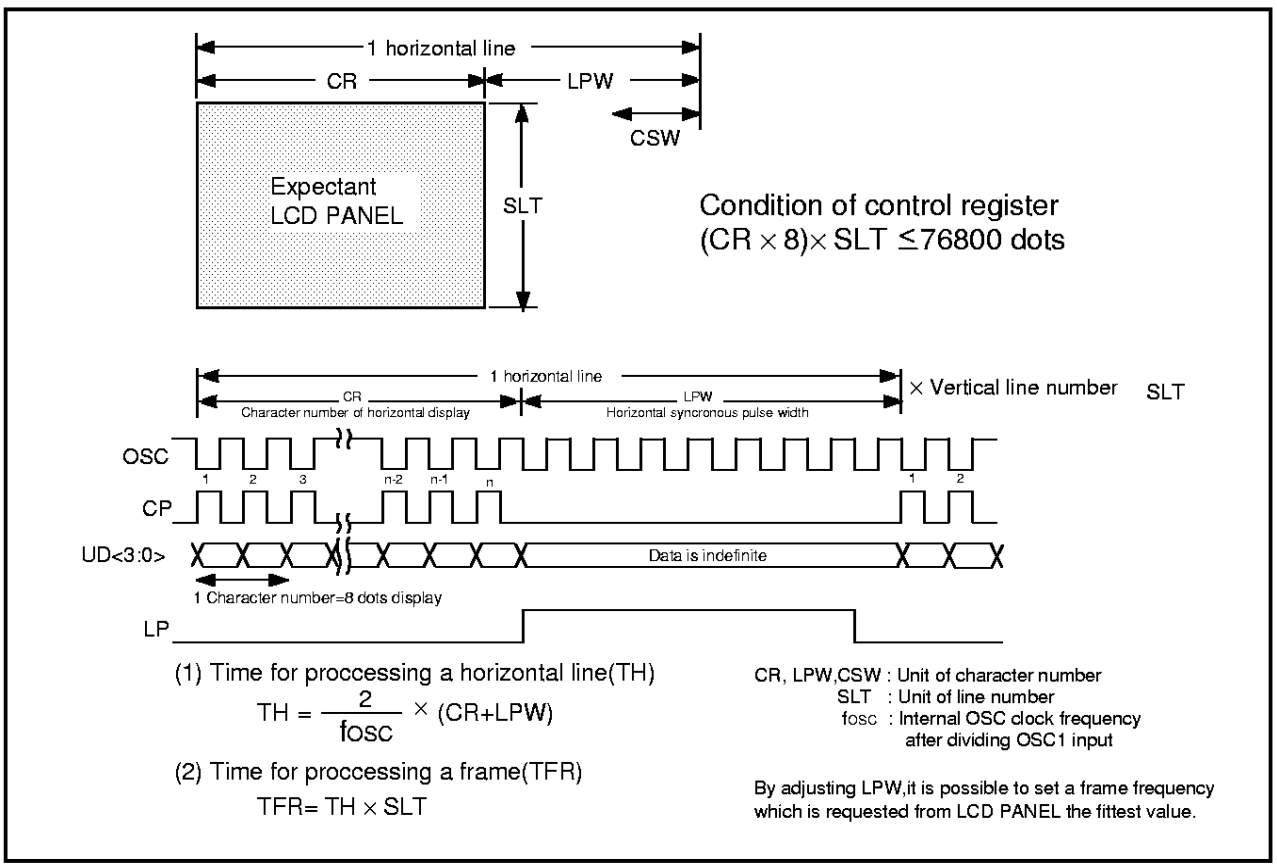


Figure-6 Relation between setting of control register and LCD displaying

Relation between address of VRAM and LCD display

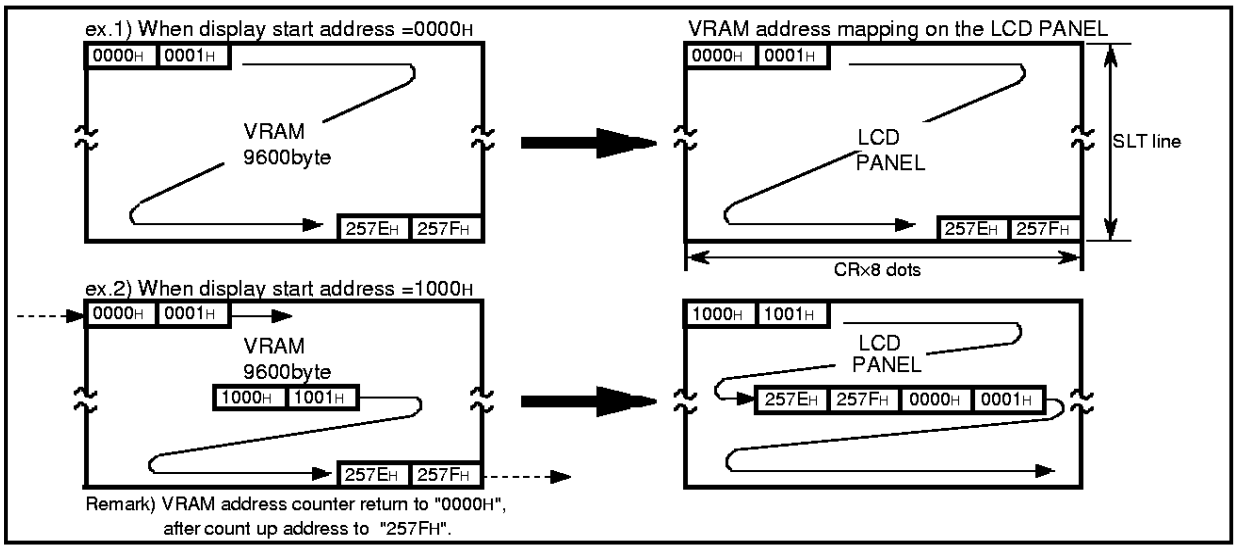


Figure-7 Relation between address of VRAM and LCD display

Relation between VRAM data ,LCD display and display start address register

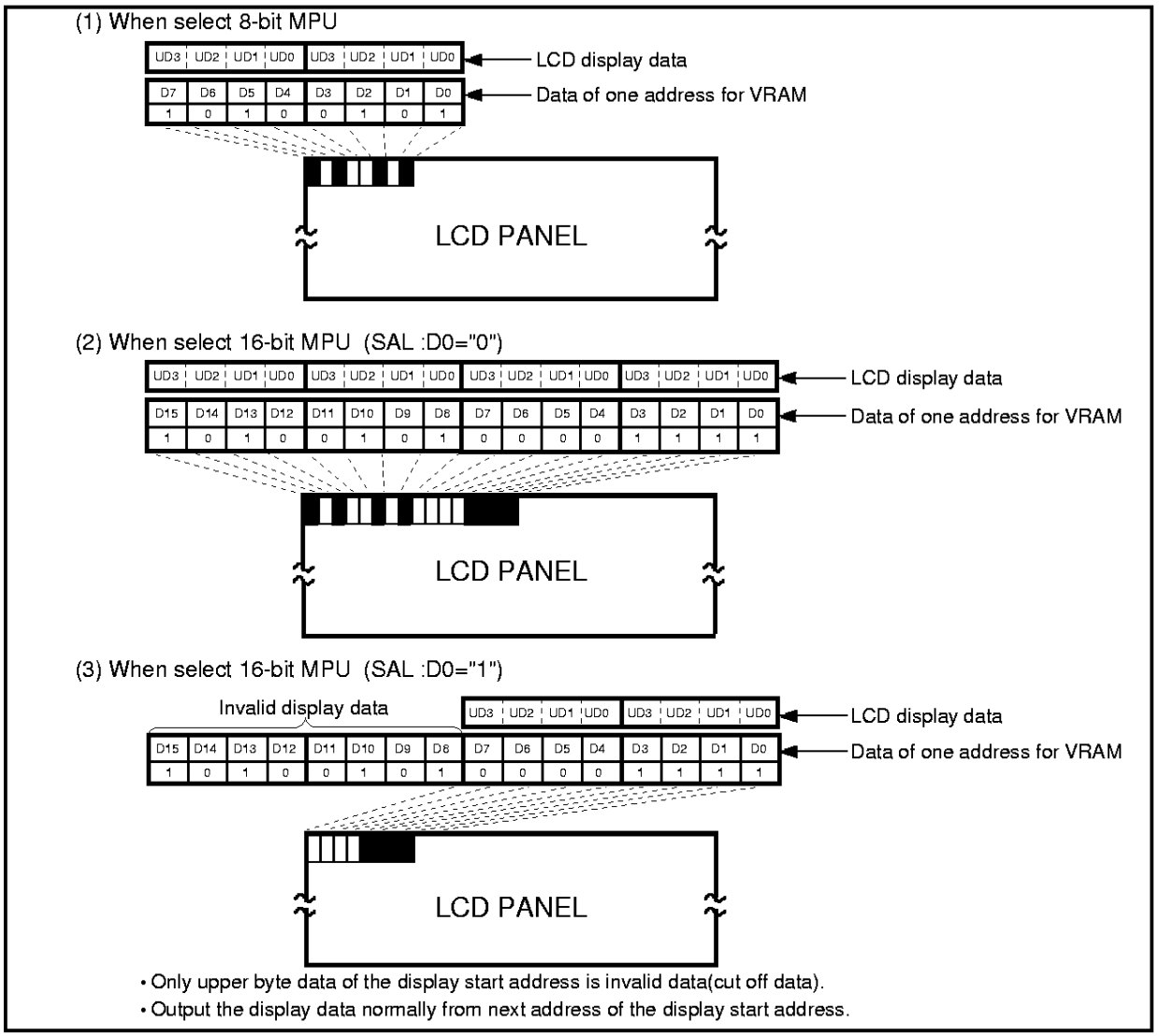
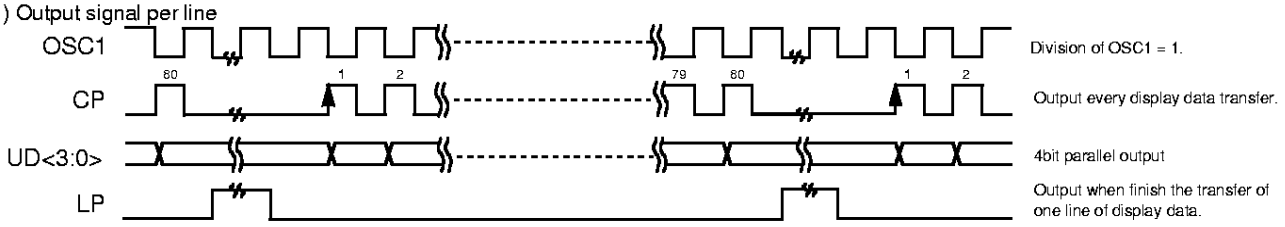


Figure-8 Relation between VRAM data ,LCD display and display start address register

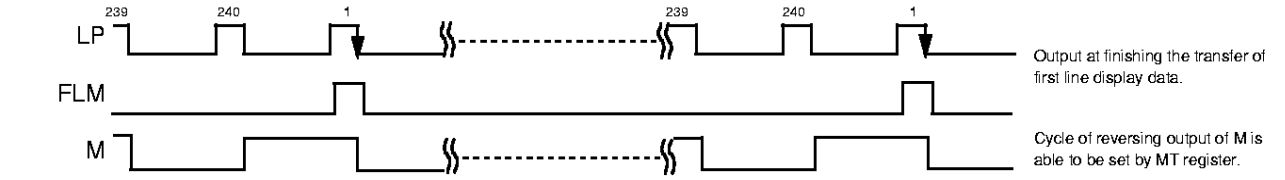
Output signal of LCD side

Ex.) Assuming 320×240 dots LCD
(In setting of CR=40characters,LPW=2characters,SLT=240lines,OSCC=1division,MT=1toggle per line)

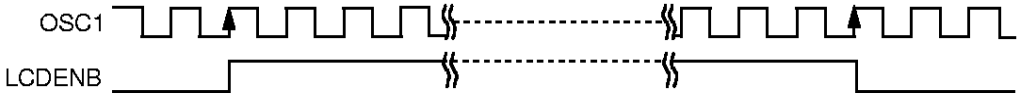
(1) Output signal per line



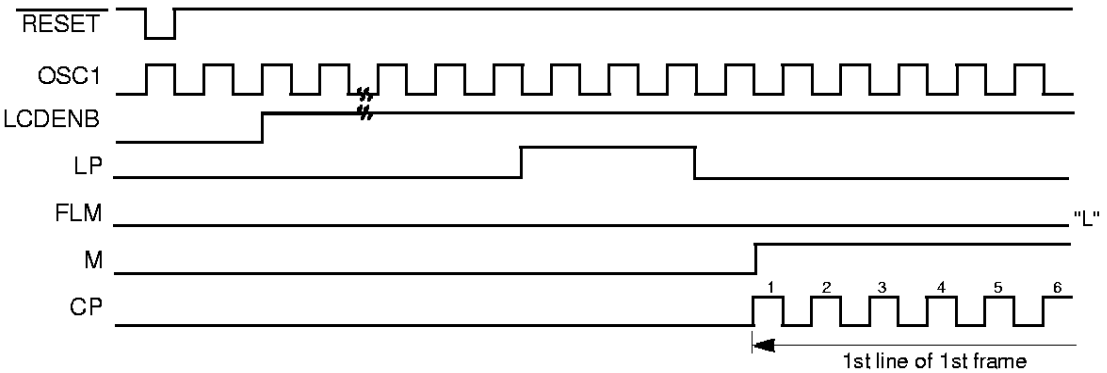
(2) Output signal per frame



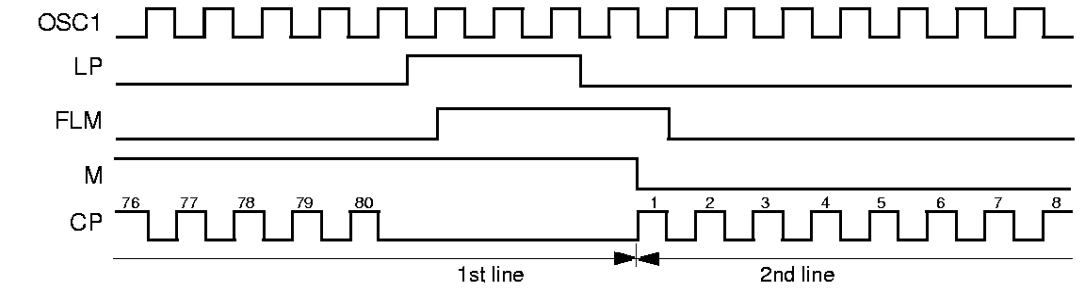
(3) LCDENB output signal



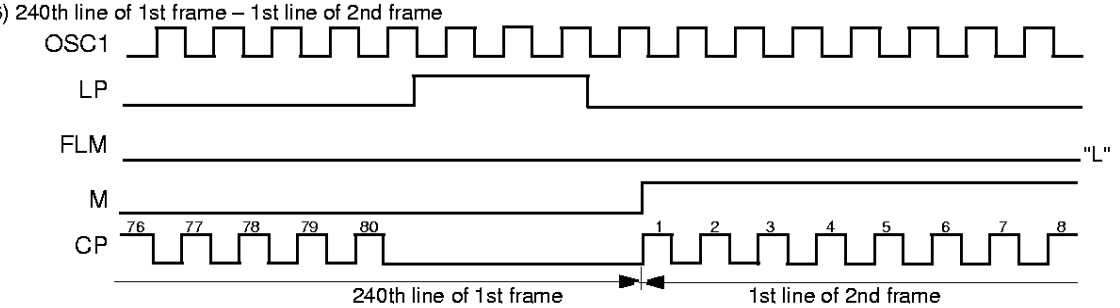
(4) Reset – 1st line of 1st frame



(5) 1st line – 2nd line



(6) 240th line of 1st frame – 1st line of 2nd frame



ABSOLUTE MAXIMUM RATINGS (Ta=0 – +70˚C unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{DD}	Supply voltage		–0.3 – +6.5	V
V_I	Input voltage		–0.3 – V_{DD}+0.3	V
V_O	Output voltage		–0.3 – V_{DD}+0.3	V
I_O	Output current		±10	mA
Pd	Power dissipation		600	mW
Tstg	Storage temperature		–55 – +150	˚C

RECOMMENDED OPERATING CONDITIONS (Ta=0 – +70˚C unless otherwise noted)

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{DD}	Supply voltage		4.5	5.0	5.5	V
V_{SS}	Supply voltage			0		V
V_I	Input voltage		0		VDD	V
V_O	Output voltage		0		VDD	V
Topr	Operating temperature		0	+25	+70	˚C

ELECTRICAL CHARACTERISTICS (V_{DD}=5V±10%, Ta=0 – +70˚C unless otherwise noted)

Symbol	Parameter		Conditions		Limits			Unit
					Min.	Typ.	Max.	
V_{IH}	High-level input voltage	All inputs except for OSC1, $\overline{RESET}$ and MPUSEL	V_{DD}=5.5V		2.2			V
V_{IL}	Low-level input voltage		V_{DD}=4.5V				0.8	V
V_{IH}	High-level input voltage	OSC1	V_{DD}=5.5V		3.5			V
V_{IL}	Low-level input voltage		V_{DD}=4.5V				1.0	V
V_{T+}	Positive-going threshold voltage	MPUSEL, $\overline{RESET}$	V_{DD}=5.0V		2.3		3.7	V
V_{T-}	Negative-going threshold voltage		V_{DD}=5.0V		1.25		2.3	V
V_{OH}	High-level output voltage	All outputs except for OSC2 and outputs of D<15:0>	V_{DD}=4.5V	I_{OH}=–4mA	4.1			V
V_{OL}	Low-level output voltage			I_{OL}= 4mA			0.4	V
V_{OH}	High-level output voltage	OSC2	V_{DD}=4.5V	I_{OH}=–50uA	4.1			V
V_{OL}	Low-level output voltage			I_{OL}= 50uA			0.4	V
I_{IH}	High-level input current		V_{DD}=5.5V, V_I=V_{DD}				10	µA
I_{IL}	Low-level input current		V_{DD}=5.5V, V_I=V_{SS}				–10	µA
I_{OZH}	Off-state high-level output current	D<15:0>	V_{DD}=5.5V, V_O=V_{DD}				10	µA
I_{OZL}	Off-state low-level output current		V_{DD}=5.5V, V_O=V_{SS}				–10	µA
$I_{DD(A)}$	Operating supply current (Average)		V_{DD}=5.5V, V_I=V_{DD} or V_{SS} fosc=10MHz, Output=open				40	mA
$I_{DD(S)}$	Stand-by supply current		V_{DD}=5.5V, $\overline{IOCS}$, $\overline{MCS}$=V_{DD} Others V_I=V_{DD} or V_{SS} (valid)				500	µA

SWITCHING CHARACTERISTICS (V_{DD}=5V±10%, Ta=0 – +70°C)

Symbol	Parameter	Test condition	Limits			Unit
			Min.	Typ.	Max.	
$t_{a(IOCS-D)}$ $t_{a(MCS-D)}$ $t_{a(RD-D)}$	IOCS data access time MCS data access time RD data access time	CL=50pF			70	ns
$t_{dis(IOCS-D)}$ $t_{dis(MCS-D)}$ $t_{dis(RD-D)}$	Output disable time after IOCS Output disable time after MCS Output disable time after RD				20	ns
$t_{pHL(MCS-WAIT)}$ $t_{pHL(WR-WAIT)}$ $t_{pHL(RD-WAIT)}$	WAIT output propagation time after MCS WAIT output propagation time after WR WAIT output propagation time after RD				40	ns
$t_{pLH(CLK-WAIT)}$	WAIT output propagation time after MPUCLK				20	ns
$t_{pd(OSC-CP)}$	CP output propagation time after OSC				40	ns
$t_{pLH(OSC-LP)}$ $t_{pHL(OSC-LP)}$	LP output propagation time after OSC				40	ns
$t_{a(UD)}$	UD access time				40	ns
$t_{pLH(OSC-FLM)}$ $t_{pHL(OSC-FLM)}$	FLM output propagation time after OSC				40	ns
$t_{pd(OSC-M)}$	M output propagation time after OSC				40	ns
$t_{pLH(OSC-LE)}$ $t_{pHL(OSC-LE)}$	LCDENB output propagation time after OSC				40	ns
$t_{pd(D-WAIT)}$	Data definite time before cancelling WAIT		0			ns

TIMING REQUIREMENTS (V_{DD}=5V±10%, Ta=0 – +70°C)

(1) Accessing to control register

Symbol	Parameter	Test condition	Limits			Unit
			Min.	Typ.	Max.	
$t_{W(IOCS)}$ $t_{W(LWR)}$	IOCS pulse width LWR pulse width		70			ns
$t_{su(D-IOCS)}$ $t_{su(D-LWR)}$	Data set up time before falling edge of IOCS Data set up time before falling edge of LWR		0			ns
$t_{h(IOCS-D)}$ $t_{h(LWR-D)}$	Data hold time after rising edge of IOCS Data hold time after rising edge of LWR		15			ns
$t_{su(A-IOCS)}$ $t_{su(A-LWR)}$ $t_{su(A-RD)}$	Address set up time before falling edge of IOCS Address set up time before falling edge of LWR Address set up time before falling edge of RD		15			ns
$t_{h(IOCS-A)}$ $t_{h(LWR-A)}$ $t_{h(RD-A)}$	Address hold time after rising edge of IOCS Address hold time after rising edge of LWR Address hold time after rising edge of RD		15			ns

(2) Accessing to VRAM

Symbol	Parameter	Test condition	Limits			Unit
			Min.	Typ.	Max.	
$t_{W(MCS)}$ $t_{W(WR)}$	MCS pulse width WR pulse width		70			ns
$t_{su(D-MCS)}$ $t_{su(D-WR)}$	Data set up time before falling edge of MCS Data set up time before falling edge of WR		0			ns
$t_{h(MCS-D)}$ $t_{h(WR-D)}$	Data hold time after rising edge of MCS Data hold time after rising edge of WR		15			ns
$t_{su(A-MCS)}$ $t_{su(A-WR)}$ $t_{su(A-RD)}$	Address set up time before falling edge of MCS Address set up time before falling edge of WR Address set up time before falling edge of RD		15			ns
$t_{h(MCS-A)}$ $t_{h(WR-A)}$ $t_{h(RD-A)}$	Address hold time after rising edge of MCS Address hold time after rising edge of WR Address hold time after rising edge of RD		15			ns

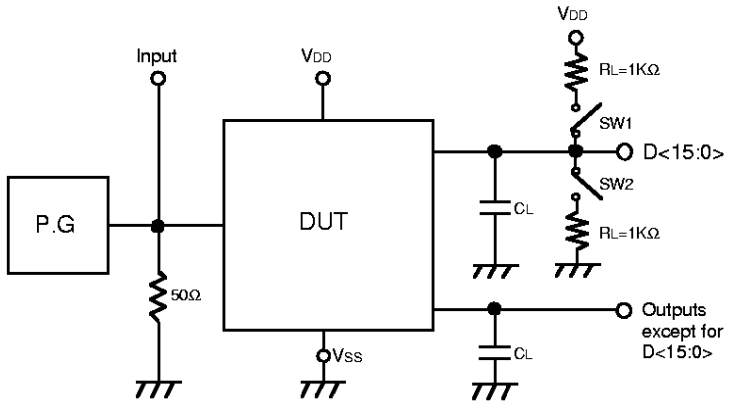
(3) Clock and accessing to LCD display

Symbol	Parameter	Test condition	Limits			Unit
			Min.	Typ.	Max.	
$t_{C(CLK)}$	MPUCLK cycle time		50			ns
$t_{WH(CLK)}$	MPUCLK "H" pulse width			$\frac{t_{C(CLK)}}{2}$		ns
$t_{WL(CLK)}$	MPUCLK "L" pulse width					
$t_{C(OSC)}$	OSC cycle time		50(note)			ns
$t_{WH(OSC)}$	OSC "H" pulse width			$\frac{t_{C(OSC)}}{2}$		ns
$t_{WL(OSC)}$	OSC "L" pulse width					
$t_{C(CP)}$	CP cycle time			$\frac{t_{C(OSC)}}{(1/n)}$		ns
$t_{WH(CP)}$	CP "H" pulse width			$\frac{t_{C(OSC)}}{2\cdot(1/n)}$		ns
$t_{WL(CP)}$	CP "L" pulse width					
$t_{W(FLM)}$	FLM pulse width			$\frac{2\cdot t_{C(OSC)}\cdot LPW}{(1/n)}$		ns

Note: Clock frequency of OSC1 input is less than fmax=20MHz.
Limit of OSC clock for the internal operation is fmax=10MHz.
When OSC1 is more than 10MHz from external input, set OSC clock up to 10MHz by using division of OSCC register.
Division is set with rising edge of OSC1 input.

1/n =Division of OSC1
LPW=Setting value of LPW register

Test circuit



Parameter	SW1	SW2
$t_{dis(LZ)}$	Closed	Open
$t_{dis(HZ)}$	Open	Closed
$t_{a(ZL)}$	Closed	Open
$t_{a(ZH)}$	Open	Closed

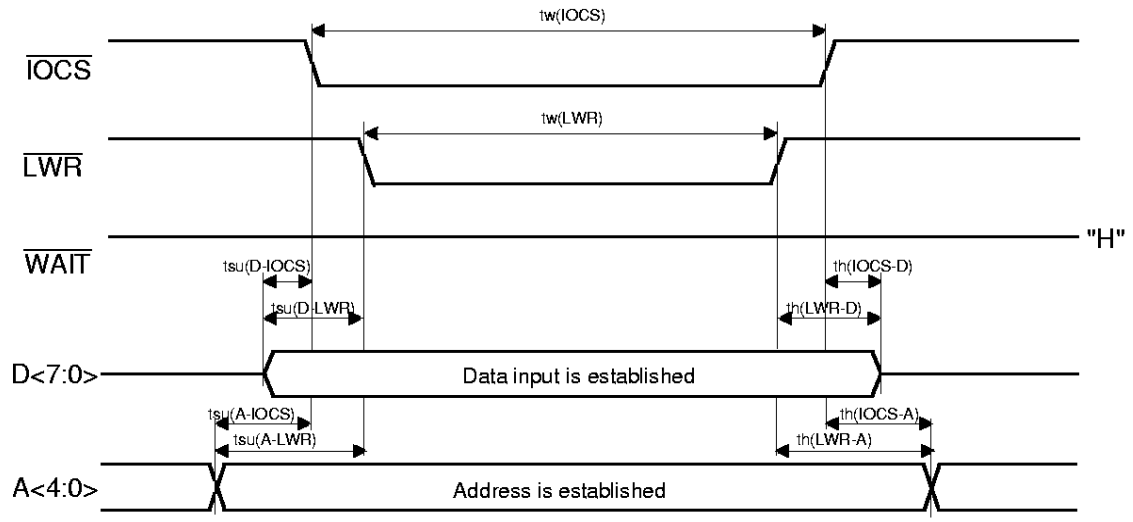
(1) Input pulse level : 0 – 3V
Input pulse rise/fall time : tr,tf=3ns
Input decision voltage : 1.5V
Output decision voltage : $V_{DD}/2$
(However,tdis(LZ) is 10% of output amplitude and tdis (HZ) is 90% of that for dezision.)

(2) Load capacity CL include float capacity of connection and input capacity of probe.

TIMING DIAGRAM

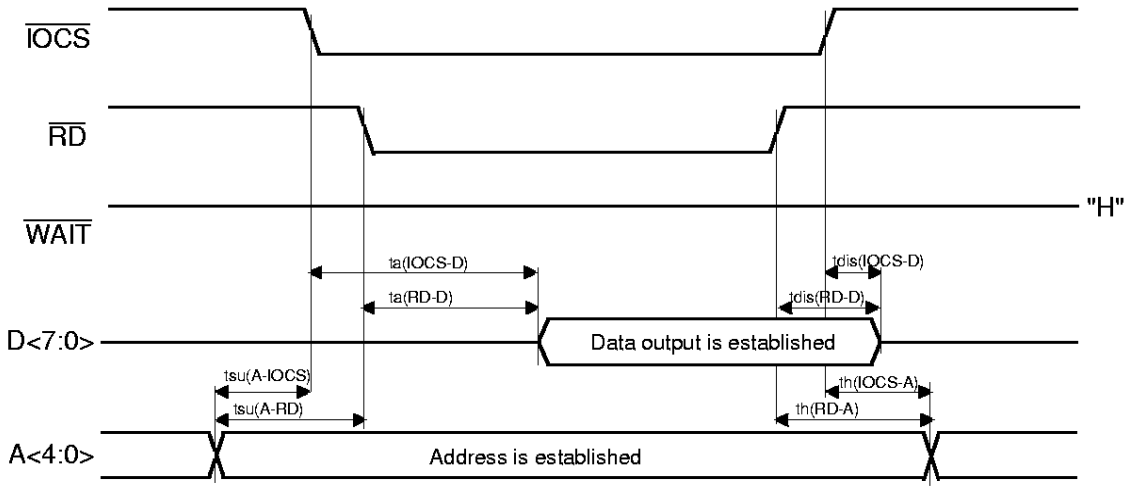
(1) Write to control register ($\overline{RD}$ = "H")

Without WAIT



(2) Read from control register ($\overline{LWR}$= "H")

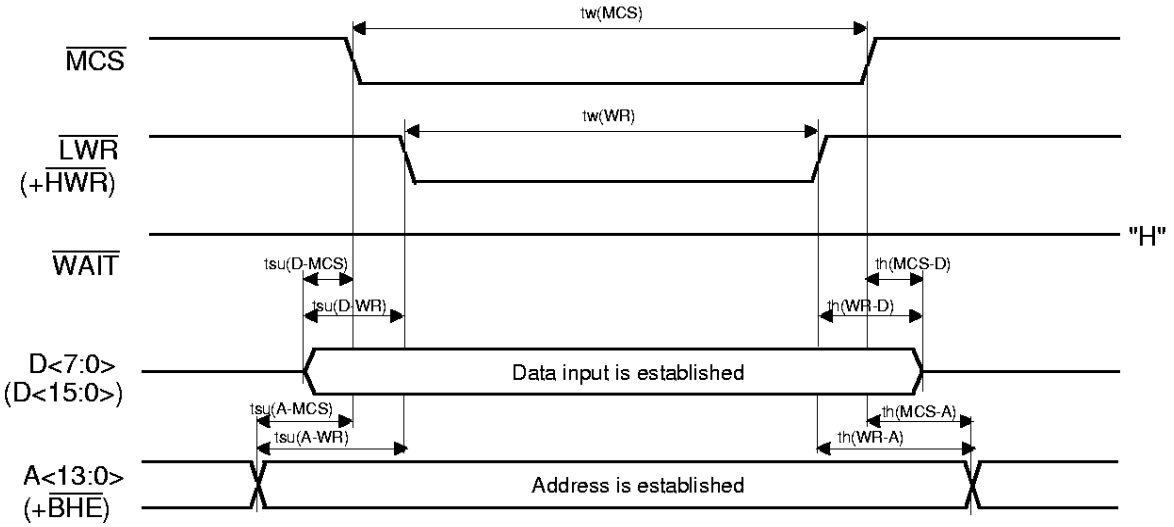
Without WAIT



Note 1: Writing/Reading operation for the control register is performed during overlapping $\overline{IOCS}$ and ($\overline{LWR}$ or $\overline{RD}$).
Limits of $\overline{IOCS}$,$\overline{LWR}$ and $\overline{RD}$ are prescribed by the input signal of last change to "L" in starting access,
and by the input signal of first change to "H" in ending access.

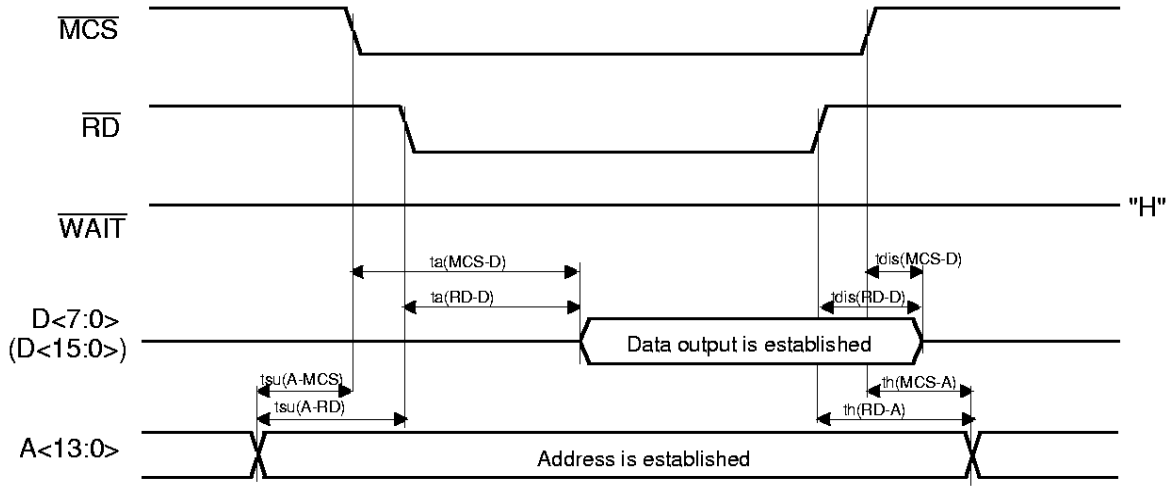
(3) Write to VRAM ($\overline{RD}$ = "H")

Term of non cycle steal access



(4) Read from VRAM ($\overline{LWR}$,$\overline{HWR}$ = "H")

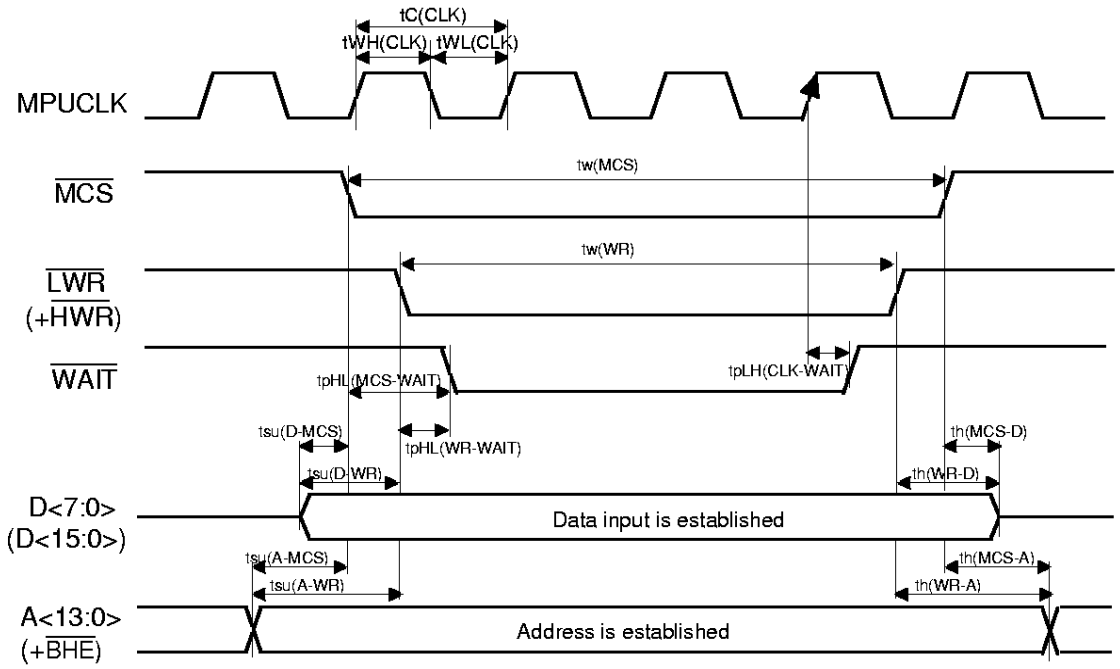
Term of non cycle steal access



Note 2: Writing/Reading operation for VRAM during non cycle steal access is performed during overlapping $\overline{MCS}$ and [$\overline{LWR}$(+$\overline{HWR}$) or $\overline{RD}$].
Limits of $\overline{MCS}$,$\overline{LWR}$(+$\overline{HWR}$) and $\overline{RD}$ are prescribed by the input signal of last change to "L" in starting access, and by the input signal of first change to "H" in ending access.

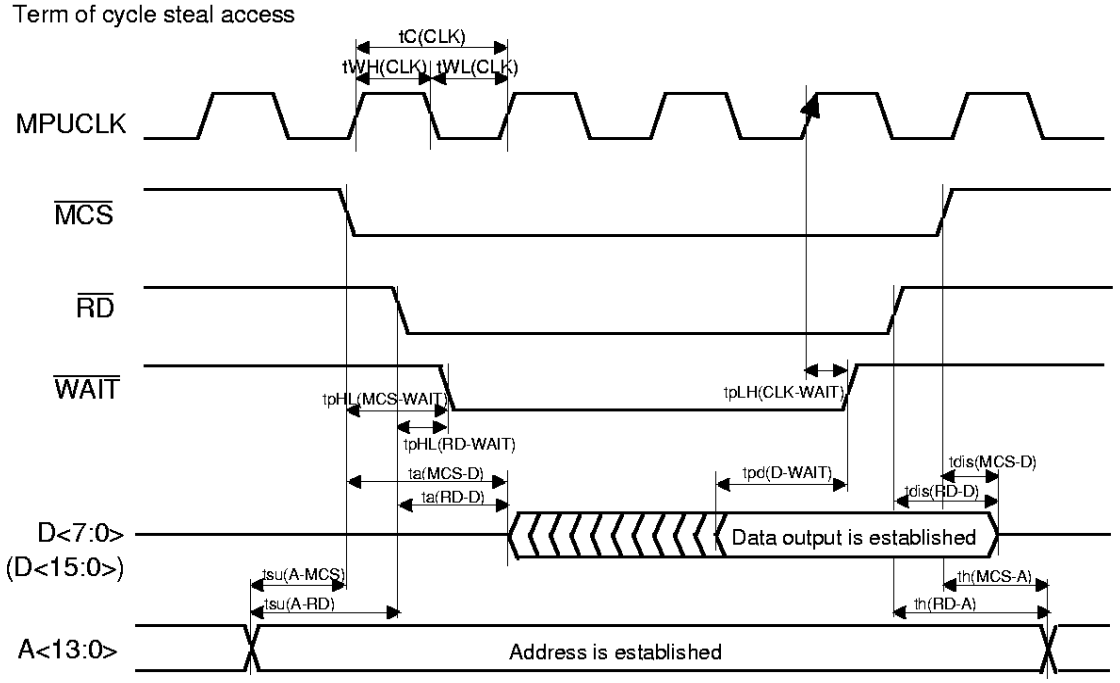
(5) Write to VRAM ($\overline{RD}$ = "H")

Term of cycle steal access



(6) Read from VRAM ($\overline{LWR}$,$\overline{HWR}$ = "H")

Term of cycle steal access



Note 3: Reading/writing operation for VRAM during cycle steal needs 1tc(Internal) in best case or 3tc(Internal) in worst case,according to the condition of the internal cycle steal at starting access requested from MPU.
tc(Internal) = Clock cycle time after setting division of OSC1.
Data output D in reading is established before changing $\overline{WAIT}$ to "H".

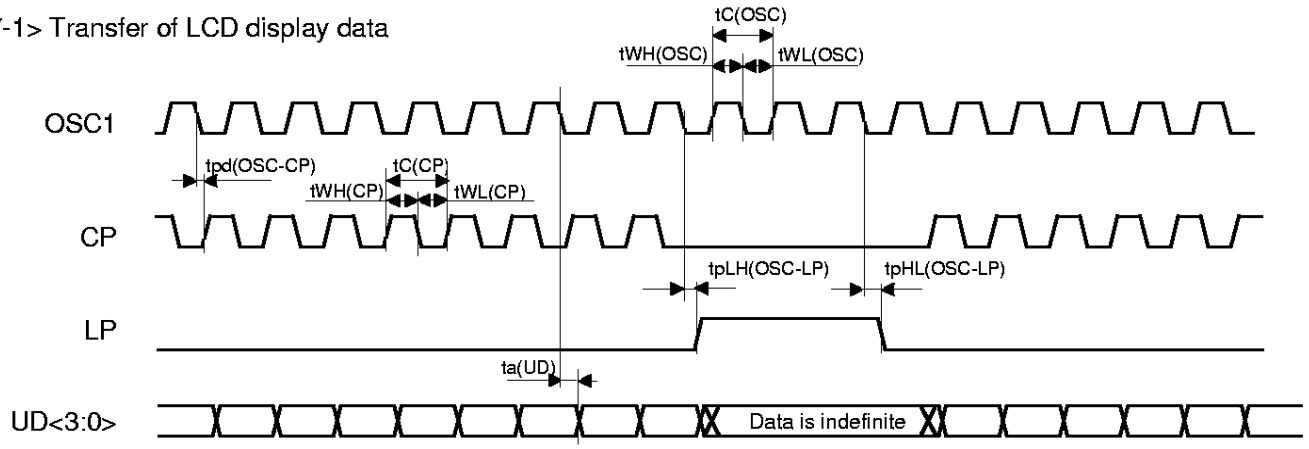
4: Limits of $\overline{MCS}$,$\overline{LWR}$(+$\overline{HWR}$) and $\overline{RD}$ are prescribed by the input signal of last change to "L" in starting access, and by the input signal of first change to "H" in ending access.

5: Always once return $\overline{MCS}$,$\overline{LWR}$(+$\overline{HWR}$) or $\overline{RD}$ to "H" after canceling $\overline{WAIT}$ output.
In case of latching "L",as don't output next $\overline{WAIT}$,this is cause of error action.

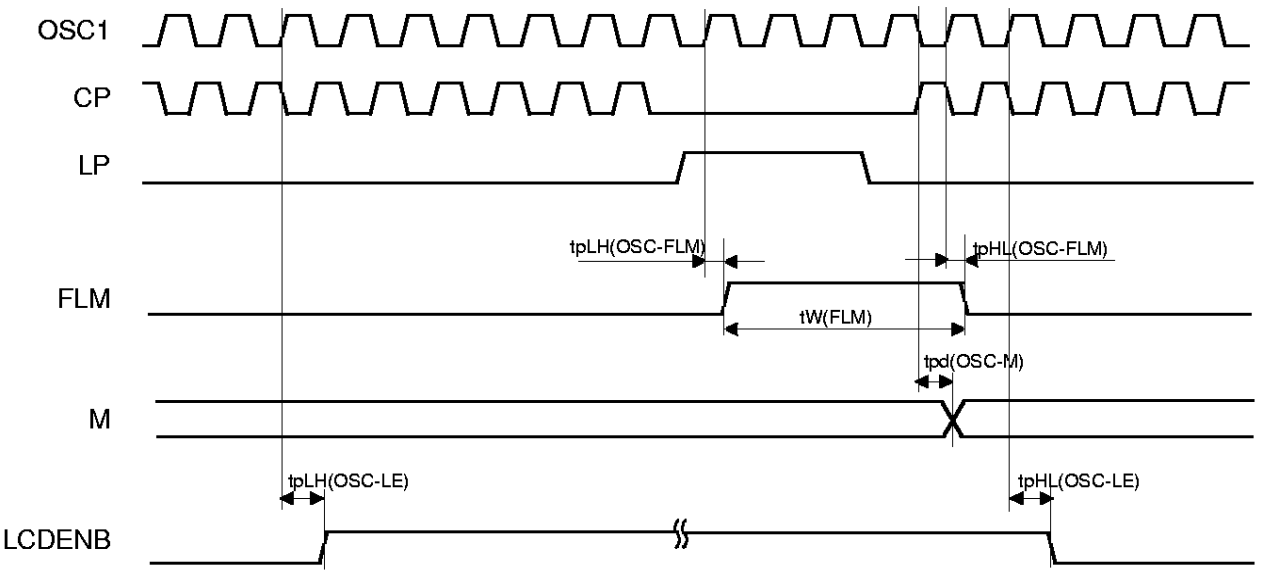
(7) Interface timing with LCD (OSCC = 1 division : set)

* When OSCC = 1 division ,OSC clock for internal operation = OSC1 input.

<7-1> Transfer of LCD display data



<7-2> LCD control signal



Note 6: Output signal to LCD side is syncronized with OSC clock for internal operation.
When division is set to 1/2 – 1/16 by OSCC register, switching characteristics is defined by rising edge of OSC1.