National Semiconductor

ADVANCE INFORMATION

74ABT162245
16-Bit Transceiver with TRI-STATE® Outputs

General Description

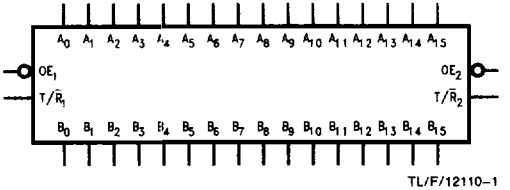
The 'ABT162245 contains sixteen non-inverting bidirectional buffers with TRI-STATE outputs and is intended for bus oriented applications. The device is byte controlled. Each byte has separate control inputs which can be shorted together for full 16-bit operation. The $T/\overline{R}$ inputs determine the direction of data flow through the device. The $\overline{OE}$ inputs disable both the A and B ports by placing them in a high impedance state.

The 25Ω series resistors in the outputs reduce ringing and eliminate the need for external resistors.

Features

- Bidirectional non-inverting buffers
- Separate control logic for each byte
- 16-bit version of the 'ABT2245
- A and B output sink capability of 64 mA, source capability of 32 mA
- Guaranteed output skew
- Guaranteed latchup protection
- High impedance glitch free bus loading during entire power up and power down cycle
- Non-destructive hot insertion capability

Logic Symbol



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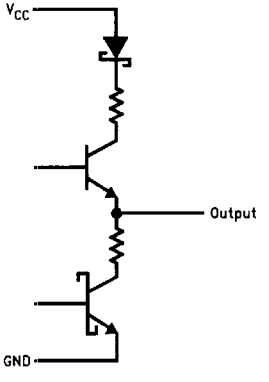
Pin Description

Pin Names	Description
$\overline{OE}_n$	Output Enable Input (Active Low)
$T/\overline{R}_n$	Transmit/Receive Input
A_0–A_{15}	Side A Inputs/Outputs
B_0–B_{15}	Side B Inputs/Outputs

Schematic of Each Output



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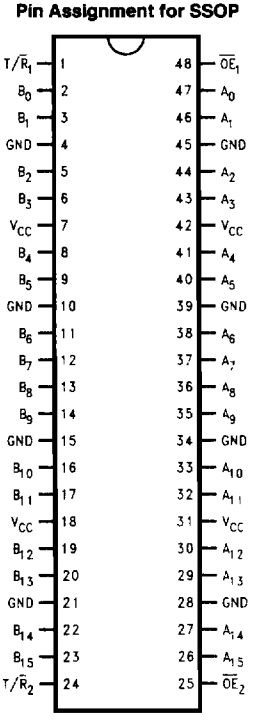
Connection Diagram

Pin Assignment for SSOP



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Functional Description

The 'ABT162245 contains sixteen non-inverting bidirectional buffers with TRI-STATE outputs. The device is byte controlled with each byte functioning identically, but independent of the other. The control pins can be shorted together to obtain full 16-bit operation.

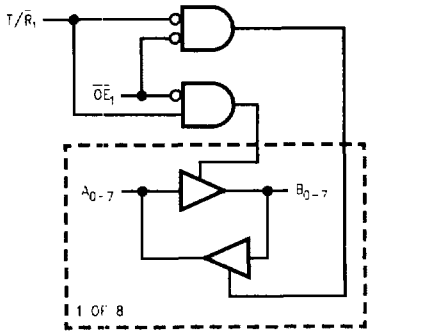
Truth Tables

Inputs		Outputs
$\overline{OE}_1$	$T/\overline{R}_1$	
L	L	Bus B_0–B_7 Data to Bus A_0–A_7
L	H	Bus A_0–A_7 Data to Bus B_0–B_7
H	X	HIGH-Z State on A_0–A_7, B_0–B_7

Inputs		Outputs
$\overline{OE}_2$	$T/\overline{R}_2$	
L	L	Bus B_8–B_{15} Data to Bus A_8–A_{15}
L	H	Bus A_8–A_{15} Data to Bus B_8–B_{15}
H	X	HIGH-Z State on A_8–A_{15}, B_8–B_{15}

H = High Voltage Level
L = Low Voltage Level
X = Immaterial
Z = High Impedance

Logic Diagrams



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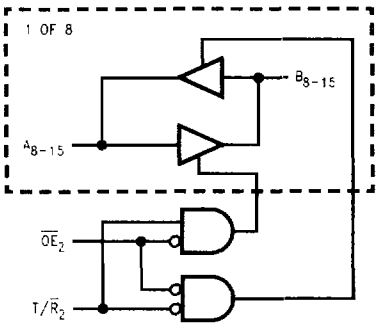

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