TOSHIBA MOS MEMORY PRODUCTS

262,144 WORD×1 BIT DYNAMIC RAM
SILICON MONOLITHIC
N-CHANNEL SILICON GATE MOS

TMM41257AP/AT/AZ-10, TMM41257AP/AT/AZ-12 TMM41257AP/AT/AZ-15

DESCRIPTION

The TMM41257AP/AT/AZ is the N-channel dynamic RAM organized 262,144 words by 1 bit. Multiplexed address inputs permit the TMM41257AP/AT/AZ to be packaged in a standard 16 pin plastic DIP, 18 pin PLCC and 16 pin ZIP. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. The double layered MOS technology with polycide and poly Si permits the TMM41257AP/AT/AZ high speed operation. Also, the advanced circuit techniques have realized low power dissipation. System oriented features include single power supply of 5V ± 10% tolerance, direct interfacing capacibility with high performance logic families such as schottky TTL. In addition to the $\overline{RAS}$ only refresh mode, a $\overline{CAS}$ before $\overline{RAS}$ automatic refresh is available. Another special feature of TMM41257AP/AT/AZ is nibble mode, allowing the user to serially access 4 bits of data at a high data rate.

FEATURES

- 262,144 words by 1 bit organization
- Fast access time and cycle time

	TMM41257AP/AT/AZ-10/-12/-15
$\overline{RAS}$ Access Time	100ns/120ns/150ns
$\overline{CAS}$ Access Time	50ns/ 60ns/ 75ns
Cycle Time	190ns/220ns/260ns
Nibble Mode Access Time	25ns/ 30ns/ 40ns
Nibble Mode Cycle Time	50ns/ 60ns/ 70ns

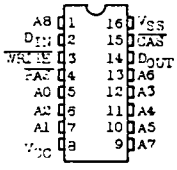
- Single power supply of 5V ± 10% with a built-in V_{BB} generator
- Low Power:
  440mW MAX. Operating (TMM41257AP/AT/AZ-10)
  396mW MAX. Operating (TMM41257AP/AT/AZ-12)
  358mW MAX. Operating (TMM41257AP/AT/AZ-15)
  28mW MAX. Standby

Output unlatched at cycle end allows two-dimensional chip selection
Common I/O capability using "EARLY WRITE" operation
Read-Modify-Write, $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, Hidden refresh, and Nibble Mode capability
All inputs and output TTL compatible
256 refresh cycles/4ms
Package

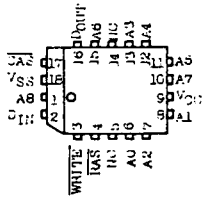
Plastic DIP	: TMM41257AP
Plastic Leaded Chip Carrier	: TMM41257AT
Plastic ZIP	: TMM41257AZ

PIN CONNECTION (TOP VIEW)

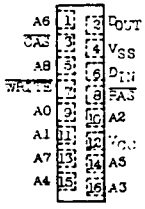
TMM41257AP



TMM41257AT



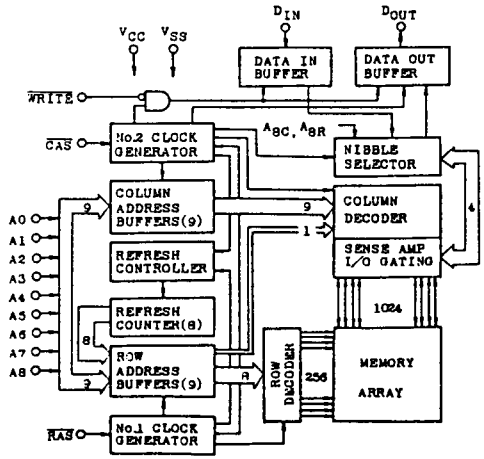
TMM41257AZ



PIN NAMES

A0 ~ A8	Address Inputs
$\overline{CAS}$	Column Address Strobe
D_{IN}	Data In
D_{OUT}	Data Out
$\overline{RAS}$	Row Address Strobe
$\overline{WRITE}$	Read/Write Input
V_{CC}	Power (+5V)
V_{SS}	Ground

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNITS	NOTES
Input and Output Voltage	V_{IN}, V_{OUT}	−1 ~ 7	V	1
Power Supply Voltage	V_{CC}	−1 ~ 7	V	1
Operating Temperature	T_{OPR}	0 ~ 70	°C	1
Storage Temperature	T_{STG}	−55 ~ 150	°C	1
Soldering Temperature • Time	T_{SOLDER}	260 • 10	°C • sec	1
Power Dissipation	P_D	600	mW	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (T_a = 0 ~ 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	–	6.5	V	2
V_{IL}	Input Low Voltage	−1	–	0.8	V	2

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, T_a = 0 ~ 70°C)

SYMBOL	PARAMETER		MIN.	MAX.	UNITS	NOTES
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$ Cycling: t_{RC} = t_{RC} MIN.)	TMM41257AP/AT/AZ-10	–	80	mA	3, 4
		TMM41257AP/AT/AZ-12	–	72		
		TMM41257AP/AT/AZ-15	–	65		
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		–	5	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, RAS Only Refresh Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: t_{RC} = t_{RC} MIN.)	TMM41257AP/AT/AZ-10	–	70	mA	3
		TMM41257AP/AT/AZ-12	–	62		
		TMM41257AP/AT/AZ-15	–	55		
I_{CC4}	NIBBLE MODE CURRENT Average Power Supply Current, Nibble Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ Cycling: t_{NC} = t_{NC} MIN.)	TMM41257AP/AT/AZ-10	–	50	mA	3, 4
		TMM41257AP/AT/AZ-12	–	48		
		TMM41257AP/AT/AZ-15	–	45		
I_{CC5}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Refresh Mode ($\overline{RAS}$, $\overline{CAS}$ Cycling, $\overline{CAS}$ Before $\overline{RAS}$: t_{RC} = t_{RC} MIN.)	TMM41257AP/AT/AZ-10	–	70	mA	3
		TMM41257AP/AT/AZ-12	–	62		
		TMM41257AP/AT/AZ-15	–	55		
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any input (0V ≤ V_{IN} ≤ 6.5V, All Other Pins Not Under Test = 0V)		−10	10	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, 0V ≤ V_{OUT} ≤ +5.5V)		−10	10	μA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT} = −5mA)		2.4	–	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT} = 4.2mA)		–	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC} = 5V ± 10%, Ta = 0 ~ 70°C) (Notes 5, 6, 7)

SYMBOL	PARAMETER	TMM41257AP/AT/AZ-10		TMM41257AP/AT/AZ-12		TMM41257AP/AT/AZ-15		UNITS	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	190	–	220	–	260	–	ns	
t_{RWC}	Read-Write Cycle Time	200	–	240	–	285	–	ns	
t_{RMW}	Read-Modify-Write Cycle Time	220	–	260	–	310	–	ns	
t_{NC}	Nibble Mode Cycle Time	50	–	60	–	70	–	ns	
t_{NRWC}	Nibble Mode Read-Write/Read-Modify Write Cycle Time	75	–	90	–	105	–	ns	
t_{RAC}	Access Time from $\overline{RAS}$	–	100	–	120	–	150	ns	8, 10
t_{CAC}	Access Time from $\overline{CAS}$	–	50	–	60	–	75	ns	9, 10
t_{NCAC}	Nibble Mode Access Time	–	25	–	30	–	40	ns	10
t_{OFF}	Output Buffer Turn-Off Delay	5	25	5	30	5	35	ns	11
t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	7
t_{RP}	$\overline{RAS}$ Precharge Time	80	–	90	–	100	–	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	100	10,000	120	10,000	150	10,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	50	–	60	–	75	–	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	100	–	120	–	150	–	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	50	10,000	60	10,000	75	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	25	50	25	60	25	75	ns	13
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	10	–	10	–	10	–	ns	
t_{CPN}	$\overline{CAS}$ Precharge Time	15	–	20	–	25	–	ns	
t_{ASR}	Row Address Set-Up Time	0	–	0	–	0	–	ns	
t_{RAH}	Row Address Hold Time	15	–	15	–	15	–	ns	
t_{ASC}	Column Address Set-Up Time	0	–	0	–	0	–	ns	
t_{CAH}	Column Address Hold Time	20	–	25	–	30	–	ns	
t_{AR}	Column Address Hold Time Reference to $\overline{RAS}$	70	–	85	–	105	–	ns	
t_{RCS}	Read Command Set-Up Time	0	–	0	–	0	–	ns	
t_{RCH}	Read Command Hold Time Reference to $\overline{CAS}$	0	–	0	–	0	–	ns	12
t_{RRH}	Read Command Hold Time Reference to $\overline{RAS}$	10	–	15	–	20	–	ns	12
t_{WCH}	Write Command Hold Time	20	–	25	–	30	–	ns	
t_{WCR}	Write Command Hold Time Reference to $\overline{RAS}$	70	–	85	–	105	–	ns	
t_{WP}	Write Command Pulse Width	20	–	25	–	30	–	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	25	–	35	–	45	–	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	25	–	35	–	45	–	ns	
t_{DS}	Data-In Set-Up Time	0	–	0	–	0	–	ns	14
t_{DH}	Data-In Hold Time	20	–	25	–	30	–	ns	14
t_{DHR}	Data-In Hold Time Reference to $\overline{RAS}$	70	–	85	–	105	–	ns	
t_{REF}	Refresh Period	–	4	–	4	–	4	ms	
t_{WCS}	Write Command Set-Up Time	0	–	0	–	0	–	ns	15
t_{CWD}	$\overline{CAS}$ to $\overline{WRITE}$ Delay Time	30	–	40	–	50	–	ns	15

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Continued)

SYMBOL	PARAMETER	TMM41257AP/AT/AZ-10		TMM41257AP/AT/AZ-12		TMM41257AP/AT/AZ-15		UNITS	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ Delay Time	80	–	100	–	125	–	ns	15
t_{NCAS}	Nibble Mode $\overline{CAS}$ Pulse Width	25	–	30	–	40	–	ns	
t_{NCP}	Nibble Mode $\overline{CAS}$ Precharge Time	15	–	20	–	20	–	ns	
t_{NRRSH}	Nibble Mode $\overline{RAS}$ Hold Time (Read)	20	–	25	–	30	–	ns	
t_{NWRSH}	Nibble Mode $\overline{RAS}$ Hold Time (Write)	40	–	45	–	50	–	ns	
t_{NCWD}	Nibble Mode $\overline{CAS}$ to $\overline{WRITE}$ Delay Time	25	–	30	–	40	–	ns	
t_{NCWL}	Nibble Mode $\overline{WRITE}$ Command to $\overline{CAS}$ Lead Time	20	–	25	–	30	–	ns	
t_{CSR}	$\overline{CAS}$ Set-Up Time ($\overline{CAS}$ before $\overline{RAS}$)	10	–	10	–	10	–	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$)	30	–	30	–	30	–	ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Active Time	0	–	0	–	0	–	ns	
t_{CPT}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Counter Test)	40	–	50	–	60	–	ns	

CAPACITANCE (V_{CC} = 5V ± 10%, f = 1MHz, Ta = 0 ~ 70°C)

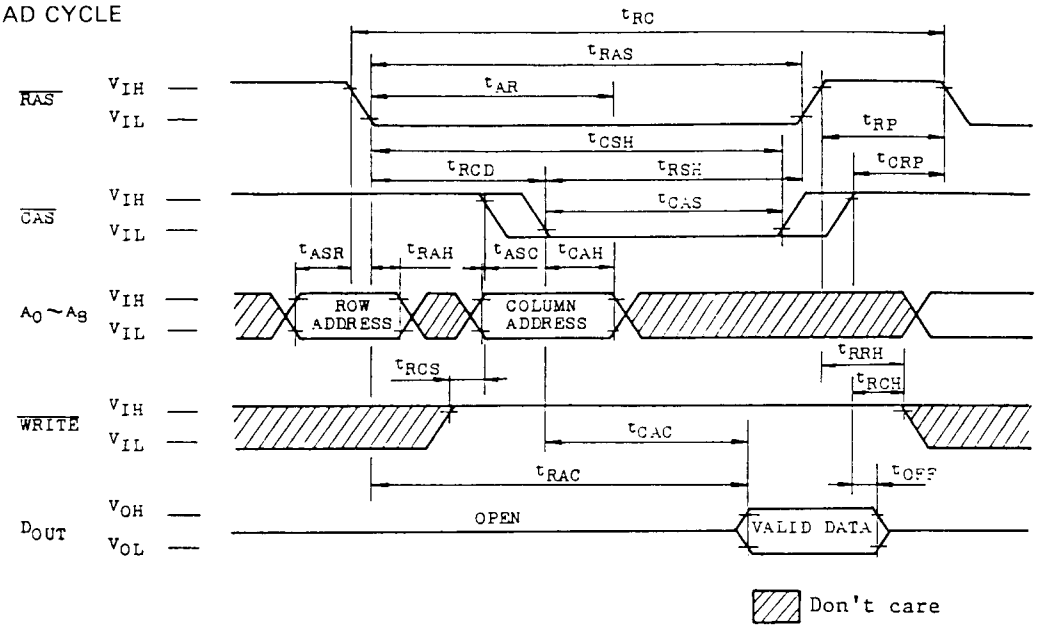
SYMBOL	PARAMETER	MIN.	MAX.	UNITS
C_{I1}	Input Capacitance ($A_0 \sim A_8$, D_{IN})	–	5	pF
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$)	–	7	pF
C_O	Output Capacitance (D_{OUT})	–	7	pF

NOTES:

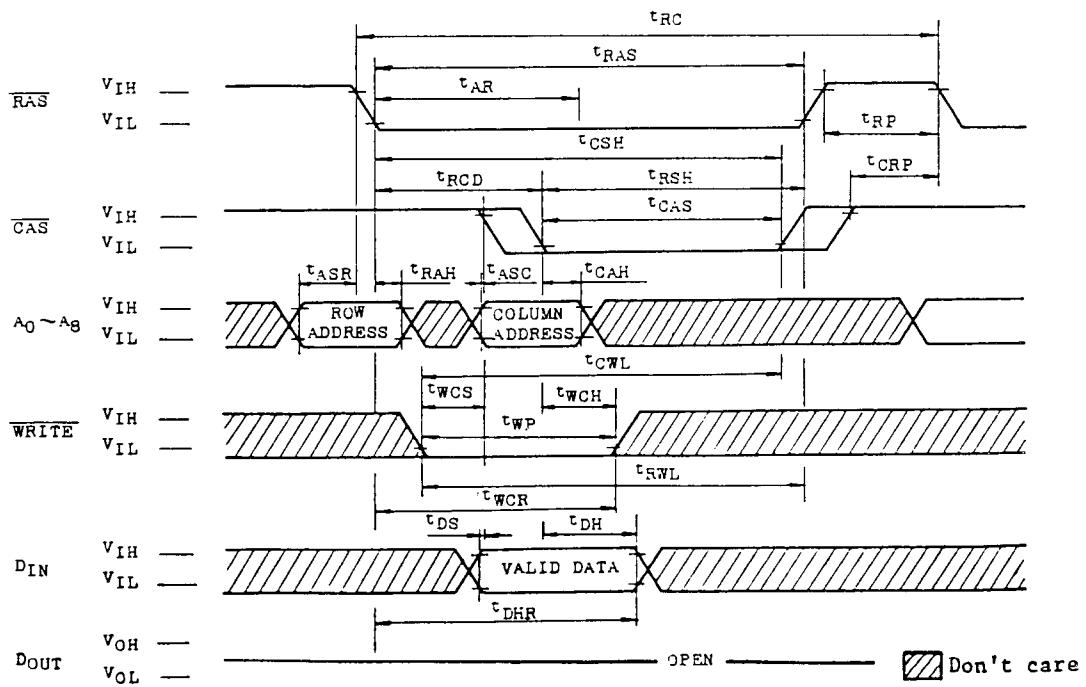
1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltages are referenced to V_{SS}.
3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC5} depend on cycle rate.
4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
5. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ Before $\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
6. AC measurements assume t_T = 5 ns.
7. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Assumes that $t_{RCD} \leq t_{RCD}$ (max.). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
9. Assumes that $t_{RCD} \geq t_{RCD}$ (max.)
10. Measured with a load equivalent to 2 TTL loads and 100 pF.
11. t_{OFF} (max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
12. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
13. Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RAC} (max.) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled exclusively by t_{CAC}.
14. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in read-write or read-modify-write cycles.
15. t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (min.), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; If $t_{CWD} \geq t_{CWD}$ (min.) and $t_{RWD} \geq t_{RWD}$ (min.), the cycle is a read-write cycle or read-modify-write cycle and the data out will contain data read from the selected cell: If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

TIMING WAVEFORMS

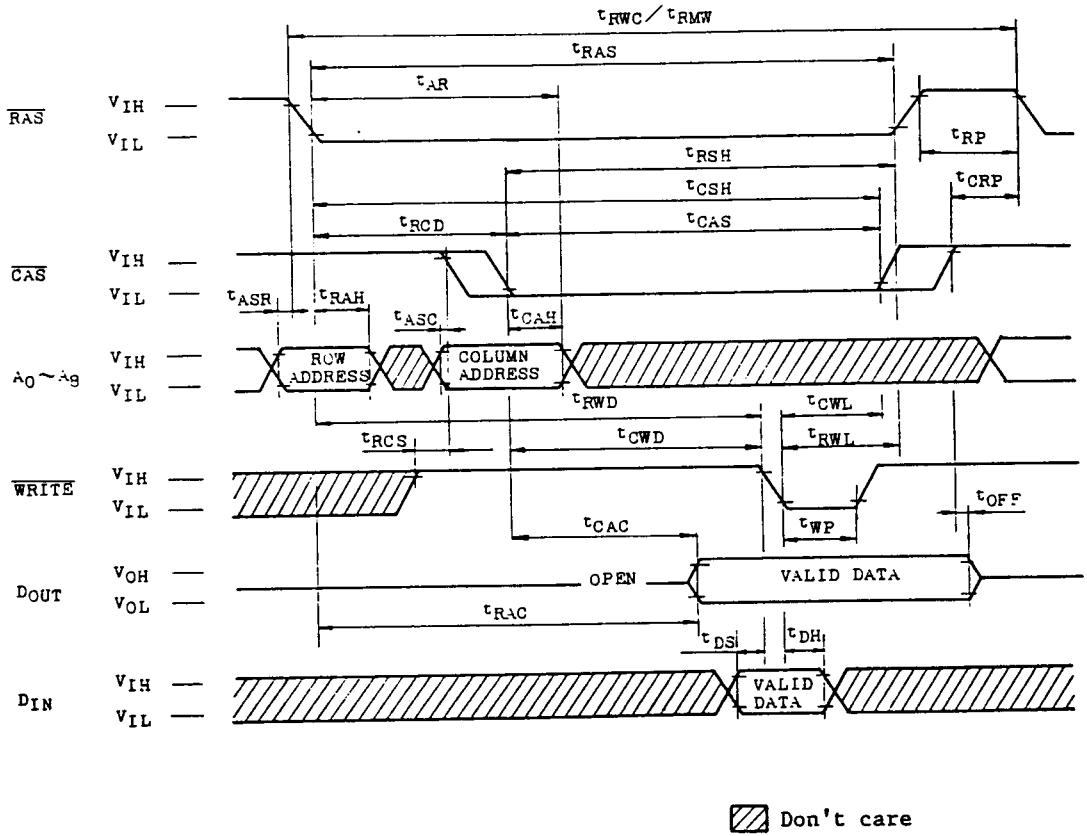
- READ CYCLE



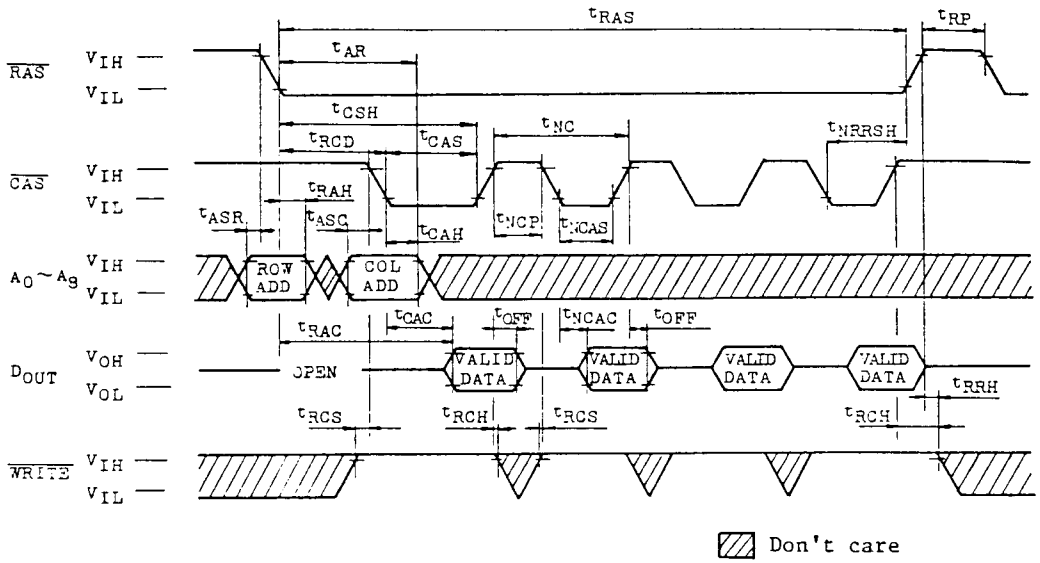
- WRITE CYCLE (EARLY WRITE)



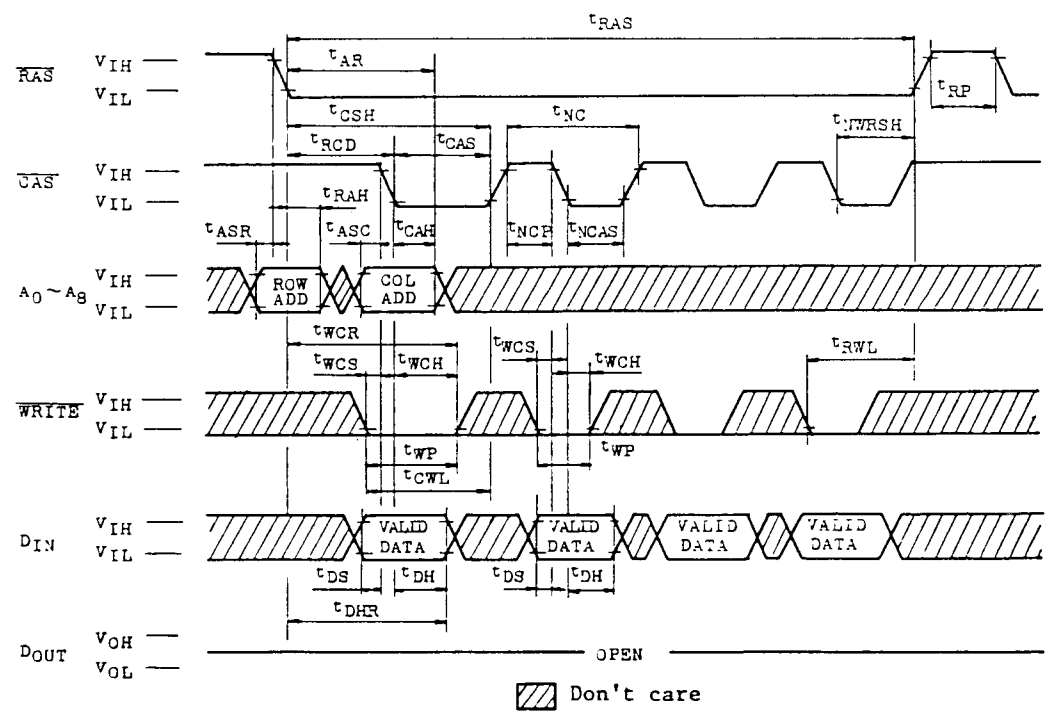
- READ-WRITE/READ-MODIFY-WRITE CYCLE



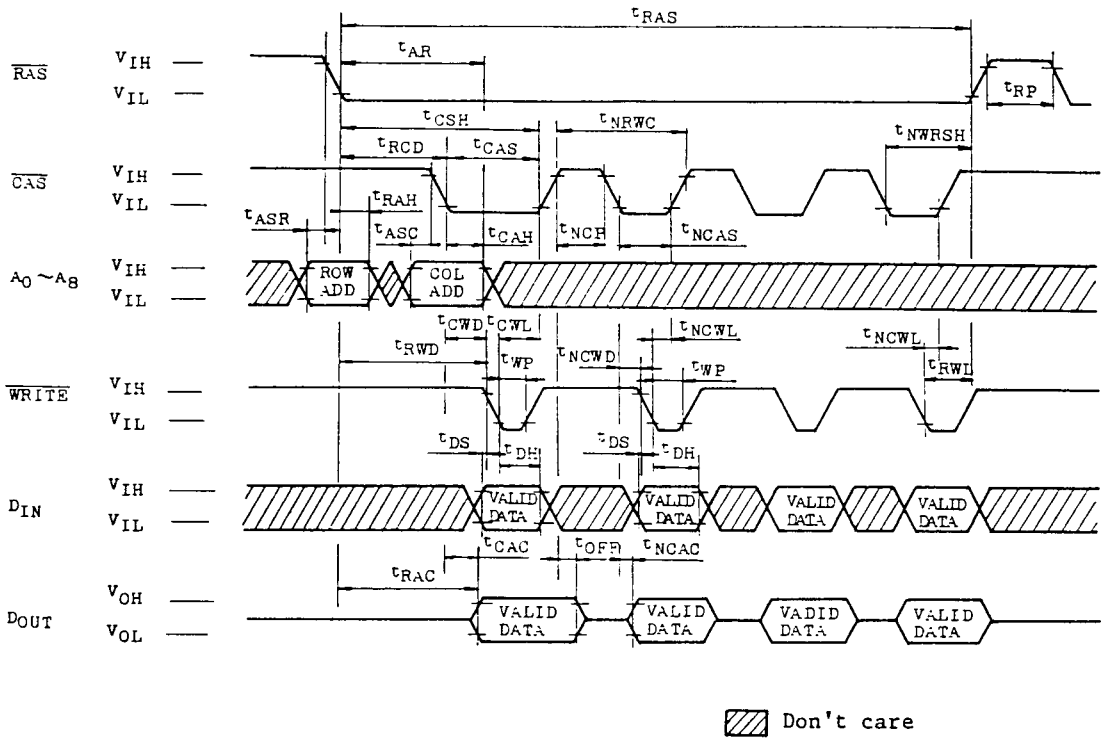
- NIBBLE MODE READ CYCLE



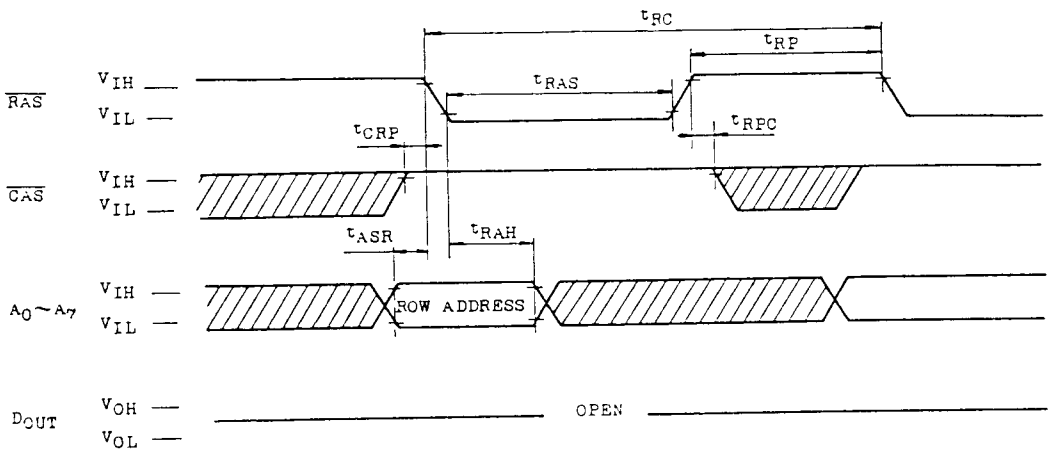
- NIBBLE MODE WRITE CYCLE (EARLY WRITE)



- NIBBLE MODE READ-WRITE/READ-MODIFY-WRITE CYCLE



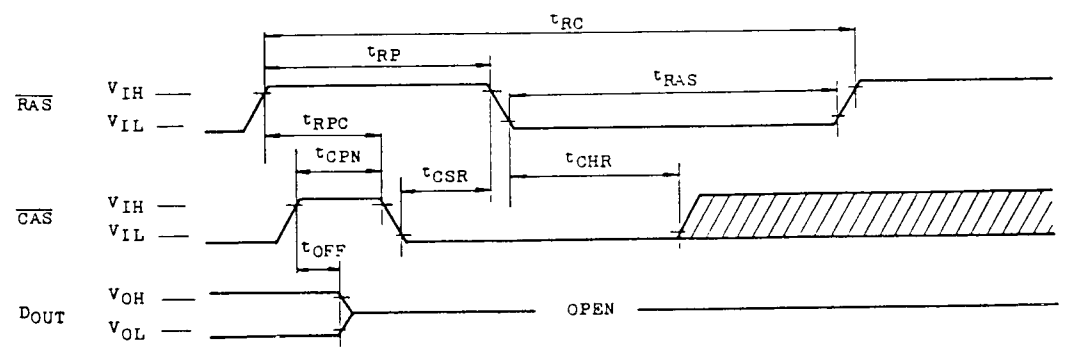
- $\overline{RAS}$ ONLY REFRESH CYCLE



Note: $\overline{WRITE}$=Don't care, A8=Don't care

Don't care

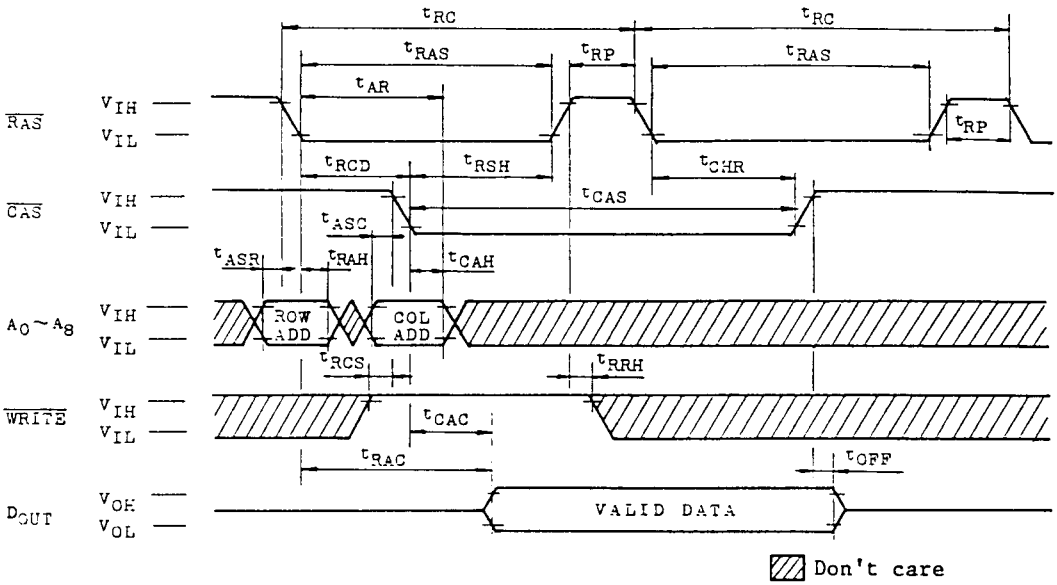
- $\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



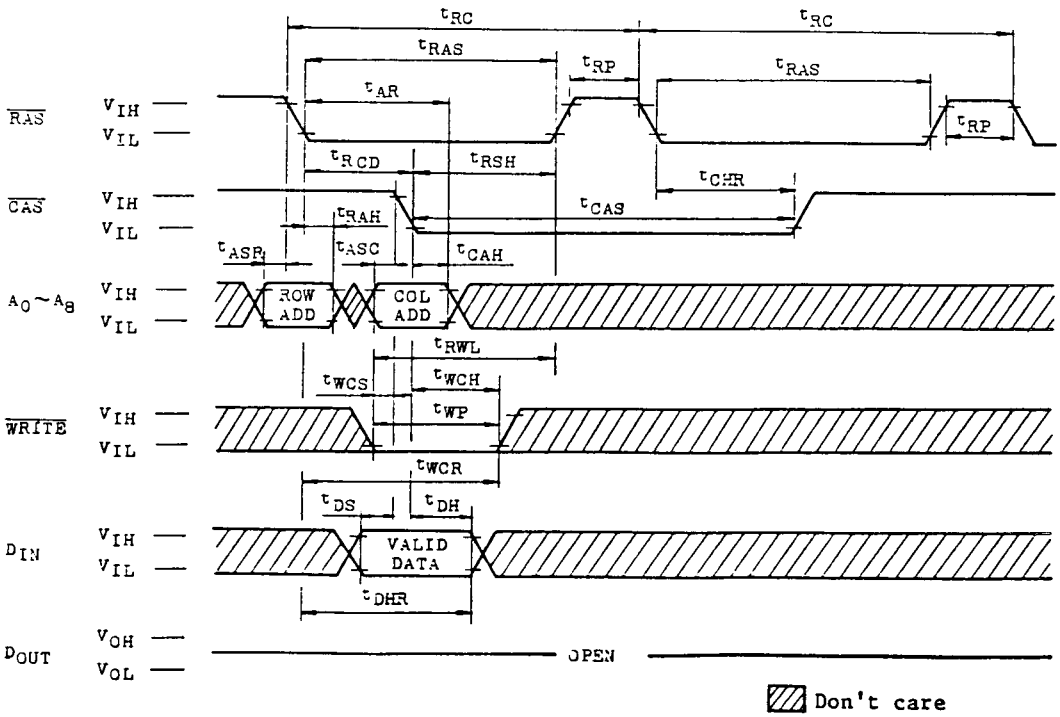
Note: $\overline{WRITE}$=Don't care, A0 ∿ A8=Don't care

Don't care

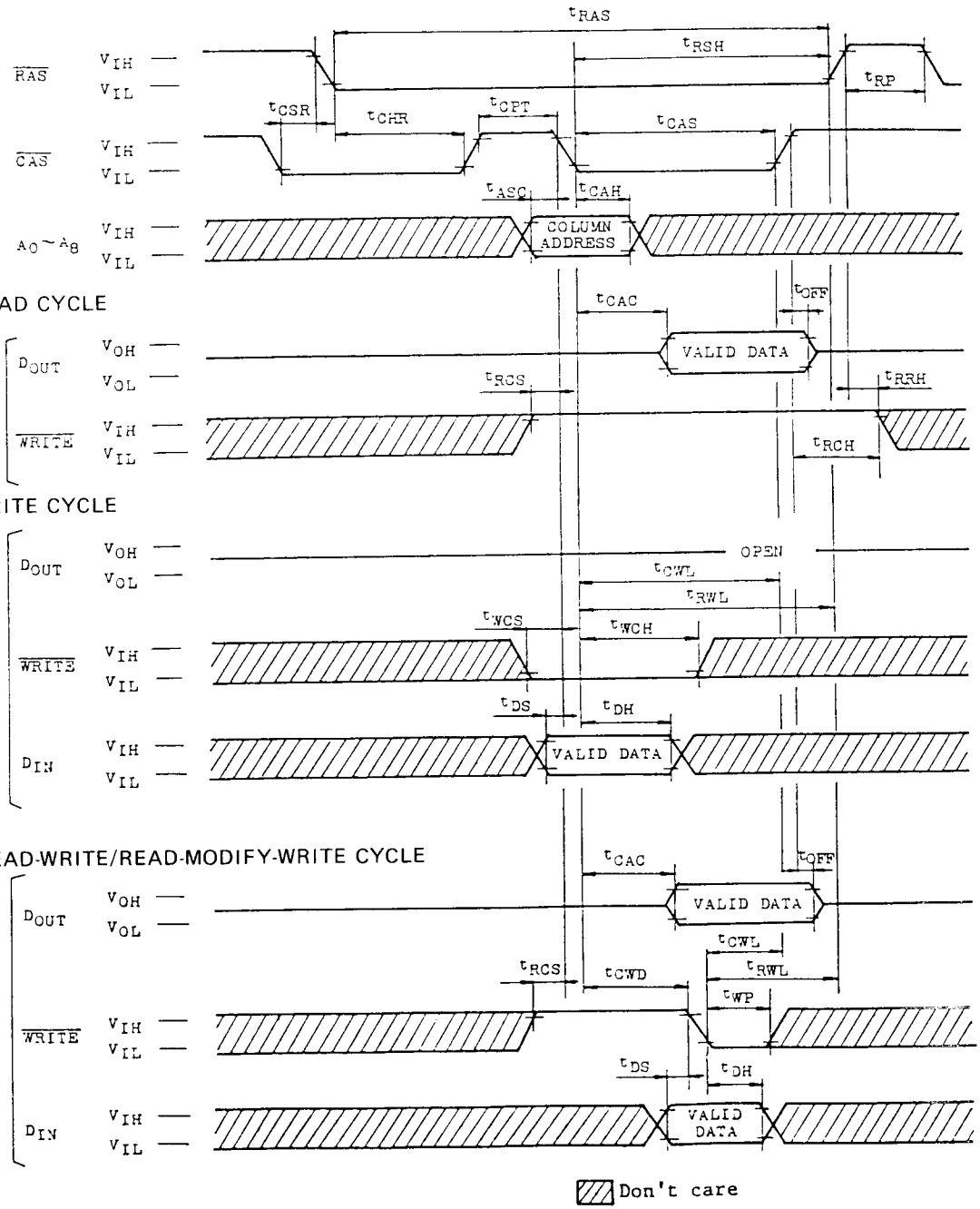
- HIDDEN REFRESH CYCLE (READ)



- HIDDEN REFRESH CYCLE (WRITE)



- $\overline{CAS}$ BEFORE RAS REFRESH COUNTER TEST CYCLE



- READ CYCLE
- WRITE CYCLE
- READ-WRITE/READ-MODIFY-WRITE CYCLE

APPLICATION INFORMATION

ADDRESSING

The 18 address bits required to decode 1 of the 262,144 cell locations within the TMM41257AP/AT/AZ are multiplexed onto the 9 address inputs and latched into the on-chip address latches by externally applying two negative going TTL-level clocks.

The first clock, the Row Address Strobe ($\overline{RAS}$), latches the 9 row address bits into the chip. The second clock, the Column Address Strobe ($\overline{CAS}$), subsequently latches the 9 column address bits into the chip. Each of these signals, $\overline{RAS}$, and $\overline{CAS}$, triggers a sequence of events which are controlled by different delayed internal clocks.

The two clock chains are linked together logically in such a way that the address multiplexing operation is done outside of the critical path timing sequence for read data access. The later events in the $\overline{CAS}$ clock sequence are inhibited until the occurrence of a delayed signal derived from the $\overline{RAS}$ clock chain. This "gated $\overline{CAS}$" feature allows the $\overline{CAS}$ clock to be externally activated as soon as the Row address Hold Time specification (t_{RAH}) has been satisfied and the address inputs have been changed from Row address to Column address information.

DATA INPUT/OUTPUT

Data to be written into a selected cell is latched into an on-chip register by a combination of $\overline{WRITE}$ and $\overline{CAS}$ while $\overline{RAS}$ is active. The later of the signals ($\overline{WRITE}$ or $\overline{CAS}$) to make its negative transition is the strobe for the Data In (D_{IN}) register. This permits several options in the write cycle timing. In a write cycle, if the $\overline{WRITE}$ input is brought low (active) prior to $\overline{CAS}$, the D_{IN} is strobed by $\overline{CAS}$ and the set-up and hold times are referenced to $\overline{CAS}$. If the input data is not available at $\overline{CAS}$ time or if it is desired that the cycle be a read-write cycle, the $\overline{WRITE}$ signal will be delayed until after $\overline{CAS}$ has made its negative transition. In this "delayed write cycle" the data input set-up and hold times are referenced to the negative edge of $\overline{WRITE}$ rather than $\overline{CAS}$. (To illustrate this feature, D_{IN} is referenced to $\overline{WRITE}$ in the timing diagrams depicting the read-write and nibble mode write cycles while the "early write" cycle diagram shows D_{IN} referenced to $\overline{CAS}$).

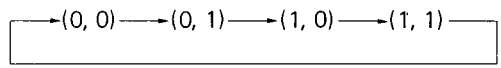
Data is retrieved from the memory in a read cycle by maintaining $\overline{WRITE}$ in the inactive or high state throughout the portion of the memory cycle in which $\overline{CAS}$ is active (low). Data read from the selected cell will be available at the output within the specified access time.

DATA OUTPUT CONTROL

The normal condition of the Data Output (D_{OUT}) of the TMM41257AP/AT/AZ is the high impedance (open circuit) state. This is to say, anytime CAS is at a high level, the D_{OUT} pin will be floating. The only time the output will turn on and contain either a logic 0 or logic 1 is at access time during a read cycle. D_{OUT} will remain valid from access time until $\overline{CAS}$ is taken back to the inactive (high level) condition.

NIBBLE MODE

Nibble mode operation allows faster successive data operation on 4 bits. The first of 4 bits is accessed in the usual manner with read data coming out at t_{CAC} time. By keeping $\overline{RAS}$ low, $\overline{CAS}$ can be cycled up and then down, to read or write the next three pages at high data rate (faster than t_{CAC}). Row and column addresses need only be supplied for the first access of the cycles. From then on, the falling edge of $\overline{CAS}$ will activate the next bit. After four bits have been accessed, the next bit will be the same as the first bit accessed (wrap-around) method).



Pin one (A_8) determines the starting point of the circular 4 bits nibble. Row A_8 and column A_8 provide the two binary bits needed to select one of four bits. From then on, successive bits come out in a binary fashion; 00 → 01 → 10 → 11 with A_8 row being the least significant address.

A nibble cycle can be a read, write, or late write cycle. Any combinations of reads and writes or late writes will be allowed. In addition, the circular wrap-around will continue for as long as $\overline{RAS}$ is kept low.

$\overline{RAS}$ ONLY REFRESH

Refresh of the dynamic cell matrix is accomplished by performing a memory cycle at each of the 256 row address ($A_0 \sim A_7$) within each 4 millisecond

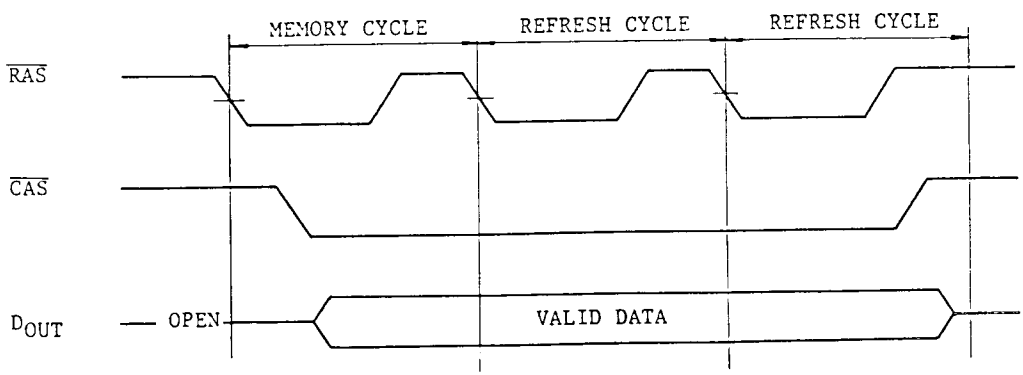
time interval. Although any normal memory cycle will perform the refresh operation, this function is most easily accomplished with "$\overline{RAS}$-only" cycles, $\overline{RAS}$ only refresh results in a substantial reduction in operating power. This reduction in power is reflected in the I_{CC3} specification.

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH

$\overline{CAS}$ before $\overline{RAS}$ refreshing available on the TMM41257AP/AT/AZ offers an alternate refresh method. If $\overline{CAS}$ is held on low for the specified period (t_{CSR}) before $\overline{RAS}$ goes to low, on chip refresh control clock generators and the refresh address counter are enabled, and an internal refresh operation takes place. After the refresh operation is performed, the refresh address counter is automatically incremented in preparation for the next $\overline{CAS}$ before $\overline{RAS}$ refresh operation.

HIDDEN REFRESH

An optional feature of the TMM41257AP/AT/AZ is that refresh cycles may be performed while maintaining valid data at the output pin. This is referred to as Hidden Refresh. Hidden Refresh is performed by holding $\overline{CAS}$ at V_{IL} and taking $\overline{RAS}$ high and after a specified precharge period (t_R), excuting a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle. (see Figure below)



This feature allows a refresh cycle to be "hidden" among data cycles without affecting the data availability.

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST

The internal refresh operation of TMM41257AP/AT/AZ can be tested by $\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST. This cycle performs READ/WRITE operation taking the internal counter address as row address and the input address as column address.

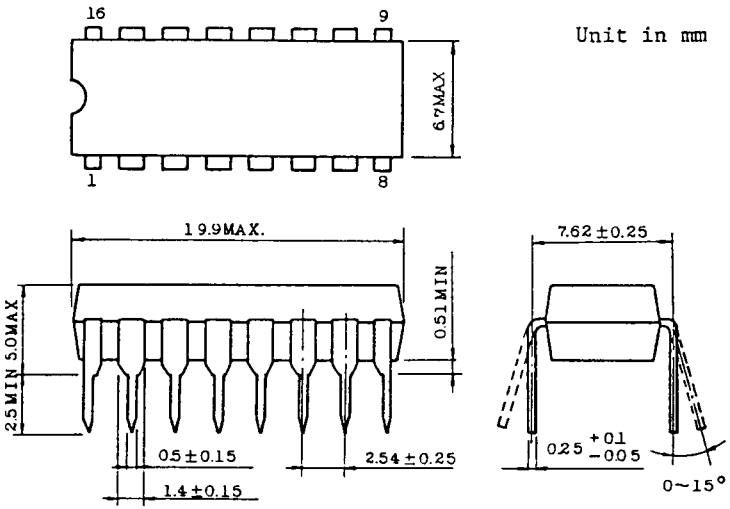
The test is performed after a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ cycles as initialization cycles. The test procedure is as follows.

① Write "0" into all the memory cells at normal write mode.
② Select one certain column address and read "0" out and write "1" in each cell by performing $\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST (READ-WRITE CYCLE). Repeat this operation 256 times.
③ Check "1" out of 256 bits at normal read mode, which was written at ②.
④ Using the same column as ②, read "1" out and write "0" in each cell performing $\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST.
Repeat this operation 256 times.
⑤ Check "0" out of 256 bits at normal read mode, which was written at ④.
⑥ Perform the above ① to ⑤ the complement data.

OUTLINE DRAWINGS

- Plastic DIP

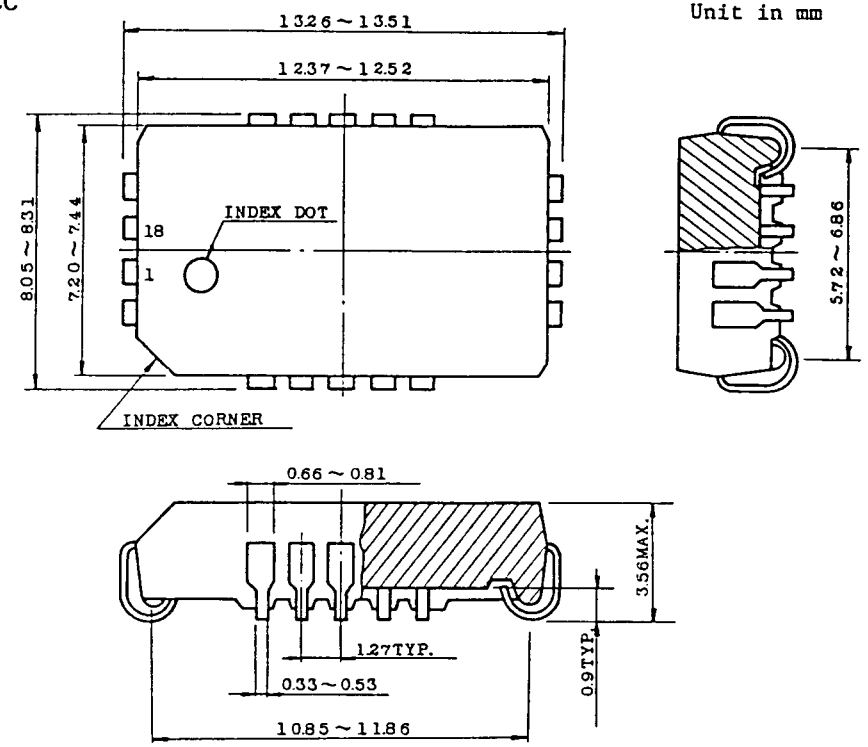
Unit in mm



Note: Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect to No. 1 and No. 16 leads. All dimensions are in millimeters.

- Plastic LCC

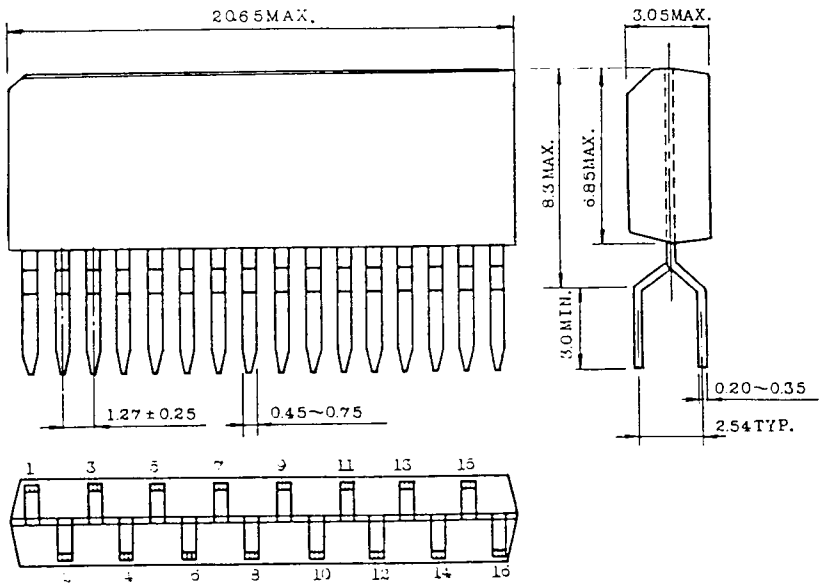
Unit in mm



Note: Each lead pitch is 1.27mm. All dimensions are in millimeters.

- Plastic ZIP

Unit in mm



Note: Each lead pitch is 1.27mm. All dimensions are in millimeters.

Note: Toshiba does not assume any responsibility for use of any circuitry described; no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.