

SP8797

225MHz ÷ 32/33 PRESCALER

The SP8797 is a low power programmable +32/33 counter which operates over the full military temperature range. It divides by 32 when the control input is in the high state and by 33 when in the low state.

FEATURES

- Very Low Power
- Control Input and Output CMOS and TTL Compatible
- AC Coupled Input
- Buffer Amp for Good Reverse Isolation
- Operation Up to 9.5V Using Internal Regulator

QUICK REFERENCE DATA

- Supply voltage: 4.5V to 9.5V
- Power consumption 65mW at $V_{CC} = 9.5V$
- Temperature range: $-55^{\circ}C$ to $+125^{\circ}C$

ORDERING INFORMATION

SP8797 A DG

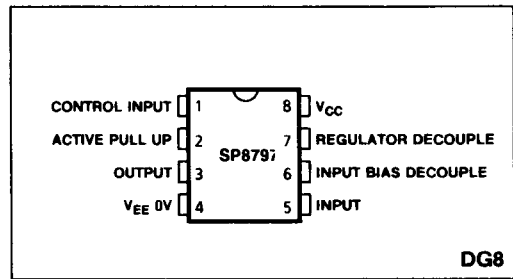


Fig 1 Pin Connections - top view

ABSOLUTE MAXIMUM RATINGS

Supply voltage pin 7	6.5V
Clock input voltage	2.5V p-p
Storage temperature range	$-55^{\circ}C$ to $+150^{\circ}C$
Junction temperature	$+175^{\circ}C$
Supply Voltage pin 8	13.5V

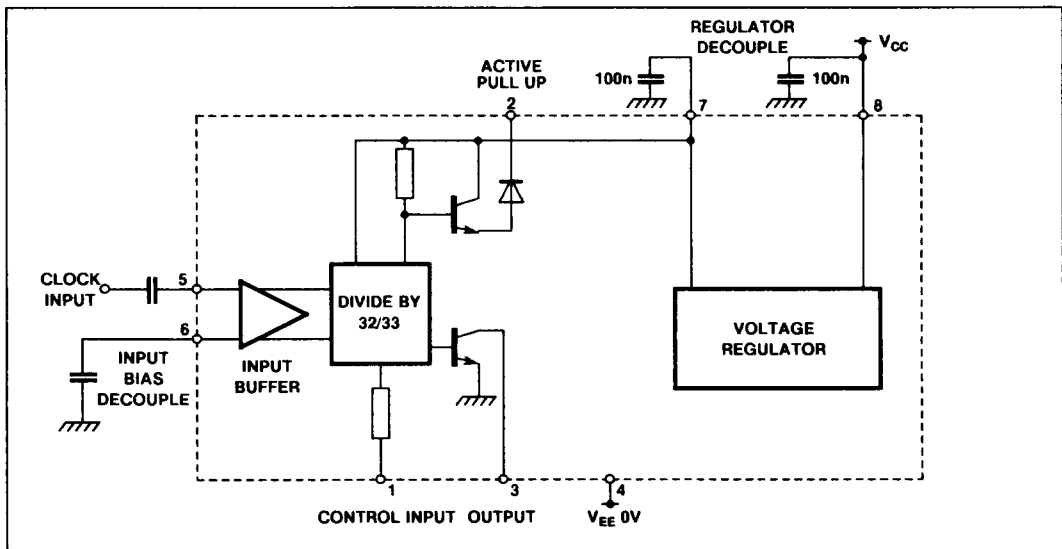


Fig 2 SP8797 Block Diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated)

Supply Voltage $V_{CC} = +4.5V$ to $5.5V$ $T_{amb} = -55^{\circ}C$ to $+125^{\circ}C$

Characteristic	Sym	Value		Units	Conditions
		Min.	Max.		
Supply current	I_{CC}		7.8	mA	
Maximum frequency (sinewave input)	f_{MAX}	225		MHz	Input = 200mV to 800mV p-p
Minimum frequency (sinewave input)	f_{MIN}		20	MHz	Input = 200mV to 800mV p-p
Control input high voltage	V_{INH}	2	5.5	V	Pin 7 Voltage = 5.5V
Control input low voltage	V_{INL}	0	0.8	V	
Output high voltage	V_{OH}	2.5		V	Pin 2 connected to pin 3 $V_{CC} = 4.5V$ $I_{OH} = 100\mu A$
Output low voltage	V_{OL}		0.5	V	Pin 2 connected to pin 3 $I_{OL} = 1.6mA$
Set up time	t_s	14		ns	$25^{\circ}C$
Release time	t_r	20		ns	$25^{\circ}C$
Clock to output propagation time	t_p		45	ns	$25^{\circ}C$

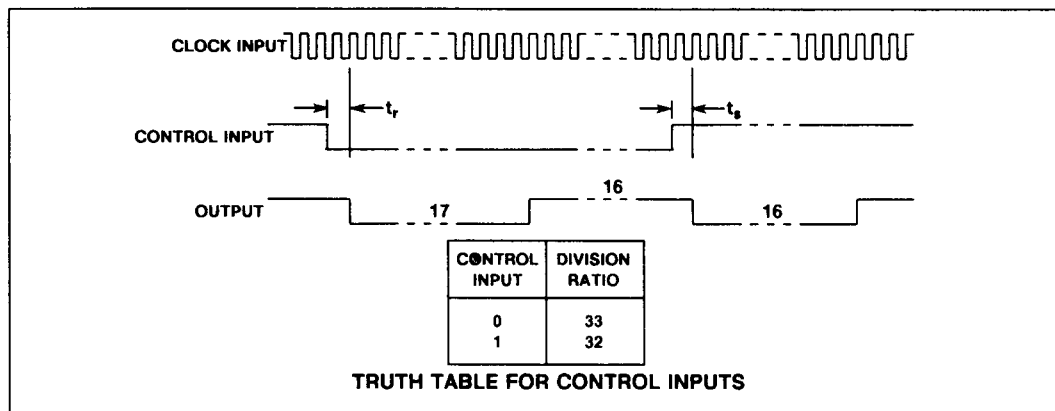


Fig.3 Timing diagram SP8797A

NOTES

The set up time t_s is defined as the minimum time that can elapse between the LOW to HIGH transition of control input and the next LOW to HIGH clock pulse transition to ensure +32 mode is selected.

The release time t_r is defined as the minimum time that can elapse between the HIGH to LOW transition of the control input and the next LOW to HIGH clock pulse transition to ensure +33 mode is selected.

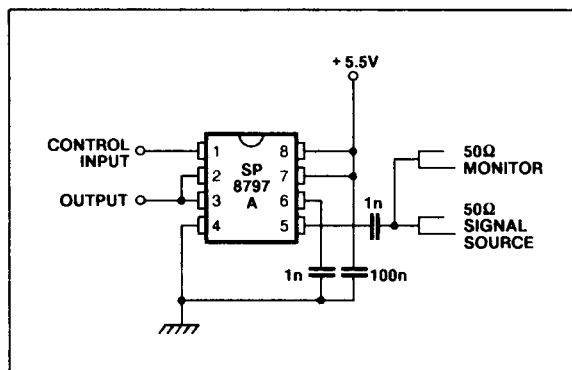


Fig.4 Toggle frequency test circuit

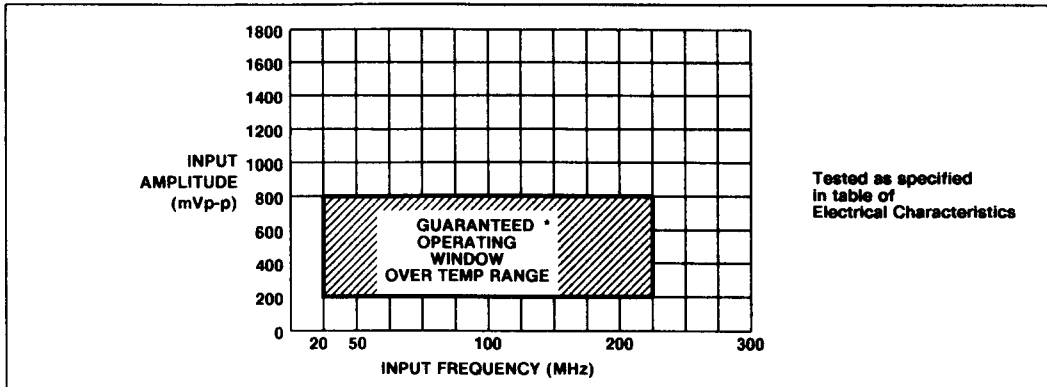


Fig.5 Input sensitivity SP8797A

OPERATING NOTES

1. The clock input (pin 5) should be capacitively coupled to the signal source. The input signal path is completed by coupling a capacitor from the internal bias decoupling, Pin 6 to ground.
2. The output on pin 3 is an open collector and can be interfaced to CMOS by connecting a pull up resistor to a positive supply of up to +9.5V. The sink current through this resistor should not exceed 2mA. When an interface to TTL is required, the active pull up on pin 2 should be connected to pin 3, giving a fan out of 1. The supply current will be increased by approximately 2mA.
3. The circuit will operate down to DC but a slew rate of better than 20V/ μ s is required on the clock input.
4. The mark to space ratio at the output is approximately 1.2:1 at 225 MHz.

5. Input impedance is a function of frequency. See Fig.6.
6. If no signal is present the device will self-oscillate. If this is undesirable it may be prevented by connecting a 680K resistor between the unused input and ground. This reduces the input sensitivity by typically 50-100mV p-p.

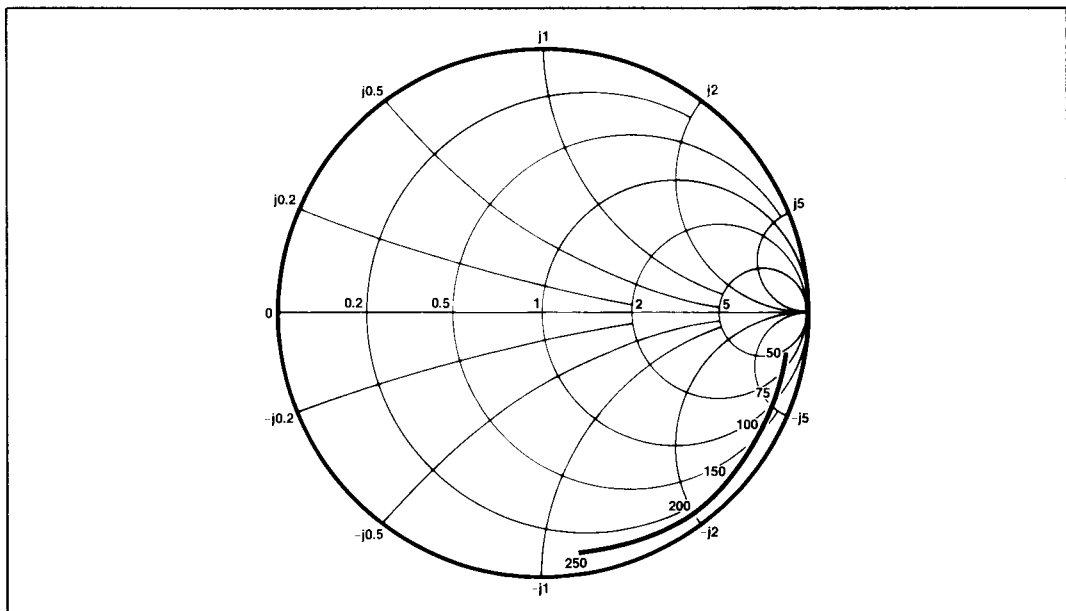


Fig.6 Typical input impedance. Test conditions: supply voltage 5.2V, ambient temperature 25°C, frequencies in MHz, impedances normalised to 50 ohms.