
HM5116405B Series HM5117405B Series

4,194,304-word $\times$ 4-bit Dynamic Random Access Memory

HITACHI

ADE-203-511A (Z)

Rev. 1.0

Mar. 28, 1996

Description

The Hitachi HM5116405B Series, HM5117405B Series are CMOS dynamic RAMs organized 4,194,304-word $\times$ 4-bit. They employ the most advanced CMOS technology for high performance and low power. The HM5116405B Series, HM5117405B Series offer Extended Data Out (EDO) Page Mode as a high speed access mode.

Features

- Single 5 V ($\pm 10\%$)
- High speed
 - Access time: 60 ns/70 ns/80 ns (max)
- Low power dissipation
 - Active mode : 550mW/495 mW/440 mW (max) (HM5116405B Series)
: 605mW/550 mW/495 mW (max) (HM5117405B Series)
 - Standby mode : 11 mW (max)
: 0.83 mW (max) (L-version)
- EDO page mode capability
- Long refresh period
 - 4096 refresh cycles : 64 ms (HM5116405B Series)
: 128 ms (L-version)
 - 2048 refresh cycles : 32 ms (HM5117405B Series)
: 128 ms (L-version)
- 3 variations of refresh
 - $\overline{\text{RAS}}$ -only refresh
 - $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh
 - Hidden refresh
- Battery backup operation (L-version)

This specification is fully compatible with the 16-Mbit DRAM specifications from TEXAS INSTRUMENTS.

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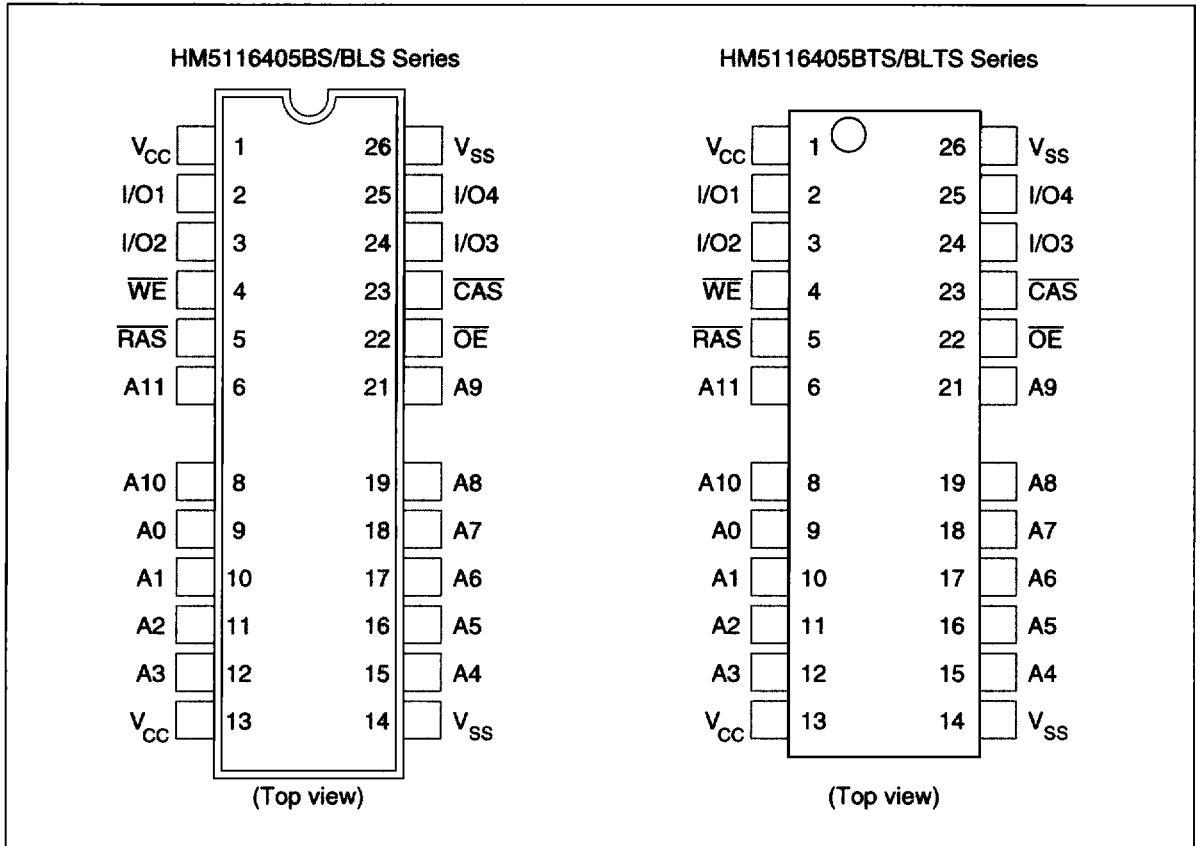
- Test function
 - 16-bit parallel test mode

Ordering Information

Type No.	Access time	Package
HM5116405BS-6	60 ns	300-mil 26-pin plastic SOJ (CP-26/24DB)
HM5116405BS-7	70 ns	
HM5116405BS-8	80 ns	
HM5116405BLS-6	60 ns	
HM5116405BLS-7	70 ns	
HM5116405BLS-8	80 ns	
HM5117405BS-6	60 ns	
HM5117405BS-7	70 ns	
HM5117405BS-8	80 ns	
HM5117405BLS-6	60 ns	
HM5117405BLS-7	70 ns	
HM5117405BLS-8	80 ns	
HM5116405BTS-6	60 ns	300-mil 26-pin plastic TSOP II (TTP-26/24DA)
HM5116405BTS-7	70 ns	
HM5116405BTS-8	80 ns	
HM5116405BLTS-6	60 ns	
HM5116405BLTS-7	70 ns	
HM5116405BLTS-8	80 ns	
HM5117405BTS-6	60 ns	
HM5117405BTS-7	70 ns	
HM5117405BTS-8	80 ns	
HM5117405BLTS-6	60 ns	
HM5117405BLTS-7	70 ns	
HM5117405BLTS-8	80 ns	

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Pin Arrangement

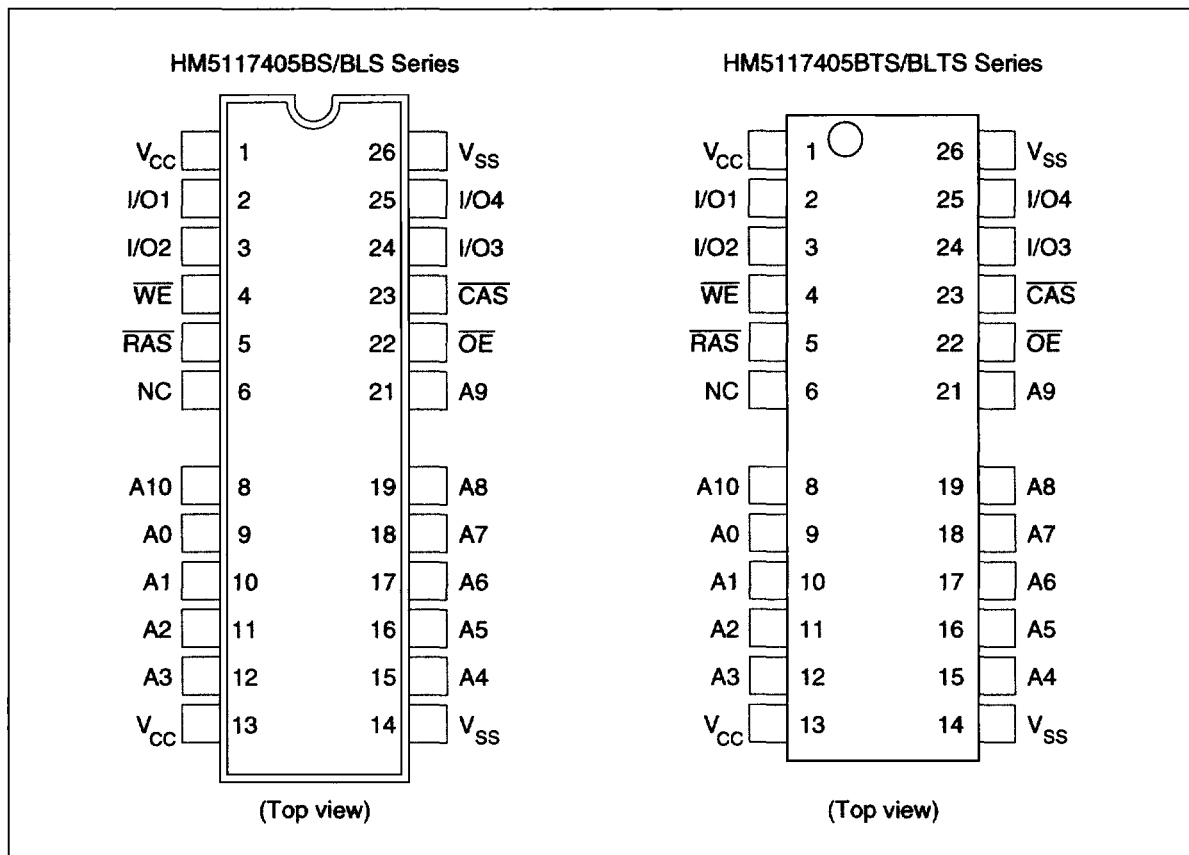


Pin Description

Pin name	Function
A0 to A11	Address input — Row/Refresh address A0 to A11 — Column address A0 to A9
I/O1 to I/O4	Data input/Data output
$\overline{\text{RAS}}$	Row address strobe
$\overline{\text{CAS}}$	Column address strobe
$\overline{\text{WE}}$	Write enable
$\overline{\text{OE}}$	Output enable
V_{CC}	Power supply
V_{SS}	Ground

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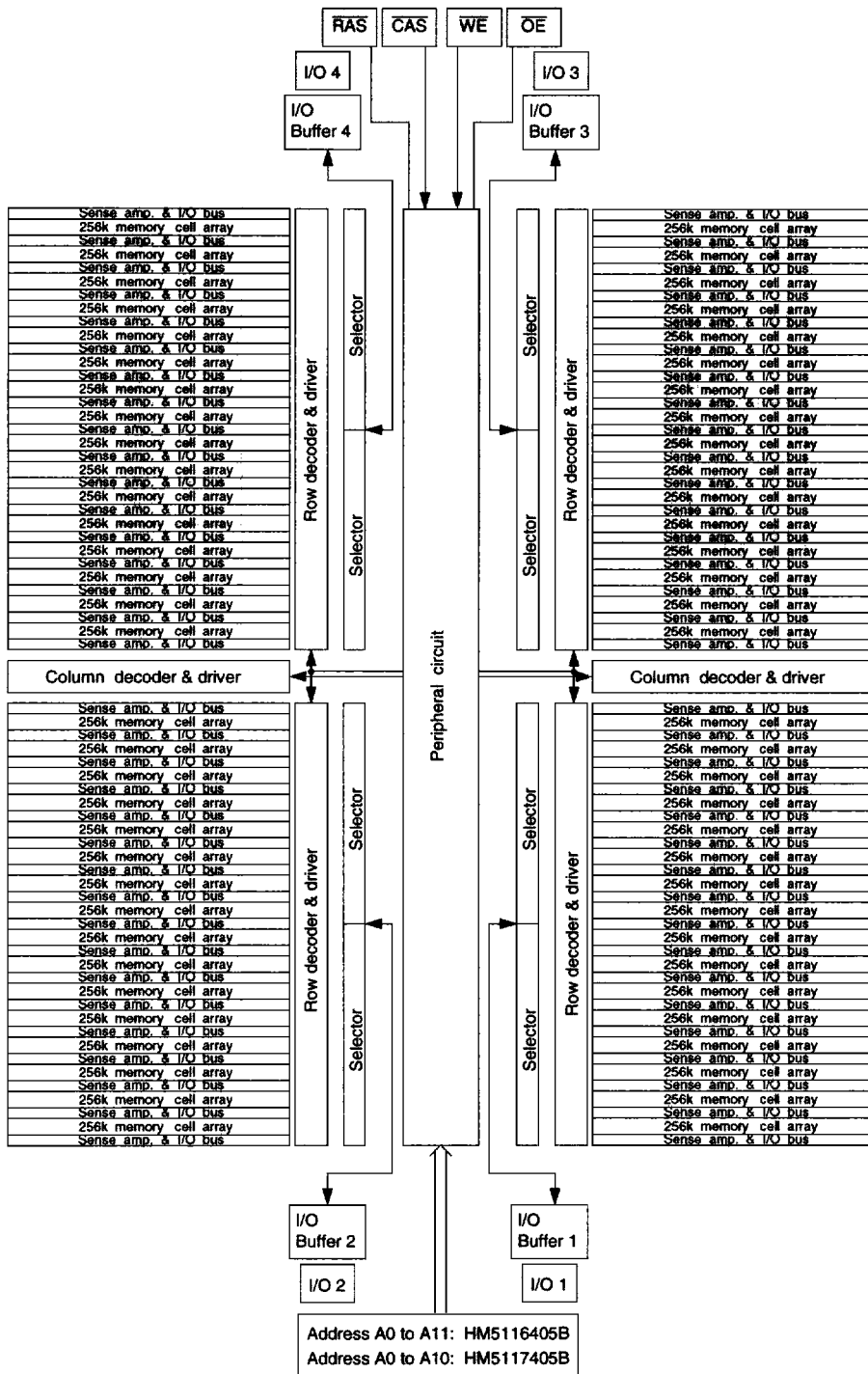
Pin Arrangement



Pin Description

Pin name	Function
A0 to A10	Address input — Row/Refresh address A0 to A10 — Column address A0 to A10
I/O1 to I/O4	Data input/Data output
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{WE}$	Write enable
$\overline{OE}$	Output enable
V_{CC}	Power supply
V_{SS}	Ground
NC	No connection

Block Diagram



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Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_T	-1.0 to +7.0	V
Supply voltage relative to V_{SS}	V_{CC}	-1.0 to +7.0	V
Short circuit output current	I_{out}	50	mA
Power dissipation	P_T	1.0	W
Operating temperature	T_{opr}	0 to +70	°C
Storage temperature	T_{stg}	-55 to +125	°C

Recommended DC Operating Conditions ($T_a = 0$ to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{CC}	4.5	5.0	5.5	V	1
Input high voltage	V_{IH}	2.4	—	6.5	V	1
Input low voltage	V_{IL}	-1.0	—	0.8	V	1

Note: 1. All voltage referred to V_{SS} .

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DC Characteristics

(Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V) (HM5116405B Series)

HM5116405B									
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Test conditions
Operating current ^{*1, *2}	I _{CC1}	—	80	—	70	—	65	mA	t _{RC} = min
Standby current	I _{CC2}	—	2	—	2	—	2	mA	TTL interface R _{AS} , C _{AS} = V _{IH} Dout = High-Z
		—	1	—	1	—	1	mA	CMOS interface R _{AS} , C _{AS} ≥ V _{CC} - 0.2 V Dout = High-Z
Standby current (L-version)	I _{CC2}	—	150	—	150	—	150	μA	CMOS interface R _{AS} , C _{AS} ≥ V _{CC} - 0.2 V Dout = High-Z
R _{AS} -only refresh current ^{*2}	I _{CC3}	—	80	—	70	—	65	mA	t _{RC} = min
Standby current ^{*1}	I _{CC5}	—	5	—	5	—	5	mA	R _{AS} = V _{IH} C _{AS} = V _{IL} Dout = enable
CAS-before-R _{AS} refresh current	I _{CC6}	—	80	—	70	—	65	mA	t _{RC} = min
EDO page mode current ^{*1, *3}	I _{CC7}	—	100	—	90	—	80	mA	t _{HPC} = min
Battery backup current	I _{CC10}	—	350	—	350	—	350	μA	CMOS interface Dout = High-Z, CBR refresh: t _{RC} = 31.3 μs t _{RAS} ≤ 0.3 μs
Input leakage current	I _{LI}	-10	10	-10	10	-10	10	μA	0 V ≤ Vin ≤ 7 V
Output leakage current	I _{LO}	-10	10	-10	10	-10	10	μA	0 V ≤ Vin ≤ 7 V Dout = disable
Output high voltage	V _{OH}	2.4	V _{CC}	2.4	V _{CC}	2.4	V _{CC}	V	High Iout = -2 mA
Output low voltage	V _{OL}	0	0.4	0	0.4	0	0.4	V	Low Iout = 2 mA

Notes : 1. I_{CC} depends on output load condition when the device is selected. I_{CC} max is specified at the output open condition.

2. Address can be changed once or less while R_{AS} = V_{IL}.

3. Address can be changed once or less while C_{AS} = V_{IH}.

HM5116405B Series, HM5117405B Series

DC Characteristics

(Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V) (HM5117405B Series)

HM5117405B									
		-6		-7		-8			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Test conditions
Operating current*1, *2	I _{CC1}	—	110	—	100	—	90	mA	t _{RC} = min
Standby current	I _{CC2}	—	2	—	2	—	2	mA	TTL interface RAS, CAS = V _{IH} Dout = High-Z
		—	1	—	1	—	1	mA	CMOS interface RAS, CAS ≥ V _{CC} - 0.2 V Dout = High-Z
Standby current (L-version)	I _{CC2}	—	150	—	150	—	150	μA	CMOS interface RAS, CAS ≥ V _{CC} - 0.2 V Dout = High-Z
RAS-only refresh current*2	I _{CC3}	—	110	—	100	—	90	mA	t _{RC} = min
Standby current*1	I _{CC5}	—	5	—	5	—	5	mA	RAS = V _{IH} CAS = V _{IL} Dout = enable
CAS-before-RAS refresh current	I _{CC6}	—	110	—	100	—	90	mA	t _{RC} = min
EDO page mode current*1, *3	I _{CC7}	—	110	—	100	—	90	mA	t _{HPC} = min
Battery backup current	I _{CC10}	—	350	—	350	—	350	μA	CMOS interface Dout = High-Z, CBR refresh: t _{RC} = 62.5 μs t _{RAS} ≤ 0.3 μs
Input leakage current	I _{LI}	-10	10	-10	10	-10	10	μA	0 V ≤ Vin ≤ 7 V
Output leakage current	I _{LO}	-10	10	-10	10	-10	10	μA	0 V ≤ Vin ≤ 7 V Dout = disable
Output high voltage	V _{OH}	2.4	V _{CC}	2.4	V _{CC}	2.4	V _{CC}	V	High Iout = -2 mA
Output low voltage	V _{OL}	0	0.4	0	0.4	0	0.4	V	Low Iout = 2 mA

Notes : 1. I_{CC} depends on output load condition when the device is selected. I_{CC} max is specified at the output open condition.

2. Address can be changed once or less while RAS = V_{IL}.

3. Address can be changed once or less while CAS = V_{IH}.

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Capacitance ($T_a = 25^\circ\text{C}$, $V_{CC} = 5\text{ V} \pm 10\%$)

Parameter	Symbol	Typ	Max	Unit	Notes
Input capacitance (Address)	C_{I1}	—	5	pF	1
Input capacitance (Clocks)	C_{I2}	—	7	pF	1
Output capacitance (Data-in, Data-out)	C_{IO}	—	7	pF	1, 2

Notes : 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.

2. $\overline{\text{CAS}} = V_{IH}$ to disable Dout.

HM5116405B Series, HM5117405B Series

AC Characteristics ($T_a = 0$ to $+70^\circ\text{C}$, $V_{CC} = 5\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$) *¹, *², *¹⁸

Test Conditions

- Input rise and fall time: 2 ns
- Input levels: $V_{IL} = 0\text{ V}$, $V_{IH} = 3\text{ V}$
- Input timing reference levels: 0.8 V, 2.4 V
- Output timing reference levels: 0.8 V, 2.0 V
- Output load: 1 TTL gate + C_L (100 pF) (Including scope and jig)

Read, Write, Read-Modify-Write and Refresh Cycles (Common parameters)

		HM5116405B/HM5117405B							
		-6		-7		-8			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Random read or write cycle time	t_{RC}	104	—	124	—	144	—	ns	
$\overline{\text{RAS}}$ precharge time	t_{RP}	40	—	50	—	60	—	ns	
$\overline{\text{CAS}}$ precharge time	t_{CP}	10	—	13	—	15	—	ns	
$\overline{\text{RAS}}$ pulse width	t_{RAS}	60	10000	70	10000	80	10000	ns	
$\overline{\text{CAS}}$ pulse width	t_{CAS}	10	10000	13	10000	15	10000	ns	
Row address setup time	t_{ASR}	0	—	0	—	0	—	ns	
Row address hold time	t_{RAH}	10	—	10	—	10	—	ns	
Column address setup time	t_{ASC}	0	—	0	—	0	—	ns	
Column address hold time	t_{CAH}	10	—	13	—	15	—	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time	t_{RCD}	20	45	20	52	20	60	ns	3
$\overline{\text{RAS}}$ to column address delay time	t_{RAD}	15	30	15	35	15	40	ns	4
$\overline{\text{RAS}}$ hold time	t_{RSH}	15	—	18	—	20	—	ns	
$\overline{\text{CAS}}$ hold time	t_{CSH}	48	—	58	—	68	—	ns	
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ precharge time	t_{CRP}	5	—	5	—	5	—	ns	
$\overline{\text{OE}}$ to Din delay time	t_{OED}	15	—	18	—	20	—	ns	5
$\overline{\text{OE}}$ delay time from Din	t_{DZO}	0	—	0	—	0	—	ns	6
$\overline{\text{CAS}}$ delay time from Din	t_{DZC}	0	—	0	—	0	—	ns	6
Transition time (rise and fall)	t_T	2	50	2	50	2	50	ns	7

HM5116405B Series, HM5117405B Series

Read Cycle

		HM5116405B/HM5117405B							
		-6		-7		-8			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Access time from $\overline{\text{RAS}}$	t_{RAC}	—	60	—	70	—	80	ns	8, 9, 19
Access time from $\overline{\text{CAS}}$	t_{CAC}	—	15	—	18	—	20	ns	9, 10, 17, 19
Access time from address	t_{AA}	—	30	—	35	—	40	ns	9, 11, 17, 19
Access time from $\overline{\text{OE}}$	t_{OEA}	—	15	—	18	—	20	ns	9, 19
Read command setup time	t_{RCS}	0	—	0	—	0	—	ns	
Read command hold time to $\overline{\text{CAS}}$	t_{RCH}	0	—	0	—	0	—	ns	12
Read command hold time from $\overline{\text{RAS}}$	t_{RCHR}	60	—	70	—	80	—	ns	
Read command hold time to $\overline{\text{RAS}}$	t_{RRH}	0	—	0	—	0	—	ns	12
Column address to $\overline{\text{RAS}}$ lead time	t_{RAL}	30	—	35	—	40	—	ns	
Column address to $\overline{\text{CAS}}$ lead time	t_{CAL}	18	—	23	—	28	—	ns	
$\overline{\text{CAS}}$ to output in low-Z	t_{CLZ}	0	—	0	—	0	—	ns	
Output data hold time	t_{OH}	3	—	3	—	3	—	ns	
Output data hold time from $\overline{\text{OE}}$	t_{OHO}	3	—	3	—	3	—	ns	
Output buffer turn-off time	t_{OFF}	—	15	—	15	—	15	ns	13
Output buffer turn-off to $\overline{\text{OE}}$	t_{OEZ}	—	15	—	15	—	15	ns	13
$\overline{\text{CAS}}$ to Din delay time	t_{CDD}	15	—	18	—	20	—	ns	5
Output data hold time from $\overline{\text{RAS}}$	t_{OHR}	3	—	3	—	3	—	ns	
Output buffer turn-off to $\overline{\text{RAS}}$	t_{OFR}	—	15	—	15	—	15	ns	
Output buffer turn-off to $\overline{\text{WE}}$	t_{WEZ}	—	15	—	15	—	15	ns	
$\overline{\text{WE}}$ to Din delay time	t_{WED}	15	—	18	—	20	—	ns	
$\overline{\text{RAS}}$ to Din delay time	t_{RDD}	15	—	18	—	20	—	ns	

HM5116405B Series, HM5117405B Series

Write Cycle

		HM5116405B/HM5117405B							
		-6		-7		-8			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Write command setup time	t_{WCS}	0	—	0	—	0	—	ns	14
Write command hold time	t_{WCH}	10	—	13	—	15	—	ns	
Write command pulse width	t_{WCP}	10	—	10	—	10	—	ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	10	—	13	—	15	—	ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	10	—	13	—	15	—	ns	
Data-in setup time	t_{DS}	0	—	0	—	0	—	ns	15
Data-in hold time	t_{DH}	10	—	13	—	15	—	ns	15

Read-Modify-Write Cycle

		HM5116405B/HM5117405B							
		-6		-7		-8			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Read-modify-write cycle time	t_{RWC}	149	—	175	—	199	—	ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	t_{RWD}	82	—	95	—	107	—	ns	14
$\overline{CAS}$ to $\overline{WE}$ delay time	t_{CWD}	37	—	43	—	47	—	ns	14
Column address to $\overline{WE}$ delay time	t_{AWD}	52	—	60	—	67	—	ns	14
$\overline{OE}$ hold time from $\overline{WE}$	t_{OEHL}	15	—	18	—	20	—	ns	

Refresh Cycle

		HM5116405B/HM5117405B							
		-6		-7		-8			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
$\overline{CAS}$ setup time (CBR refresh cycle)	t_{CSR}	5	—	5	—	5	—	ns	
$\overline{CAS}$ hold time (CBR refresh cycle)	t_{CHR}	10	—	10	—	10	—	ns	
$\overline{WE}$ setup time (CBR refresh cycle)	t_{WRP}	0	—	0	—	0	—	ns	
$\overline{WE}$ hold time (CBR refresh cycle)	t_{WRH}	10	—	10	—	10	—	ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	0	—	0	—	0	—	ns	

HM5116405B Series, HM5117405B Series

EDO Page Mode Cycle

		HM5116405B/HM5117405B							
		-6		-7		-8			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
EDO page mode cycle time	t_{HPC}	25	—	30	—	35	—	ns	20
EDO page mode $\overline{RAS}$ pulse width	t_{RASP}	—	100000	—	100000	—	100000	ns	16
Access time from $\overline{CAS}$ precharge	t_{CPA}	—	35	—	40	—	45	ns	9, 17, 19
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{CPRH}	35	—	40	—	45	—	ns	
Output data hold time from $\overline{CAS}$ low	t_{DOH}	3	—	3	—	3	—	ns	9, 17
$\overline{CAS}$ hold time referred $\overline{OE}$	t_{COL}	10	—	13	—	15	—	ns	
$\overline{CAS}$ to $\overline{OE}$ setup time	t_{COP}	5	—	5	—	5	—	ns	
Read command hold time from $\overline{CAS}$ precharge	t_{RCHC}	35	—	40	—	45	—	ns	

EDO Page Mode Read-Modify-Write Cycle

		HM5116405B/HM5117405B							
		-6		-7		-8			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
EDO page mode read- modify-write cycle time	t_{HPRWC}	79	—	90	—	99	—	ns	
$\overline{WE}$ delay time from $\overline{CAS}$ precharge	t_{CPW}	54	—	62	—	69	—	ns	14

Test Mode Cycle *18

		HM5116405B/HM5117405B							
		-6		-7		-8			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Test mode $\overline{WE}$ setup time	t_{WTS}	0	—	0	—	0	—	ns	
Test mode $\overline{WE}$ hold time	t_{WTH}	10	—	10	—	10	—	ns	

Refresh (HM5116405B Series)

Parameter	Symbol	Max	Unit	Notes
Refresh period	t_{REF}	64	ms	4096 cycles
Refresh period (L-version)	t_{REF}	128	ms	4096 cycles

HM5116405B Series, HM5117405B Series

Refresh (HM5117405B Series)

Parameter	Symbol	Max	Unit	Notes
Refresh period	t_{REF}	32	ms	2048 cycles
Refresh period (L-version)	t_{REF}	128	ms	2048 cycles

Notes: 1. AC measurements assume $t_T = 2$ ns.

- An initial pause of 200 μ s is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing $\overline{RAS}$ -only refresh or $\overline{CAS}$ -before- $\overline{RAS}$ refresh). If the internal refresh counter is used, a minimum of eight $\overline{CAS}$ -before- $\overline{RAS}$ refresh cycles are required.
 - Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC} .
 - Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA} .
 - Either t_{OED} or t_{CDD} must be satisfied.
 - Either t_{DZO} or t_{DZC} must be satisfied.
 - V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} (min) and V_{IL} (max).
 - Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
 - Measured with a load circuit equivalent to 1 TTL loads and 100 pF.
 - Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{RCD} + t_{CAC}$ (max) $\geq t_{RAD} + t_{AA}$ (max).
 - Assumes that $t_{RAD} \geq t_{RAD}$ (max) and $t_{RCD} + t_{CAC}$ (max) $\leq t_{RAD} + t_{AA}$ (max).
 - Either t_{RCH} or t_{RRH} must be satisfied for a read cycles.
 - t_{OFF} (max) and t_{OEZ} (max) define the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.
 - t_{WCS} , t_{RWD} , t_{CWD} , t_{AWD} and t_{CPW} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geq t_{RWD}$ (min), $t_{CWD} \geq t_{CWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), or $t_{CWD} \geq t_{CWD}$ (min), $t_{AWD} \geq t_{AWD}$ (min) and $t_{CPW} \geq t_{CPW}$ (min), the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
 - These parameters are referred to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in delayed write or read-modify-write cycles.
 - t_{RASP} defines $\overline{RAS}$ pulse width in EDO page mode cycles.
 - Access time is determined by the longest among t_{AA} , t_{CAC} and t_{CPA} .
 - The 16M DRAM offers a 16-bit time saving parallel test mode. Address CA0 and CA1 for the 4M $\times 4$ are don't care during test mode. Test mode is set by performing a $\overline{WE}$ -and- $\overline{CAS}$ -before- $\overline{RAS}$ (WCBR) cycle. In 16-bit parallel test mode, data is written into 4 bits in parallel at each I/O (I/O1 to I/O4) and read out from each I/O.
- If 4 bits of each I/O are equal (all 1s or 0s), data output pin is a high state during test mode read cycle, then the device has passed. If they are not equal, data output pin is a low state, then the device has failed.
- Refresh during test mode operation can be performed by normal read cycles or by WCBR refresh cycles.

HM5116405B Series, HM5117405B Series

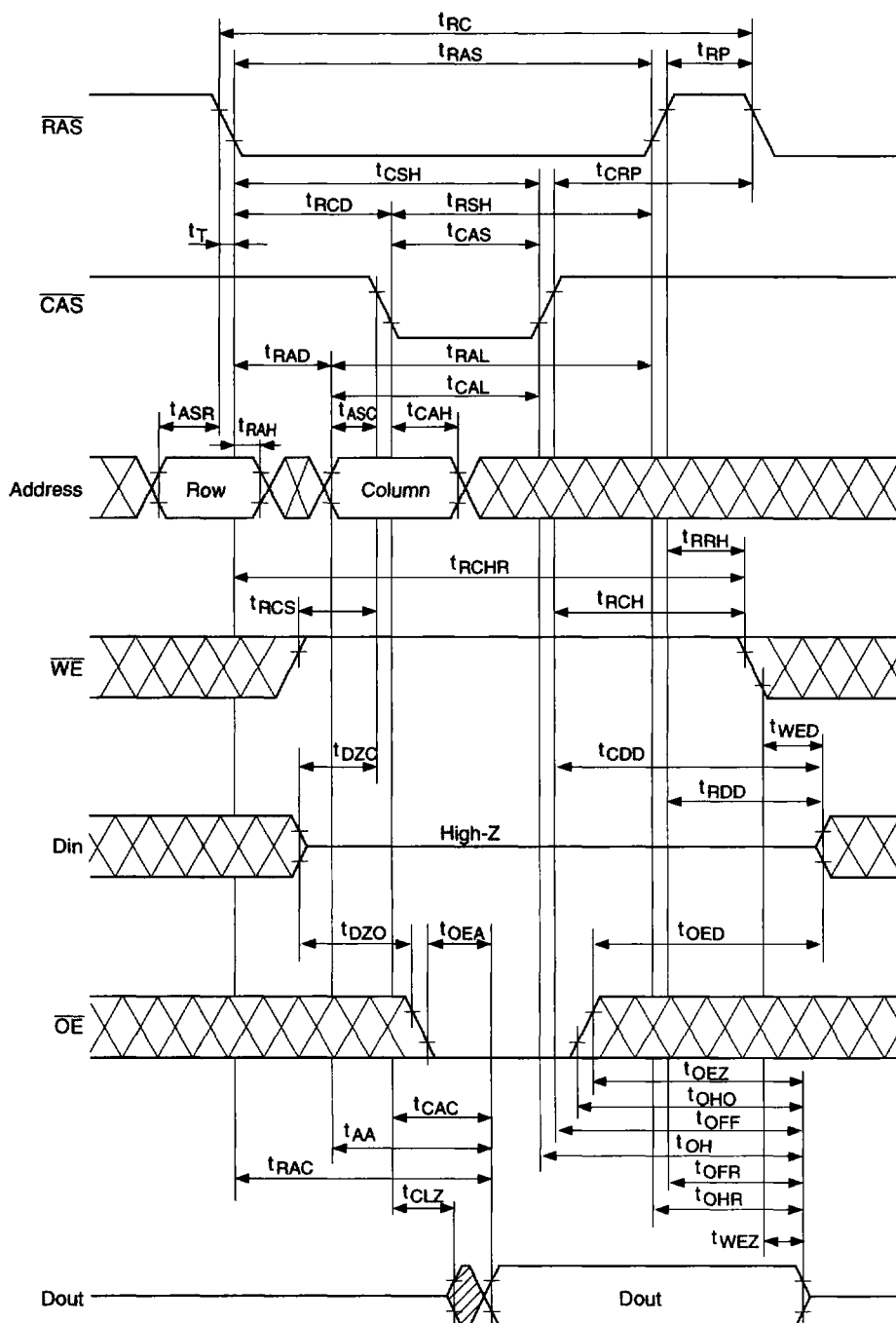
To get out of test mode and enter a normal operation mode, perform either a regular $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh cycle or $\overline{\text{RAS}}$ -only refresh cycle.

19. In a test mode read cycle, the value of t_{RAC} , t_{AA} , t_{CAC} and t_{CPA} is delayed by 2 ns to 5 ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
20. t_{HPC} (min) can be achieved during a series of EDO page mode write cycles or EDO page mode read cycles. If both write and read operation are mixed in a EDO page mode $\overline{\text{RAS}}$ cycle (EDO page mode mix cycle (1), (2)), minimum value of $\overline{\text{CAS}}$ cycle ($t_{\text{CAS}} + t_{\text{CP}} + 2 t_{\text{T}}$) becomes greater than the specified t_{HPC} (min) value. The value of $\overline{\text{CAS}}$ cycle time of mixed EDO page mode is shown in EDO page mode mix cycle (1) and (2).
21. XXX: H or L (H: V_{IH} (min) $\leq V_{\text{IN}} \leq V_{\text{IH}}$ (max), L: V_{IL} (min) $\leq V_{\text{IN}} \leq V_{\text{IL}}$ (max))
/////: Invalid Out

HM5116405B Series, HM5117405B Series

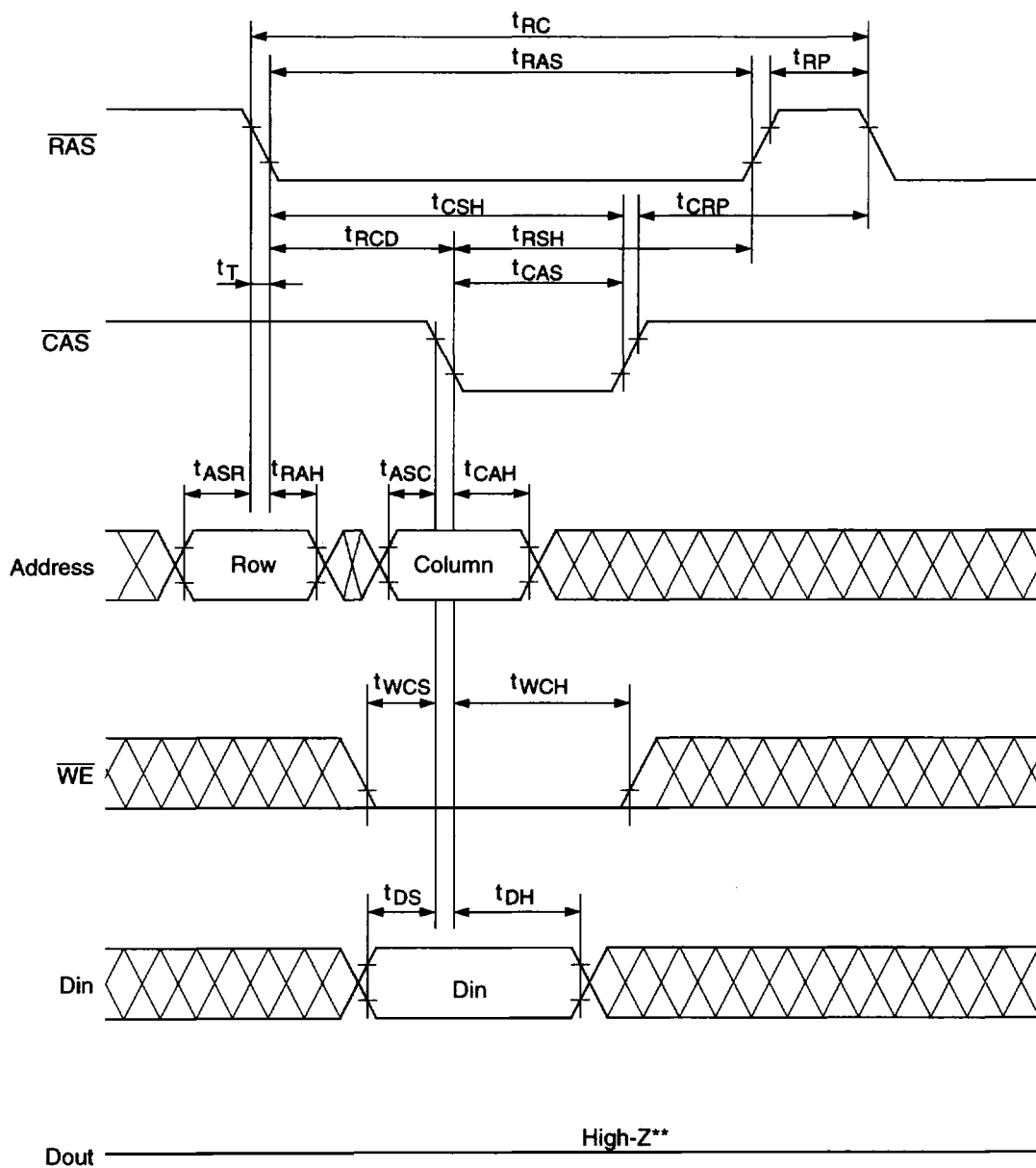
Timing Waveforms*21

Read Cycle



HM5116405B Series, HM5117405B Series

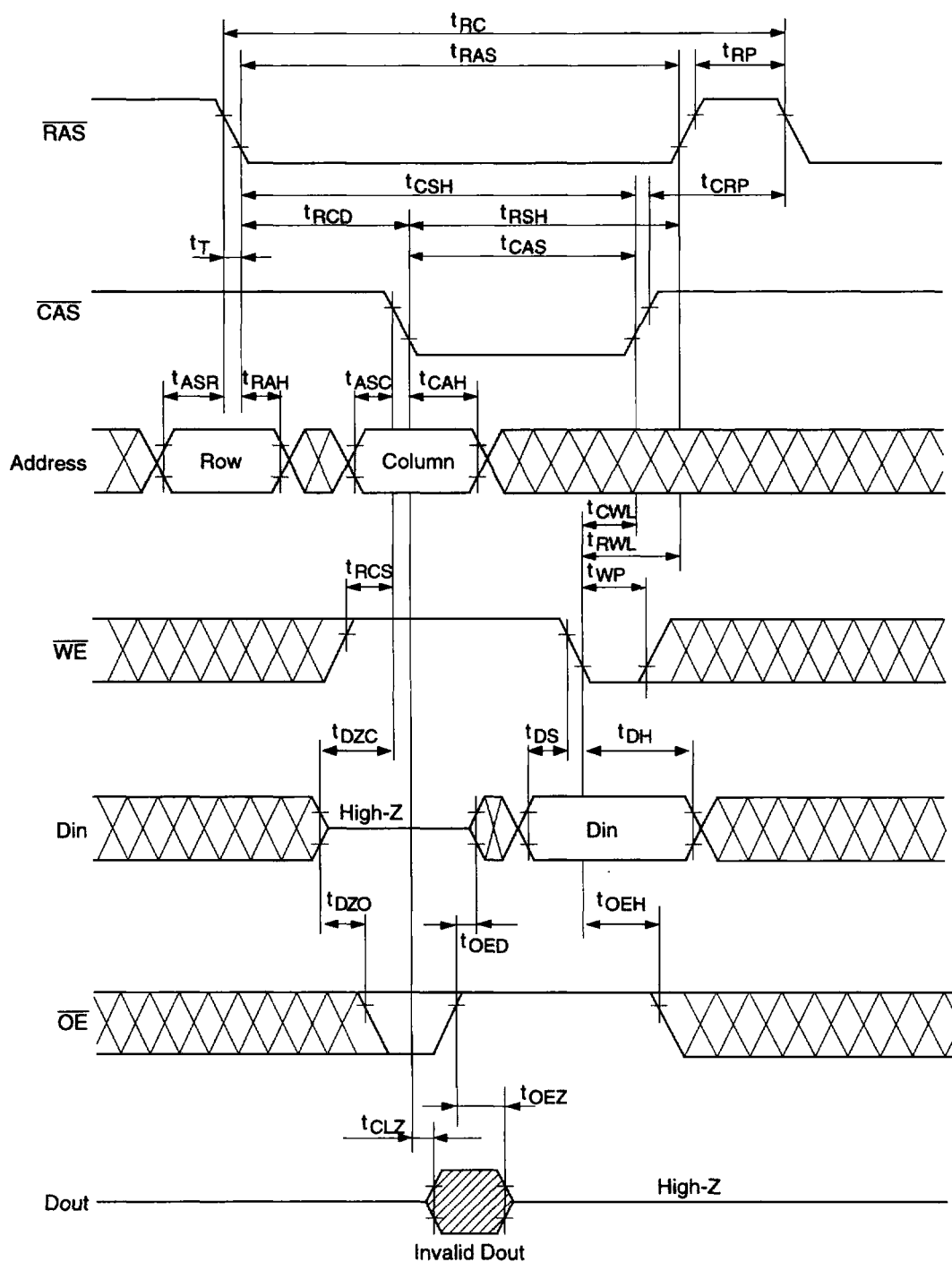
Early Write Cycle



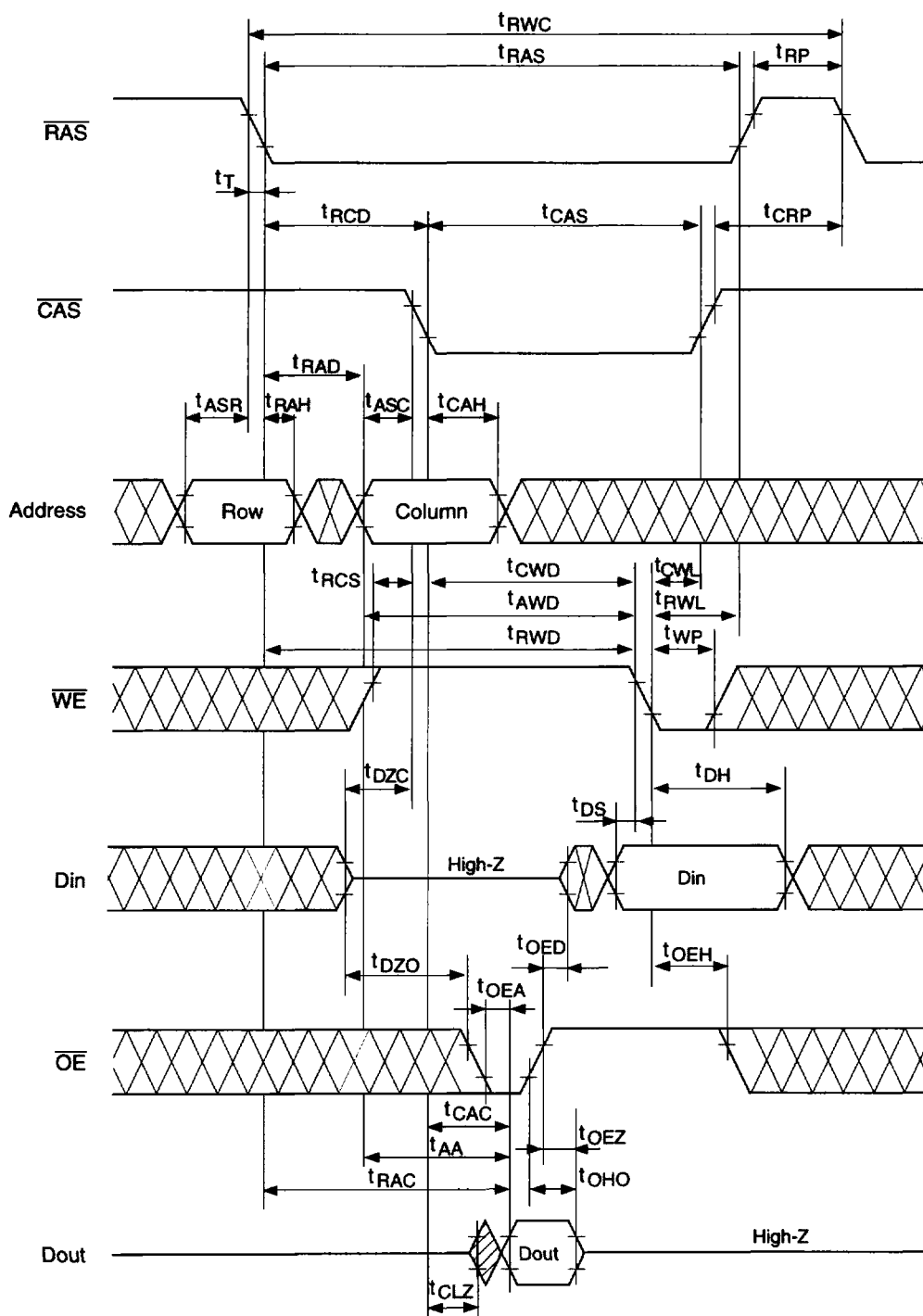
* $\overline{OE}$: H or L

** $t_{WCS} \cong t_{WCS}(\text{min})$

Delayed Write Cycle

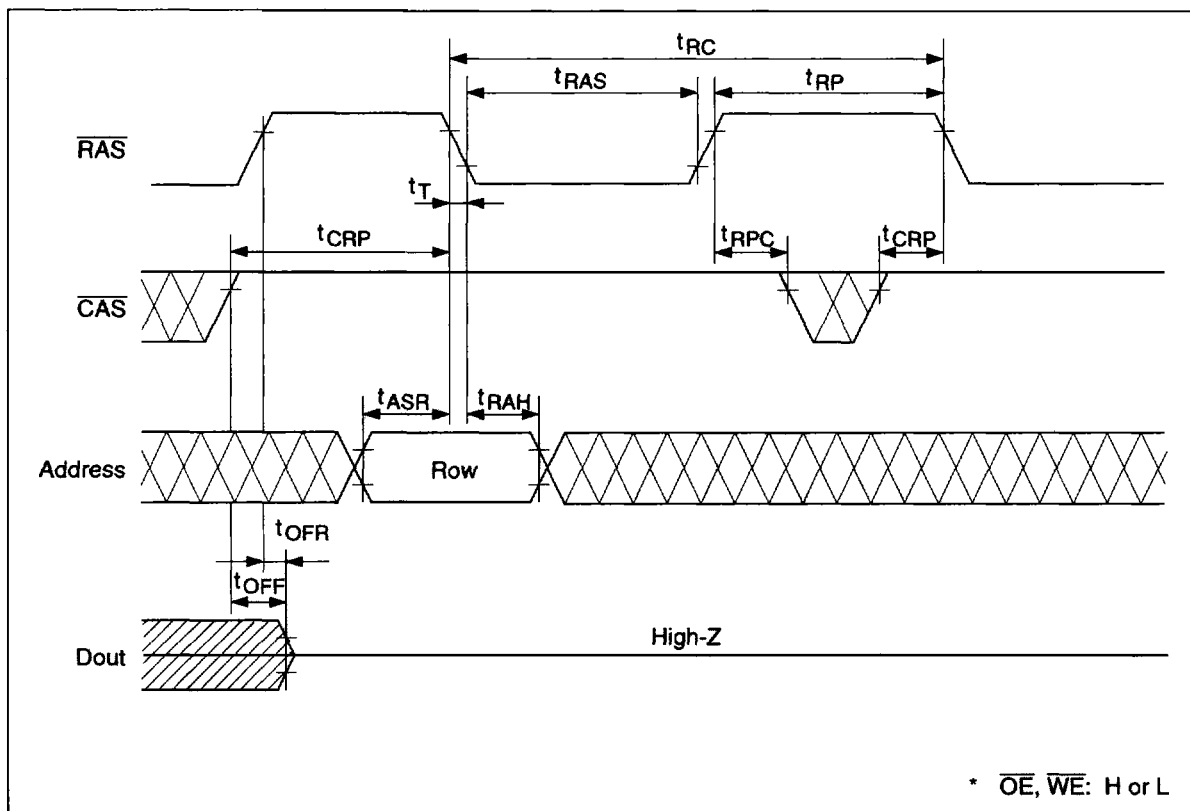


Read-Modify-Write Cycle

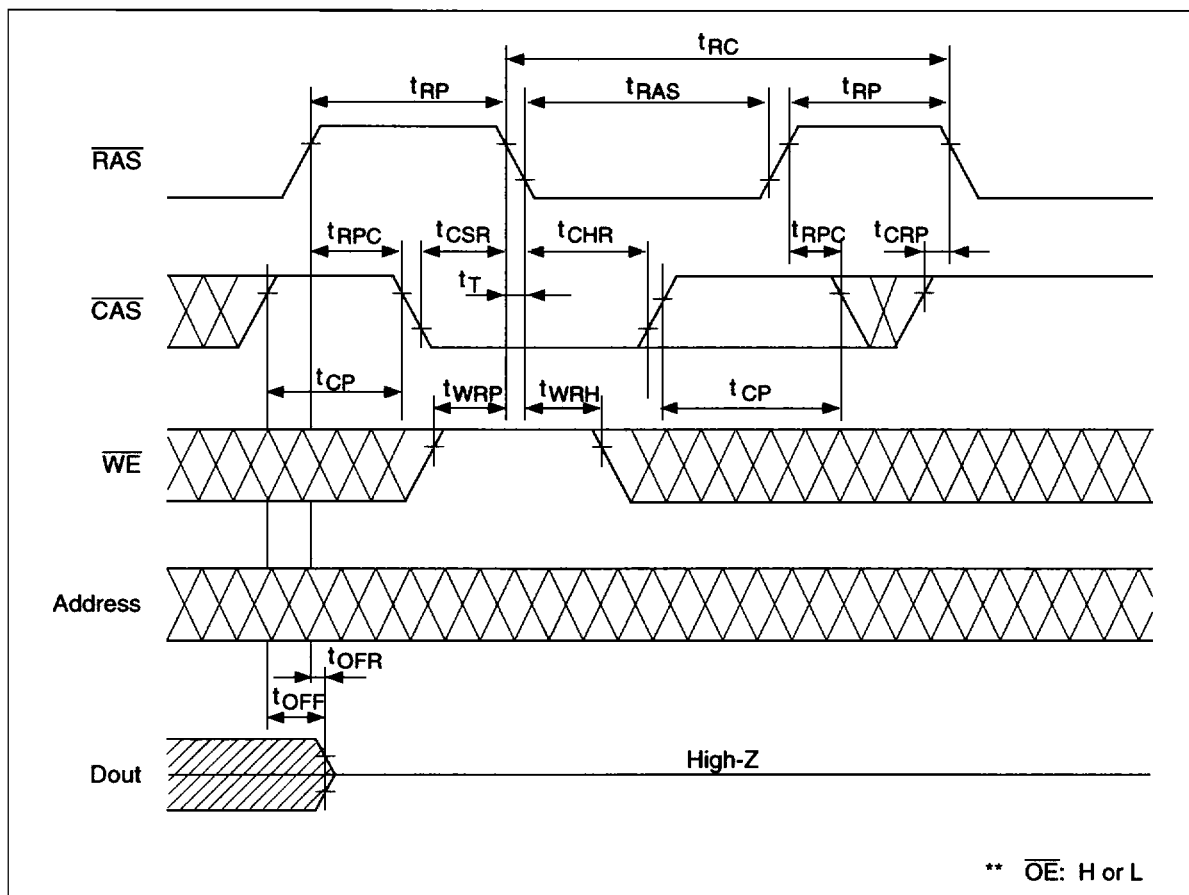


HM5116405B Series, HM5117405B Series

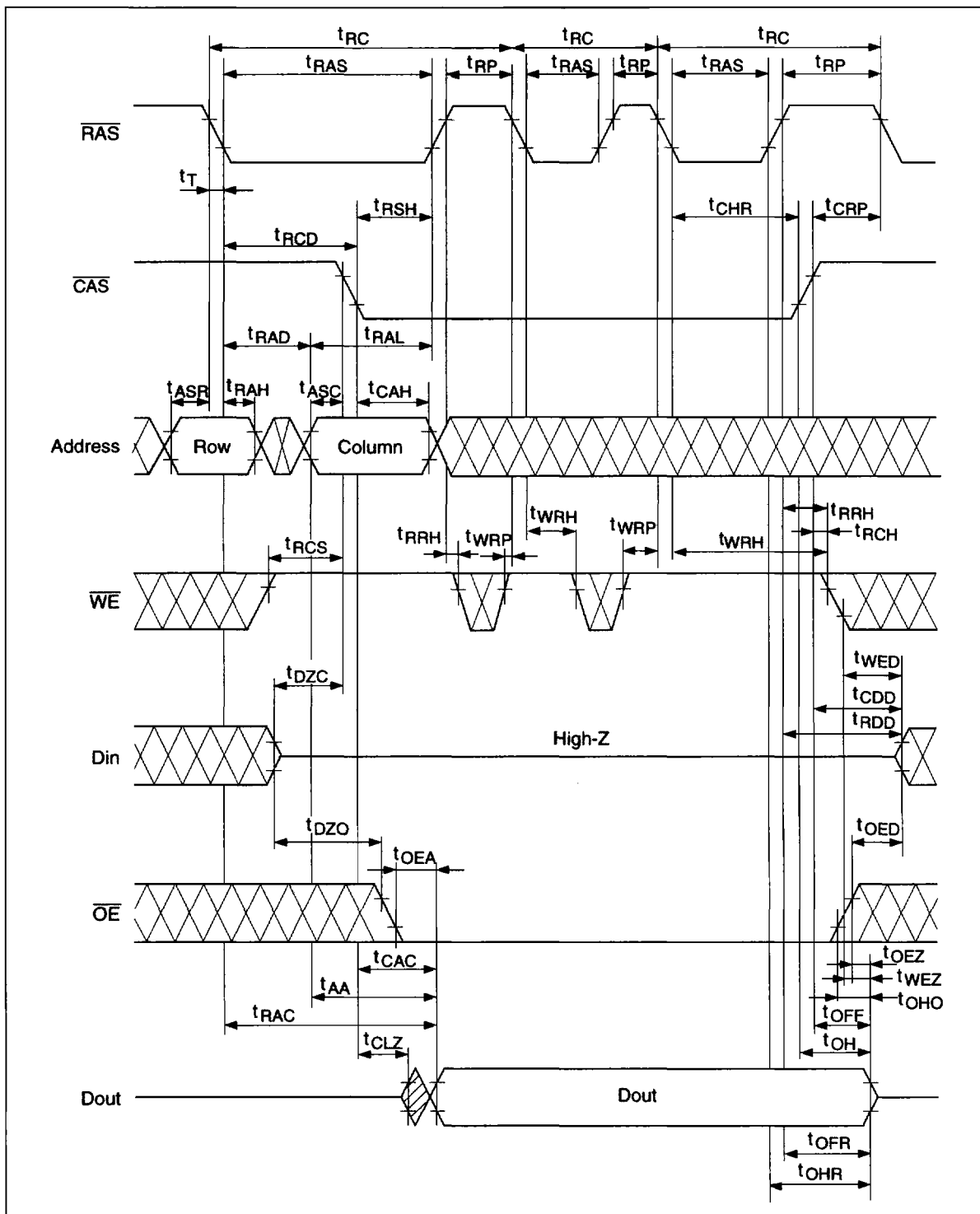
RAS-Only Refresh Cycle



$\overline{\text{CAS}}$ -Before- $\overline{\text{RAS}}$ Refresh Cycle

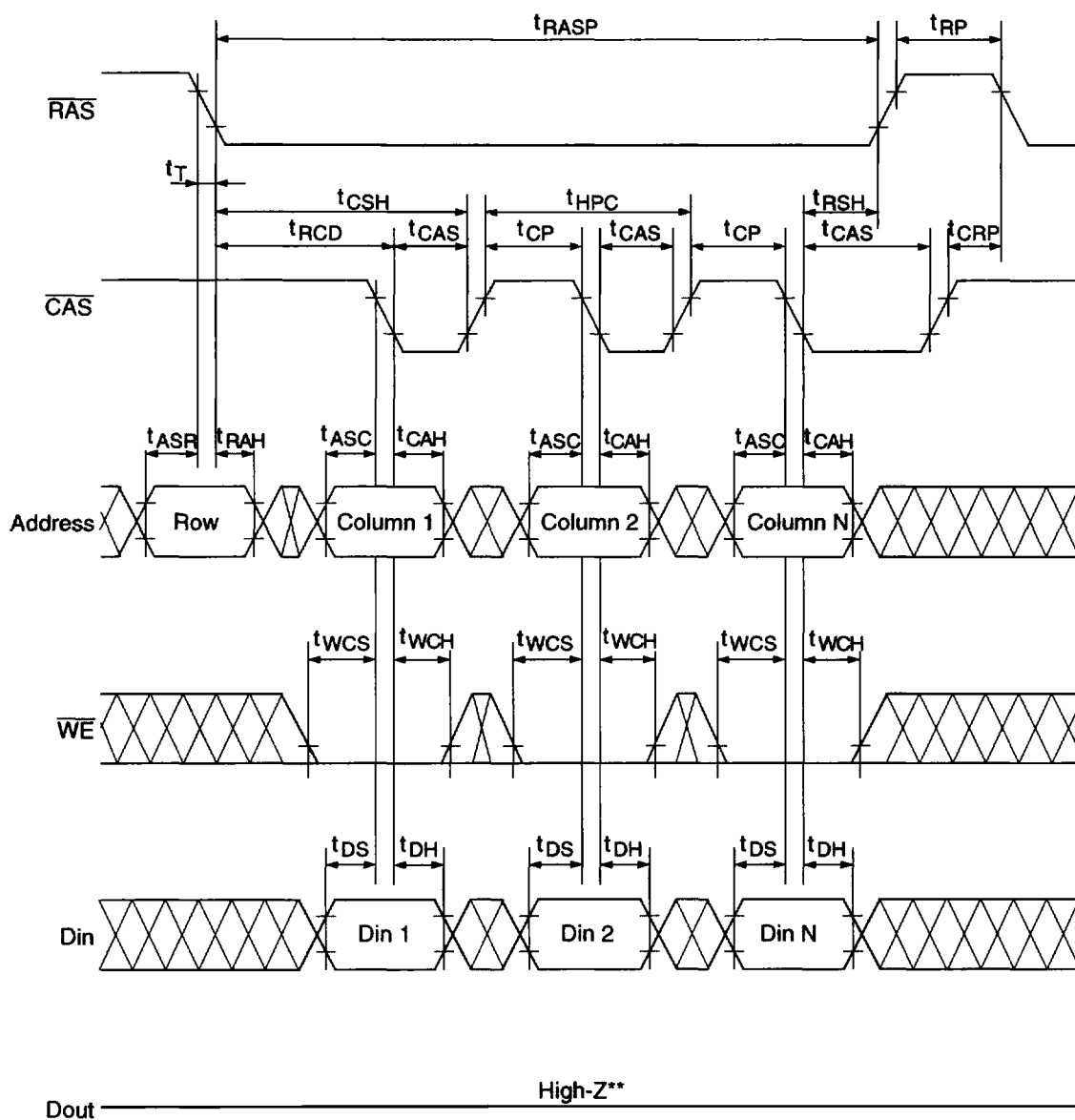


Hidden Refresh Cycle



HM5116405B Series, HM5117405B Series

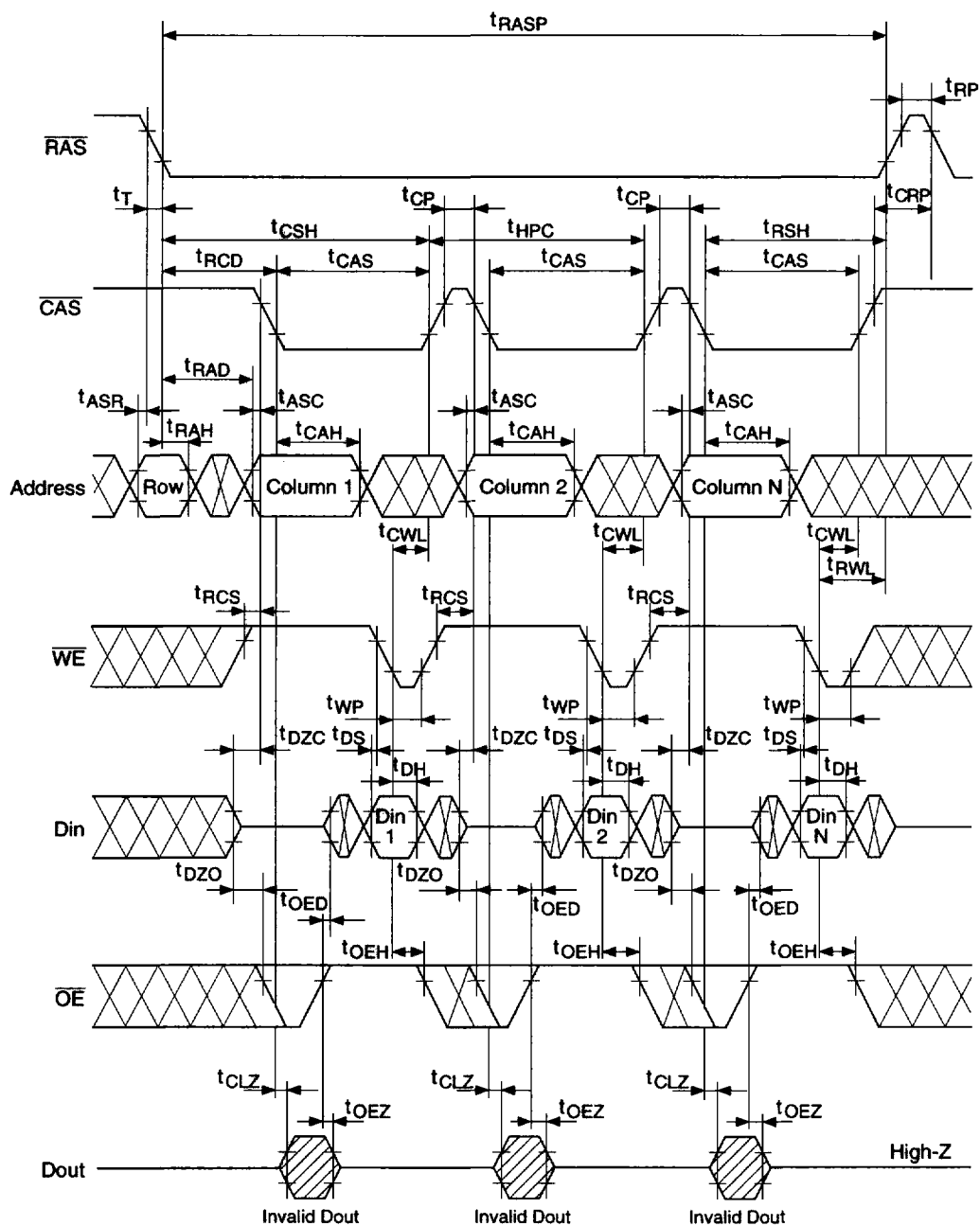
EDO Page Mode Early Write Cycle



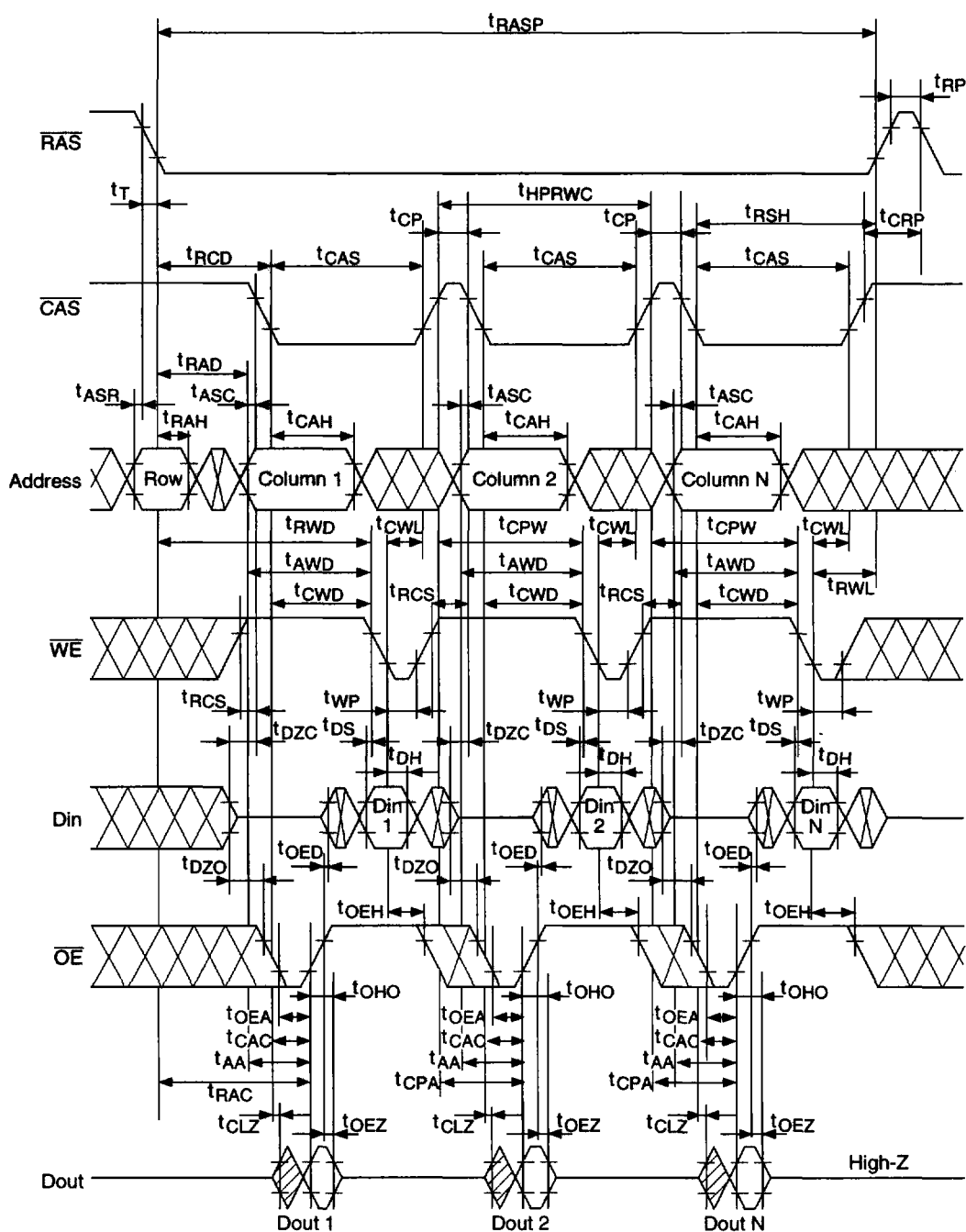
* $\overline{OE}$: H or L

** $t_{WCS} \geq t_{WCS}(\min)$

EDO Page Mode Delayed Write Cycle



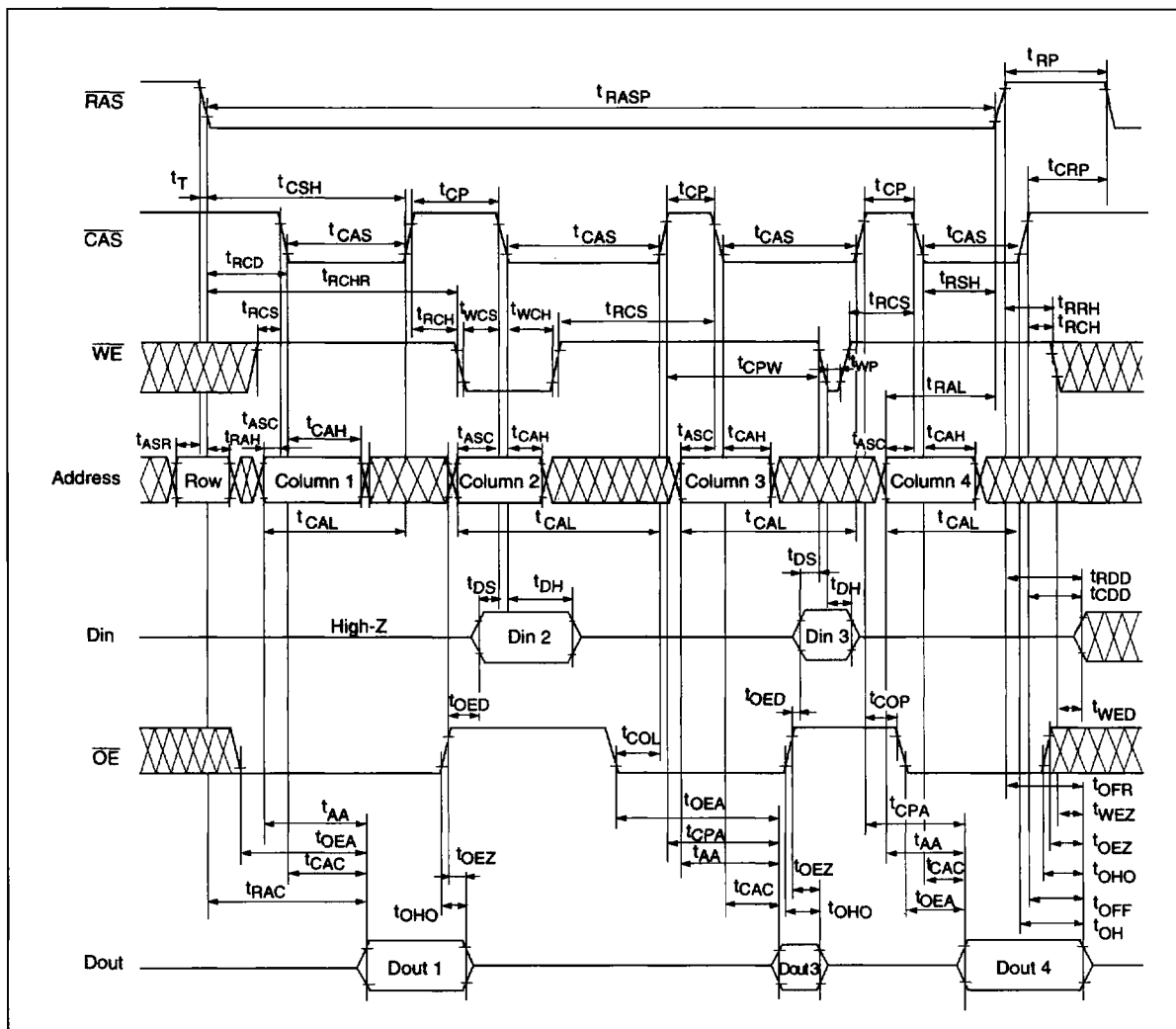
EDO Page Mode Read-Modify-Write Cycle



EDO Page Mode Mix Cycle (1)

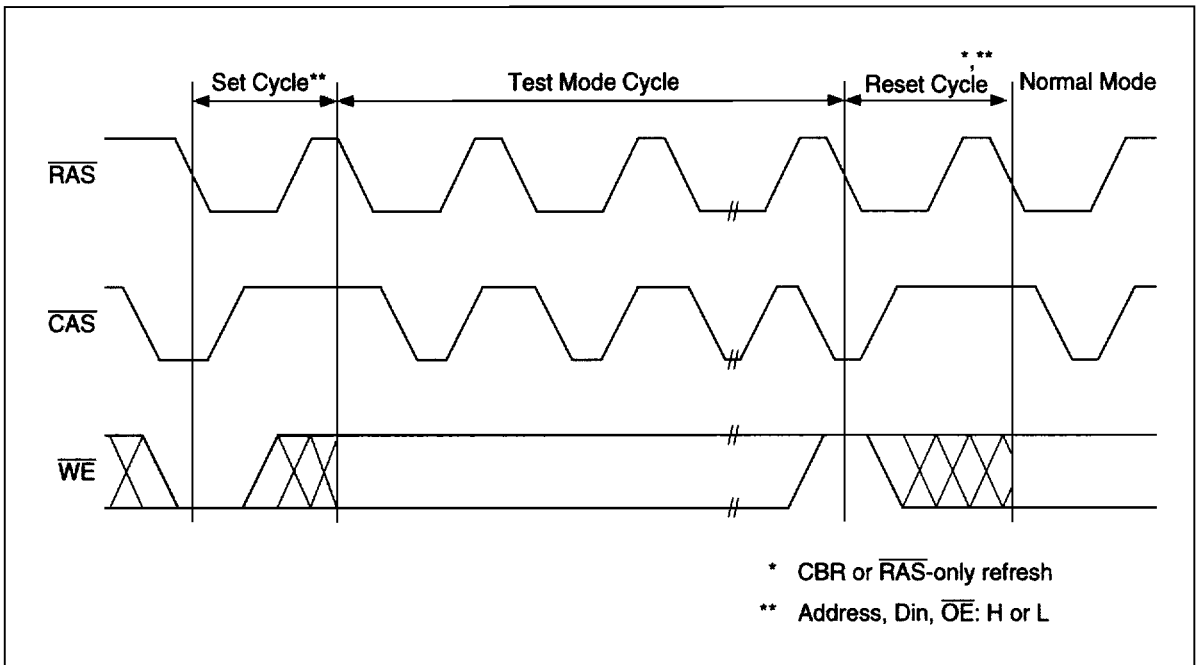


EDO Page Mode Mix Cycle (2)



HM5116405B Series, HM5117405B Series

Test Mode Cycle *¹⁸



HM5116405B Series, HM5117405B Series

Test Mode Set Cycle

