

ASIC PC Macro 16C550A Universal Asynchronous Receiver/Transmitter (UART) with Independent FIFO Buffers

Features

- Functionally compatible with 16C550A/16C450/16450 devices
- 2.7 V to 5.5 V operation ideal for portable operations
- Supported in AT&T's submicron CMOS and BiCMOS standard-cell libraries
 - High-speed HS900C
 - High-drive HD750BC
 - Low-power LP900C
- Verified models with vectors achieving 95% fault coverage
- Compatibility with *Logic Automation** models for system simulation
- Supported through AT&T ADS and third-party design kits
- Samples available for system evaluation
 - 40-pin DIP
- Unidirectional I/O buses to help ease simulation
- Soft macro (netlist) for simplified layout
- Independent 16-byte receive and transmit FIFOs for reduced interrupt overhead
- Programmable serial interface characteristics:
 - 5-, 6-, 7-, or 8-bit characters
 - 1, 1.5, or 2 stop-bit generation
 - Baud rate generation, dc to 256K baud

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Description

The 16C550A Universal Asynchronous Receiver/Transmitter (UART) with Independent FIFO Buffers is used for the receive and transmit functions. The macro is functionally identical to the FIFO-less 16450 UART at powerup and must be configured for 16C550A FIFO operation via the microprocessor interface. The macro supports full-duplex asynchronous modem and terminal communications. Modem status, error detection, and a fully programmable baud rate generator are standard features. The function includes two FIFO status outputs for signaling DMA transfers. A functional overview is illustrated in the block diagram.

To help ease system design, the AT&T 16C550A macro, coupled with standard pad drivers, meets I/O timing specifications for industry-standard 16C550A products. In addition, the AT&T 16C550A can be operated with V_{DD} at $3\text{ V} \pm 10\%$ for power-sensitive applications.

AT&T has performed extensive compatibility and system verification tests to help ensure conformance with industry-standard 16C550A devices.

With the 16C550A macro, designers can optimize their ASIC for performance or low power using AT&T's interchangeable CMOS and BiCMOS libraries. AT&T provides macro support files and test vectors for completing an ASIC design incorporating a 16C550A macro. For customer system verification, AT&T offers fully tested kit parts in 40-pin DIP packages.

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Description (continued)

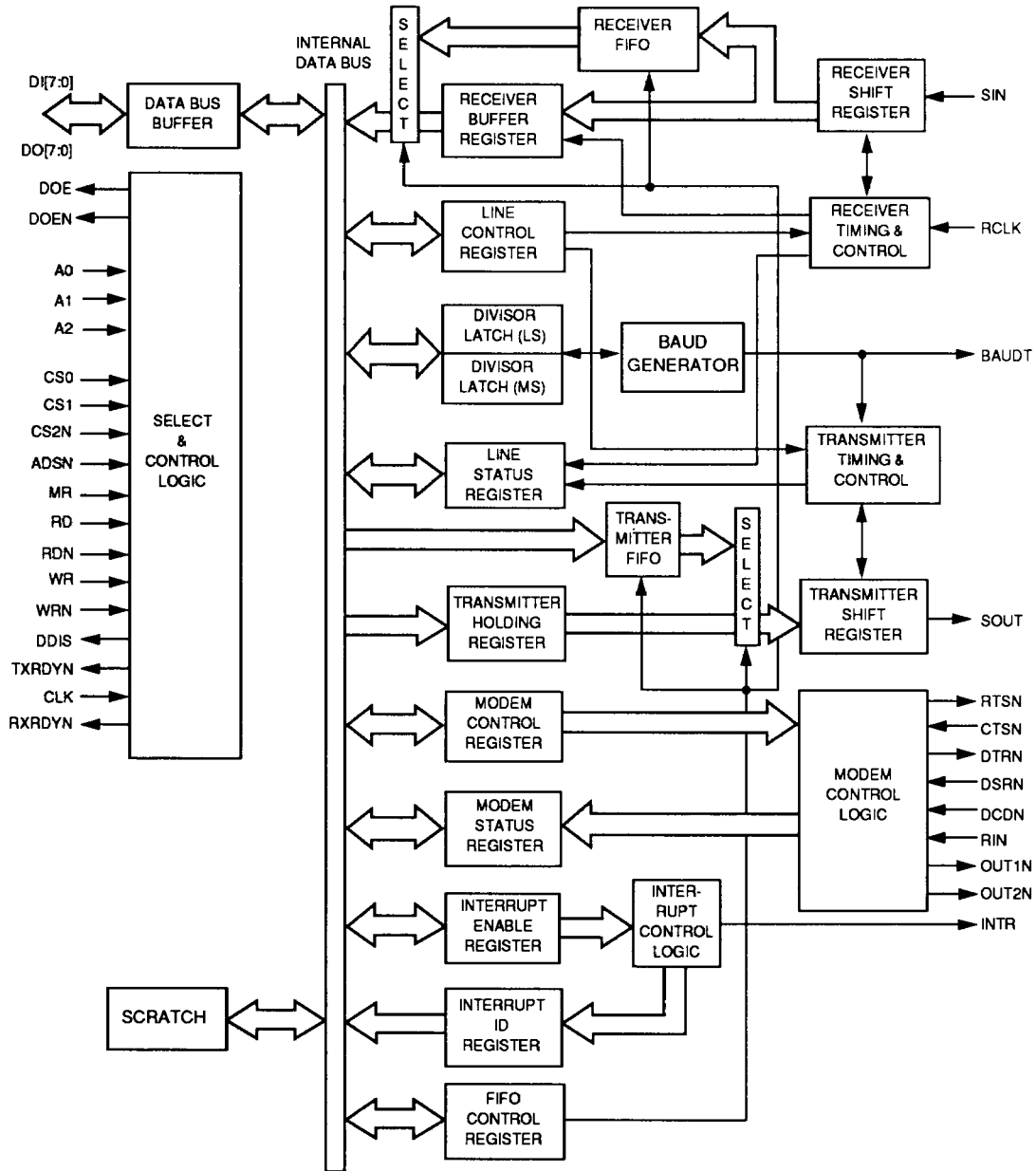


Figure 1. Functional Block Diagram

Pin Information

Table 1. Pin Descriptions

Symbol	Type	Name/Function
ADSN	I	Address Strobe (Active-Low).
CS[0:1]	I	Chip Select (Active-High).
CS2N	I	Chip Select (Active-Low).
CTSN	I	Clear to Send (Active-Low).
DSRN	I	Data Set Ready (Active-Low).
DCDN	I	Data Carrier Detect (Active-Low).
RIN	I	Ring Indicator (Active-Low).
WR	I	Write Strobe (Active-High).
WRN	I	Write Strobe (Active-Low).
RD	I	Read Strobe (Active-High).
RDN	I	Read Strobe (Active-Low).
RCLK	I	Receive Clock(↑↓).
SIN	I	Serial Input Data (Active-High).
MR	I	Master Reset (Active-High).
A[2:0]	I	Register Select (Active-High).
DI[7:0]	I	Data Input (Active-High).
CLK	I	Baud Rate Input Clock(↑↓).
OUT1N	O	User Designated Output 1 (Active-Low).
OUT2N	O	User Designated Output 2 (Active-Low).
DTRN	O	Data Terminal Ready (Active-Low).
RTSN	O	Request to Send (Active-Low).
SOUT	O	Serial Output Data (Active-High).
BAUDT	O	Baud Rate Clock (↑↓).
DDIS	O	Data Driver Disable (Active-High).
INTR	O	Interrupt (Active-High).
RXRDYN	O	Receiver Ready (Active-Low).
TXRDYN	O	Transmitter Ready (Active-Low).
DOE	O	Data Output Enable (Active-High).
DOEN	O	Data Output Enable (Active-Low).
DO[7:0]	O	Data Out (Active-High).

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Netlist Order

Inputs: ADSN, CS0, CS1, CS2N, CTSN, DSRN, DCDN, RIN, WR, WRN, RD, RDN, RCLK, SIN, MR, A2, A1, A0, DI7, DI6, DI5, DI4, DI3, DI2, DI1, DI0, CLK

Outputs: OUT1N, OUT2N, DTRN, RTSN, SOUT, BAUDT, DDIS, INTR, RXRDYN, TXRDYN, DOE, DOEN, DO7, DO6, DO5, DO4, DO3, DO2, DO1, DO0

Signal Loading/Signal Drive

Table 2. Input Signal Capacitance

Input Pin	Unit (pF)
ADSN	0.101
CS[0:1]	0.101
CS2N	0.101
CTSN	0.101
DSRN	0.101
DCDN	0.101
RIN	0.101
WR	0.101
WRN	0.101
RD	0.101
RDN	0.101
RCLK	0.101
SIN	0.103
MR	0.101
A[2:0]	0.179
DI[7:0]	0.101
CLK	0.101

Table 3. Output Signal Drive Capability

Output Signal	Driver Type
OUT1N	ND2
OUT2N	ND2
DTRN	ND2
RSTN	ND2
SDOUT	OR2
BAUDT	ND2
DDIS	INRB
INTR	INRB
RXRDYN	INRB
TXRDYN	INRB
DOE	INRB
DOEN	INRB
DO[7:0]	INRB

Timing Information

Table 4. Switching Characteristics

Measurements are preliminary. Performance optimized only.
 Time: V_{DD} = 4.5 V, T = 125 °C, WCS Processing

From Input	To Output	Load	Time	Unit
RD/RDN	DO[7:0]	1.8 pF	85	ns
RD/RDN	DOE/DOEN	2.3 pF	20	ns
RD/RDN	DDIS	0.6 pF	20	ns
XIN	BAUDT	0.7 pF	135	ns
WR/WRN (WR THR)	INTR↓	0.5 pF	135	ns
RD/RDN (RD MSR or RD IIR)	INTR↓	0.5 pF	210	ns
RD/RDN (RD RBR or RD LSR)	INTR↓	0.5 pF	1	μs
RD/RDN (RD RBR)	RXRDN↑	0.5 pF	250	ns
WR/WRN (WR THR)	TXRDN↑	0.7 pF	155	ns
CTSN	INTR↑	0.5 pF	210	ns
DSRN	INTR↑	0.5 pF	210	ns
DCDN	INTR↑	0.5 pF	210	ns
RIN	INTR↑	0.5 pF	210	ns
WR/WRN	DTRN	0.5 pF	160	ns
WR/WRN	RTSN	0.5 pF	160	ns
WR/WRN	OUT1N	0.5 pF	160	ns
WR/WRN	OUT2N	0.5 pF	160	ns

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Timing Information (continued)

Table 5. Input Timing Requirements

Measurements are preliminary. Performance optimized only.
 Setup Time: V_{DD} = 4.5 V, T = 125 °C, WCS Processing
 Hold Time: V_{DD} = 5.5 V, T = 0 °C, WCF Processing

Input Signal	Reference Clock	Setup Time	Hold Time	Unit
A[2:0] CS2N CS[1:0]	ADSN↑	60	0	ns
A[2:0] CS2N CS[1:0]	WR↑/WRN↓	30	—	ns
A[2:0] CS2N CS[1:0]	WR↓/WRN↑	—	20	ns
A[2:0] CS2N CS[1:0]	RD↑/RDN↓	30	—	ns
A[2:0] CS2N CS[1:0]	RD↓/RDN↑	—	20	ns
DI[7:0]	WR↓/WRN↑	30	30	ns

Table 6. Input Clock Requirements

Measurements are preliminary. Performance optimized only.

Input Clock	Min Period	Duty Cycle		Unit
		Min. High	Min. Low	
CLK	125	55	55	ns
RCLK	250	110	110	ns
ADSN	280	—	60	ns
RD/RDN	280	125	125	ns
WR/WRN	280	100	100	ns
RIN	—	1.5	3	s
MR	—	5	—	μs

Timing Information (continued)

Table 7. Clock Dependent Output Delays

Measurements are preliminary. Performance optimized only.

From Event/Signal	To Event/Signal	Notes	Min	Max	Units
RCLK↑	SIN Sampled	—	—	2	μs
Stop Bit Sampled	INTR↑/ RXRDYN↓	Non-FIFO Mode	—	1	RCLK Cycles
Stop Bit Sampled	INTR↑/ RXRDYN↓	FIFO Mode	—	3	RCLK Cycles
Stop Bit Sampled	INTR↑	Timeout	—	8	RCLK Cycles
Interrupt Cleared	SOUT↓ Start Bit	—	8	24	BAUDT Cycles
WR↓/WRN↑ (WR THR) Initial Write	INTR↑	—	16	24	BAUDT Cycles
Stop Bit Transmitted	INTR↑	—	8	8	BAUDT Cycles
Start Bit Transmitted	TXRDYN↓	—	—	8	BAUDT Cycles

Application Information

Design Information

The 16C550A macro was designed to meet the standard part in all aspects of operation. The user is referred to National Semiconductor's data communications handbook for waveforms that correctly interface with the part. General functions of the 16C550A include the following:

- Powerup reset places the macro in 16450 mode
- Full asynchronous serial interfaces with programmable start, stop, and parity bits
- Hold and shift registers in 16450 mode for CPU decoupling
- Independent programmable interrupts for transmit, receive, line status, and data set functions
- Programmable baud rate generator divides input clock by 1 through $2^{16} - 1$ to produce an output clock that is 16 times the transmission baud rate
- Separate receiver clock input can use the baud rate generator output or an independent clock source
- Modem control functions:
 - Clear to send
 - Request to send
 - Data set ready
 - Data terminal ready
 - Ring indicator
 - Data carrier detect
- False start-bit detection
- Break detection and generation
- Internal loopback test capability

Application Information (continued)

Bidirectional Pins

The 16C550A macro is designed to be used in systems with split input and output data buses. If it is used in this manner, the output signals DOE and DOEN are not used. If the application using the 16C550A has a bidirectional bus, DI[7:0] and DO[7:0] can be tied to the bidirectional bus by using TBUS cells from the interchangeable CMOS and BiCMOS libraries.

Fault Coverage

To ensure adequate fault coverage, a vector set consisting of approximately 65,000 vectors is available. To guarantee necessary controllability and observability for these vectors to be effective, all primary inputs, the data bus, and primary outputs should be directly accessible by external input or output pins. This can be done by multiplexing existing pins if no spares are available.

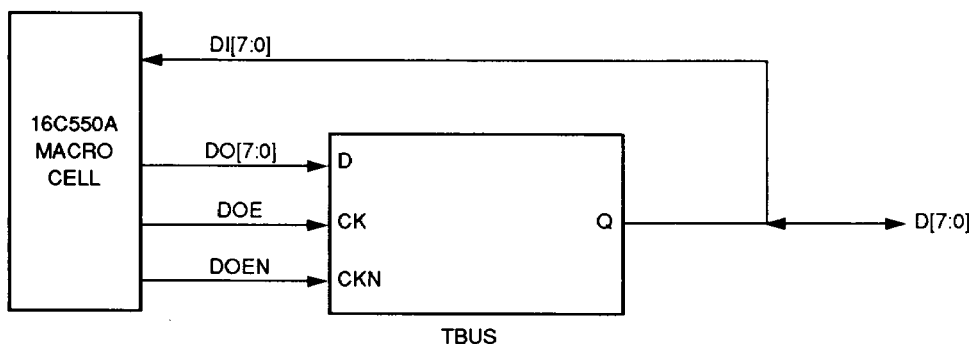


Figure 2. Connecting the 16C550A to a Bidirectional Bus

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