HARRIS

HI-5690V/95V/97V

High Speed, 12-Bit Low Cost Monolithic Digital-to-Analog Converter

Features

- Voltage Output with Fast Settling 750ns
  High Slew Rate 50V/μs
- Industry Standard Pinout - AD-DAC 80 & HI-5680 Compatible
- Two-Supply Operation .... 11.4V to 16.5V
  -11.4V to -16.5V
- Low Noise Voltage Reference
  1/f (0.1Hz to 10Hz) .... $15\mu V_{p-p}$
- Guaranteed Monotonic Over Full Temperature Range
- Application Resistors On-Chip
- Complementary Binary Input Code
- Voltage Output
- Complete Family of Temperature Grades

Applications

- High Speed A/D Converters
- Precision Instrumentation
- CRT Display Generation

Description

The HI-5690V series of complete 12 bit digital to analog converters includes a low noise, low temperature coefficient buried zener reference and a fast settling output amplifier. The series consists of the HI-5690V, -5695V and -5697V, for the commercial, industrial and military temperature ranges. Monolithic construction along with several design innovations make these converters an optimum choice for high speed, high reliability applications.

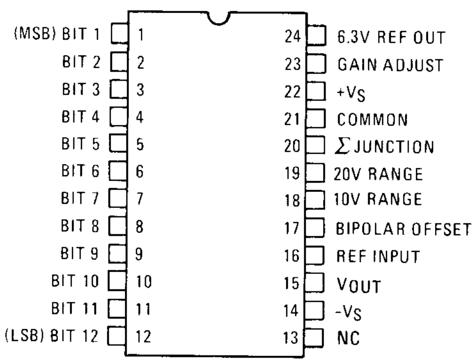
The Harris unique Dielectric Isolation (DI) processing reduces internal parasitics, resulting in fast switching times and minimum glitch. Wafer-level laser trimming of span resistors and bit current cells ensures high accuracy and exceptional tracking over temperature.

Internally, the HI-5690V series eliminates code dependent ground currents by routing current from the positive supply to the internal ground node, as determined by an auxiliary R-2R ladder. This results in a cancellation of code dependent ground currents, allowing virtually zero variation in current through the package common, thus minimizing analog ground noise seen by the converter.

The HI-5690V series operates from two supplies $\pm V_S$ in the range of ±11.4 Volts to ±16.5 volts. It is pin compatible with the AD-DAC 80 series and HI-5680 series, and since Pin 13 is not internally connected (Logic supply on standard 5680's) this device is compatible in applications with or without +5 Volts applied to Pin 13. The converter performance is guaranteed over the full power supply operating range, but not all output ranges are available with low supply voltages. The package is a 24 pin Ceramic Sidebrazed DIP. For Mil-Std-883 compliant parts, request the HI-5697V/883 data sheet.

Pinouts

DIP
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Proper IC handling procedures should be followed.

Absolute Maximum Ratings (Note 1)

Power Supply Inputs +Vs .... +20V
-Vs .... -20V

Reference
Input (pin 16) +Vs
Output can be shorted to common or either supply
Analog output can be shorted to common or either supply. (Note 2)

Digital Inputs
Bits 1 to 12 .... -1V to +12V

Junction Temperature .... 175°C

Operating Temperature Range

HI-5690V-5 .... 0°C to +75°C
HI-5695V-4 .... -25°C to +85°C
HI-5697V-2 .... -55°C to +125°C
HI-5697V/883 .... See Separate Data Sheet
Storage Temperature Range .... -65°C to +150°C

Electrical Specifications

(T_A = +25°C, V_S = ±15V. Pin 16 connected to Pin 24, unless otherwise noted. R_L = 2kΩ)

PARAMETER	HI-5690V, HI-5695V, and HI-5697V				
	CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL INPUT (Note 3)					
Resolution				12	Bits
Logic Levels	TTL Compatible				
Logic '1'	+1μA	+2		+5.5	Volts
Logic '0'	-100μA	0		+0.8	Volts
Input Currents					
I_{IH}	+2V			+1	μA
I_{IL}	+0.8V			-100	μA
ACCURACY (Note 3)					
Linearity Error All grades	+25°C		±3/16	±1/2	LSB
HI-5690V, HI-5695V			±1/5	±1/2	LSB
HI-5697V			±1/4	±3/4	LSB
Differential Linearity Error					
HI-5690V, HI-5695V			±1/5	±3/4	LSB
HI-5697V			±1/4	±1	LSB
Monotonicity		Guaranteed			
Gain Error (Note 4)					
HI-5690	+25°C		±0.05	±0.30	%FSR (5)
HI-5695V, HI-5697V	+25°C		±0.05	±0.20	%FSR
Offset Error (Note 4)					
HI-5690V	+25°C		±0.02	±0.15	%FSR
HI-5695V, HI-5697V	+25°C		±0.02	±0.10	%FSR
THERMAL DRIFT (Note 3)					
Total Bipolar Drift (Includes gain, offset & linearity drifts.)					
HI-5690V			±15	±25	ppm/°C
HI-5695V			±10	±20	ppm/°C
HI-5697V			±15	±30	ppm/°C
Gain					
HI-5690V			±10	±30	ppm/°C
HI-5695V, HI-5697V			±8	±20	ppm/°C

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
	HI-5690V, HI-5695V, and HI-5697V				
Unipolar Offset			±1.5	±4	ppm/°C
Bipolar Offset			±5	±15	ppm/°C
Total Error (Note 6)					
Unipolar					
HI-5690V			±0.08	±0.17	%FSR
HI-5695V			±0.10	±0.20	%FSR
HI-5697V			±0.13	±0.30	%FSR
Bipolar					
HI-5690V			±0.06	±0.12	%FSR
HI-5695V			±0.09	±0.12	%FSR
HI-5697V			±0.12	±0.30	%FSR
CONVERSION SPEED (Note 3)					
Settling Time (Note 3)	to ±0.01% of FSR for FSR Change				
With 10kΩ Feedback	FSR = 20V; ±15V Supplies		0.9	1.5	μs
With 5kΩ Feedback	FSR = 10V		0.75	1.2	μs
For 1 LSB change	Major Carry		0.50		μs
Slew Rate			50		V/μs
ANALOG OUTPUT					
Output Current		±5	0.05		mA
Output Resistance	DC				Ω
INTERNAL REFERENCE					
Output Voltage		+6.250	+6.3	+6.350	V
Output Resistance	DC		1.5		Ω
External Current				+2.5	mA
Reference Drift			±5	±20	ppm/°C
Output Noise at +25°C					
Wideband	10Hz to 10kHz		12.5		μVrms
Low Frequency	0.1Hz to 10Hz		15		μVp-p
POWER SUPPLY SENSITIVITY (Note 3)					
+Vs (Pin 22)			0.0008	0.002	%FSR/%Vs
-Vs (Pin 14)			0.001	0.002	%FSR/%Vs
POWER SUPPLY REQUIREMENT (Note 7)					
Range					
+Vs (Pin 22)		+11.4	+15	+16.5	V
-Vs (Pin 14)		-11.4	-15	-16.5	V
Current					
+Vs (Pin 22)	≤ +15V		18.5	22	mA
-Vs (Pin 14)	≥ -15V		-20.5	-26	mA
Pin 13 (No Connection)			0		mA

NOTES: 1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.

2. The output is designed to withstand a temporary short to common or either supply for at least one minute.

3. See definitions.

4. Adjustable to zero using external potentiometers.

5. FSR is "Full Scale Range" and is equal to the full scale output voltage minus the zero scale output voltage (i.e. 20V for ±10V range, 10V for ±5V range, etc.)

6. With gain and offset errors adjusted to zero at 25°C.

7. The HI-569XV series will operate with supply voltages as low as ±11.4V. It is recommended that output voltage range -10V to +10V not be used if the supply voltages are less than ±13V.

Digital Inputs

The HI-5690V series accepts digital input codes in complementary binary, complementary offset binary, and complementary two's complement binary.

DIGITAL INPUT	ANALOG OUTPUT		
	COMPLEMENTARY BINARY	COMPLEMENTARY OFFSET BINARY	COMPLEMENTARY TWO's COMPLEMENT*
MSB LSB			
000....000	+Full Scale	+Full Scale	-LSB
100....000	Mid Scale -1 LSB	-1 LSB	+Full Scale
111....111	Zero	-Full Scale	Zero
011....111	+1/2 Full Scale	Zero	-Full Scale

*Invert MSB with external inverter to obtain CTC Coding

Settling Time

That interval between application of a digital step input, and final entry of the analog output within a specified window about the settled value. Harris Semiconductor usually specifies a unipolar 10V full scale step, to be measured from 50% of the input digital transition, and a window of ±1/2 LSB about the final value. The device output is then rated according to the worst (longest settling) case: low to high, or high to low. In a 12 bit system ±1/2 LSB = ±0.012% of FSR.

Thermal Drift

Thermal drift is based on measurements at +25°C, at high (T_H) and low (T_L) temperatures. Drift calculations are made for the high (T_H-25°C) and low (+25°C-T_L) ranges, and the larger of the two values is given as a specification representing worstcase drift.

Gain Drift, Offset Drift, Reference Drift and Total Bipolar Drift are calculated in parts per million per °C as follows:

$$\text{Gain Drift} = \frac{\Delta FSR/\Delta^{o}C}{FSR} \times 10^6$$

$$\text{Offset Drift} = \frac{\Delta Offset/\Delta^{o}C}{FSR} \times 10^6$$

$$\text{Reference Drift} = \frac{\Delta V_{REF}/\Delta^{o}C}{V_{REF}} \times 10^6$$

$$\text{Total Bipolar Drift} = \frac{\Delta V_O/\Delta^{o}C}{FSR} \times 10^6$$

NOTE: FSR = Full Scale Output Voltage - Zero Scale Output Voltage

$\Delta FSR = FSR(T_H) - FSR(+25^{o}C)$ or $FSR(+25^{o}C) - FSR(T_L)$

V_O = Steady-state response to any input code.

Total Bipolar Drift is the variation of output voltage with temperature, in the bipolar mode of operation. It represents the net effect of drift in Gain, Offset, Linearity and Reference Voltage. Total Bipolar Drift values are calculated, based on measurements as explained above. Gain and Offset need not be calibrated to zero at +25°C. The specified limits for TBD apply for any input code and for any power supply setting within the specified operating range.

Accuracy

LINEARITY ERROR (Short for "Integral Linearity Error". Also, sometimes called "Integral Nonlinearity" and "Nonlinearity".) - The maximum deviation of the actual transfer characteristic from an ideal straight line. The ideal line is positioned according to end-point linearity for D/A converter products from Harris Semiconductor, i.e. the line is drawn between the end-points of the actual transfer characteristic (codes 00...0 and 11...1).

DIFFERENTIAL LINEARITY ERROR - The difference between one LSB and the output voltage change corresponding to any two consecutive codes. A Differential Nonlinearity of ±1 LSB or less guarantees monotonicity.

MONOTONICITY - The property of a D/A converter's transfer function which guarantees that the output derivative will not change sign in response to a sequence of increasing (or decreasing) input codes. That is, the only output response to a code change is to remain constant, increase for increasing code, or decrease for decreasing code.

TOTAL ERROR - The net output error resulting from all internal effects (primarily non-ideal Gain, Offset, Linearity and Reference Voltage). Supply voltages may be set to any values within the specified operating range. Gain and offset errors must be calibrated to zero at +25°C. Then the specified limits for Total Error apply for any input code and for any temperature within the specified operating range.

Power Supply Sensitivity

Power Supply Sensitivity is a measure of the change in gain and offset of the D/A converter resulting from a change in -Vs, or +Vs supplies. It is specified under DC conditions and expressed as full scale range percent of change divided by power supply percent change.

$$P.S.S. = \frac{\dfrac{\Delta \text{ Full Scale Range} \times 100}{\text{Full Scale Range (Nominal)}}}{\dfrac{\Delta V_S \times 100}{V_S \text{ (Nominal)}}}$$

Glitch

A glitch on the output of a D/A converter is a transient spike resulting from unequal internal ON-OFF switching times. Worst case glitches usually occur at half-scale, i.e. the major carry code transition from 011...1 to 100...0 or vice versa. For example, if turn ON is greater than OFF for 011...1 to 100...0, an intermediate state of 000...0 exists, such that, the output momentarily glitches toward zero output. Matched switching times and fast switching will reduce glitches considerably. (Measured as one half the product of duration and amplitude.)

Decoupling and Grounding

For best accuracy and high frequency performance, the grounding and decoupling scheme shown in Figure 1 should be used. Decoupling capacitors should be connected close to the HI-569XV (preferably to the device pins) and should be tantalum or electrolytic bypassed with ceramic types for best high frequency noise rejection.

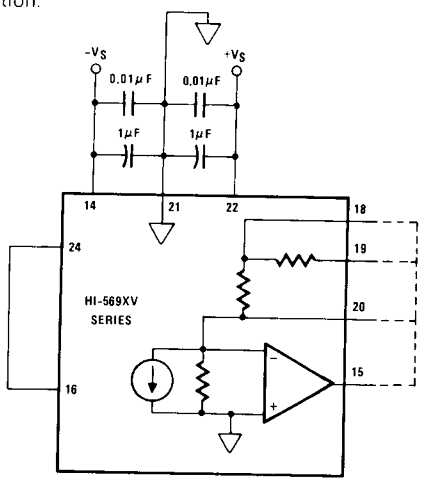


FIGURE 1.

Reference Supply

An internal 6.3 Volt reference is provided on board all HI-569XV models. This voltage (pin 24) is accurate to ±0.8% and must be connected to the reference input (pin 16) for specified operation. This reference may be used externally, provided current drain is limited to 2.5mA. An exteral buffer amplifier is recommended if this reference is to be used to drive other system components. Otherwise, variations in the load driven by the reference will result in gain variations of the HI-569XV. All gain adjustments should be made under constant load conditions.

Output Voltage Ranges

HI-569XV

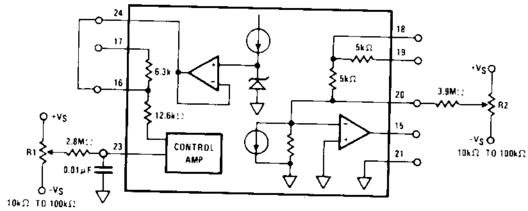


FIGURE 2.

RANGE CONNECTIONS

	RANGE	CONNECT PIN 15	PIN 17	PIN 19
Unipolar	0 to +5V	18	N.C.	20
	0 to +10V	18	N.C.	N.C.
Bipolar	±2.5V	18	20	20
	±2.5V	18	20	N.C.
	±10V	19	20	15

Gain and Offset Calibration

UNIPOLAR CALIBRATION

Step 1: Offset
Turn all bits OFF (11...1)
Adjust R_2 for zero volts out

Step 2: Gain
Turn all bits ON (00...0)
Adjust R_1 for FS-1LSB
That is:
4.9988 for 0 to +5V range
9.9976 for 0 to +10V range

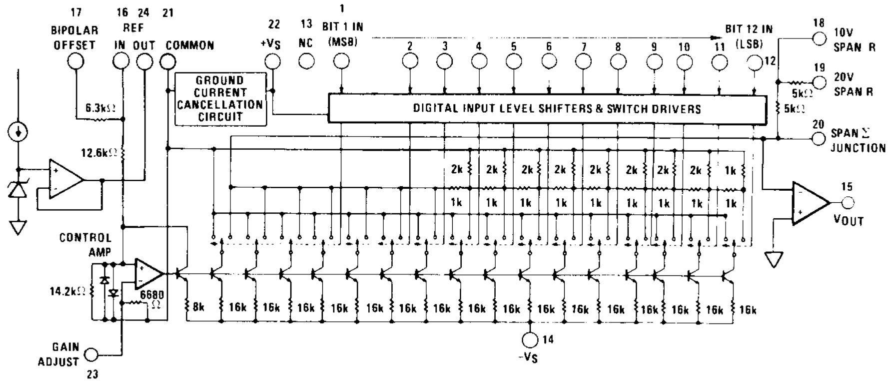
BIPOLAR CALIBRATION

Step 1: Offset
Turn all bits OFF (11...1)
Adjust R2 for Negative FS
That Is:
-10V for ±10V range
-5V for ±5V range
-2.5V for ±2.5 range

Step 2: Gain
Turn all bits ON (00...0)
Adjust R1 for positive FS-1LSB
That is:
+9.9951V for ±10V range
+4.9976V for ±5V range
+2.4988V for ±2.5V range

This Bipolar procedure adjusts the output range end points. The maximum error at zero (half scale) will not exceed the Linearity error. See the "Accuracy" specifications.

Functional Block Diagram



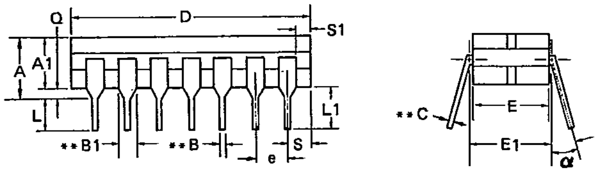
Die & Package Characteristics

Transistor Count	280
Die Size	219 x 123 mils
Thermal Impedance;	
θ_{ja}	49°C/W
θ_{jc}	12°C/W
Tie Substrate to:	Ground
Process	Bipolar-DI

Package Configuration

T-90-20

A B C D E .300 CERAMIC DUAL-IN-LINE

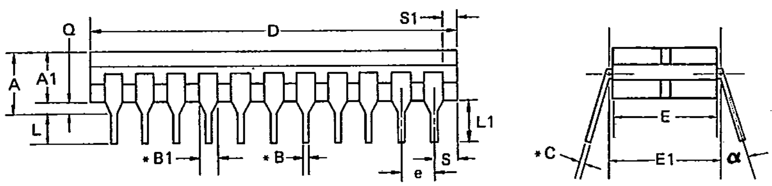


PKG. CODE	LEAD COUNT	DIM. A	DIM. A1	DIM. B	DIM. B1	DIM. C	DIM. D	DIM. E	DIM. E1	DIM. e	DIM. L	DIM. L1	DIM. S	DIM. S1	DIM. Q	DIM. α
A	8 / SSI	— / .200	.140 / .160	.016 / .023	.050 / .065	.008 / .015	.375 / .395	.245 / .265	.290 / .310	.100 / BSC	.125 / .150	.150 / —	— / .055	.005 / —	.015 / .060	0° / 15°
B1	14 / MSI	— / .200	.140 / .170	.016 / .023	.050 / .065	.008 / .015	.753 / .785	.265 / .285	.290 / .310	.100 / BSC	.125 / .180	.150 / —	— / .098	.005 / —	.015 / .060	0° / 15°
B2	14 / LSI	— / .200	.140 / .170	.016 / .023	.050 / .065	.008 / .015	.753 / .785	.285 / .305	.300 / .320	.100 / BSC	.125 / .180	.150 / —	— / .098	.005 / —	.015 / .060	0° / 15°
C1	16* / MSI	— / .200	.140 / .170	.016 / .023	.050* / .065*	.008 / .015	.753 / .785	.265 / .285	.290 / .310	.100 / BSC	.125 / .180	.150 / —	— / .080	.005 / —	.015 / .060	0° / 15°
C2	16* / LSI	— / .200	.140 / .170	.016 / .023	.050* / .065*	.008 / .015	.753 / .785	.285 / .305	.300 / .320	.100 / BSC	.125 / .180	.150 / —	— / .080	.005 / —	.015 / .060	0° / 15°
D	18 / LSI	— / .200	.140 / .170	.016 / .023	.050* / .065*	.008 / .015	.882 / .915	.285 / .305	.300 / .320	.100 / BSC	.125 / .180	.150 / —	— / .098	.005 / —	.015 / .060	0° / 15°
E	20 / LSI	— / .200	.140 / .170	.016 / .023	.050* / .065*	.008 / .015	.940 / .970	.285 / .305	.300 / .320	.100 / BSC	.125 / .180	.150 / —	— / .080	.005 / —	.015 / .060	0° / 15°

* End leads are half leads where B remains the same and B1 is 0.035 / 0.045
** Solder dip finish add +0.003 inches

F .400 CERAMIC DUAL-IN-LINE

G H .600 CERAMIC DUAL-IN-LINE



PKG. CODE	LEAD COUNT	DIM. A	DIM. A1	DIM. B	DIM. B1	DIM. C	DIM. D	DIM. E	DIM. E1	DIM. e	DIM. L	DIM. L1	DIM. S	DIM. S1	DIM. Q	DIM. α
F .400	22 / LSI	— / .225	.150 / .180	.016 / .023	.050 / .065	.008 / .015	1.055 / 1.085	.375 / .395	.395 / .415	.100 / BSC	.125 / .180	.150 / —	— / .080	.005 / —	.015 / .060	0° / 15°
G .600	24 / LSI	— / .225	.150 / .180	.016 / .023	.050 / .065	.008 / .015	1.24 / 1.27	.515 / .535	.595 / .615	.100 / BSC	.125 / .180	.150 / —	— / .098	.005 / —	.015 / .060	0° / 15°
H .600	28 / LSI	— / .225	.160 / .190	.016 / .023	.050 / .065	.008 / .015	1.44 / 1.47	.515 / .535	.595 / .615	.100 / BSC	.125 / .180	.150 / —	— / .098	.005 / —	.015 / .060	0° / 15°

* Solder dip finish add +0.003 inches.

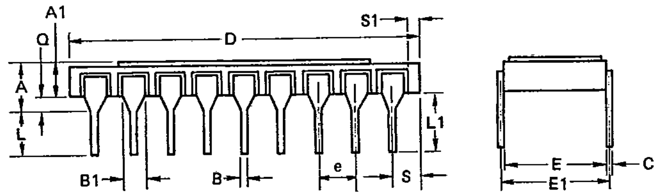
NOTE: Dimensions are Min / Max. Dimensions are in inches.

BSC means basic spacing between centerlines.

Package Configuration

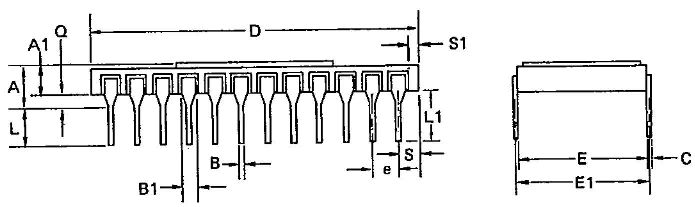
T-90-20

I .300 SIDEBRAZE DUAL-IN-LINE



PKG. CODE	LEAD COUNT	DIM. A	DIM. A1	DIM. B	DIM. B1	DIM. C	DIM. D	DIM. E	DIM. E1	DIM. e	DIM. L	DIM. L1	DIM. S	DIM. S1	DIM. Q
I	18	—/.200	.080/.110	.016/.023	.045/.060	.008/.015	.890/.910	.280/.300	.290/.310	.100/BSC	.125/.180	.150/—	—/.098	.005/—	.025/.045

J K L .600 SIDEBRAZE DUAL-IN-LINE



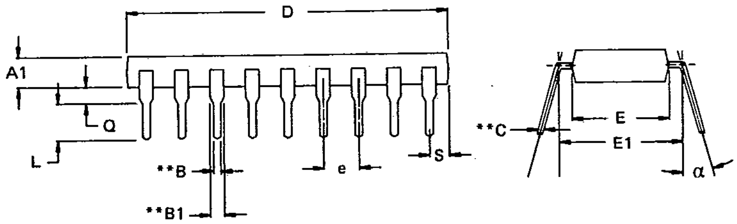
PKG. CODE	LEAD COUNT	DIM. A	DIM. A1	DIM. B	DIM. B1	DIM. C	DIM. D	DIM. E	DIM. E1	DIM. e	DIM. L	DIM. L1	DIM. S	DIM. S1	DIM. Q
J	24	—/.225	.080/.110	.016/.023	.040/.054	.008/.015	1.185/1.215	.587/.603	.598/.612	.100/BSC	.125/.180	.150/—	—/.080	.005/—	.040/.060
K	28	—/.225	.080/.110	.016/.023	.040/.054	.008/.015	1.385/1.415	.587/.603	.598/.612	.100/BSC	.125/.180	.150/—	—/.080	.005/—	.030/.060
L	40	—/.225	.080/.110	.016/.023	.040/.054	.008/.015	1.980/2.020	.587/.603	.598/.612	.100/BSC	.125/.180	.150/—	—/.080	.005/—	.040/.060

NOTE: Dimensions are $\frac{\text{Min}}{\text{Max}}$. Dimensions are in inches.

BSC means basic spacing between centerlines.

Package Configuration

M N O P Q .300 PLASTIC DUAL-IN-LINE

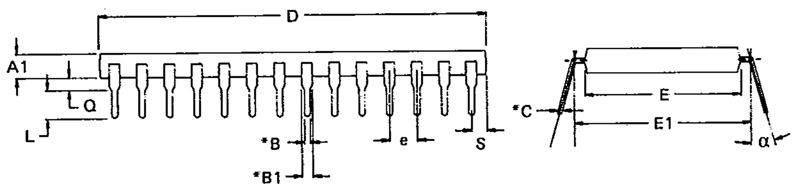


PKG. CODE	LEAD COUNT	DIM. A1	DIM. B	DIM. B1	DIM. C	DIM. D	DIM. E	DIM. E1	DIM. e	DIM. L	DIM. S	DIM. Q	DIM. α
M	8	.125/.140	.016/.023	.050/.070	.008/.015	.370/.390	.245/.265	.290/.310	.090/.110	.110/.150	.030/.050	.020/.040	0°/15°
N	14	.125/.140	.016/.023	.050/.070	.008/.015	.750/.770	.245/.265	.290/.310	.090/.110	.110/.150	.030/.050	.020/.040	0°/15°
O	16*	.125/.140	.016/.023	.050/.070	.008/.015	.750/.770	.245/.265	.290/.310	.090/.110	.110/.150	.025/.035	.020/.040	0°/15°
P	18	.125/.140	.016/.023	.050/.070	.008/.015	.900/.920	.245/.265	.290/.310	.090/.110	.110/.150	.040/.060	.020/.040	0°/15°
Q	20	.130/.145	.016/.023	.050/.070	.008/.015	1.030/1.050	.250/.270	.290/.310	.090/.110	.110/.150	.060/.080	.020/.040	0°/15°

* End leads are half leads where B remains the same and B1 is $\frac{0.035}{0.045}$

** Solder dip finish add 0.003 inches.

R S .600 PLASTIC DUAL-IN-LINE



PKG. CODE	LEAD COUNT	DIM. A1	DIM. B	DIM. B1	DIM. C	DIM. D	DIM. E	DIM. E1	DIM. e	DIM. L	DIM. S	DIM. Q	DIM. α
R	24	.145/.155	.016/.023	.050/.070	.008/.015	1.24/1.26	.540/.560	.590/.610	.090/.110	.110/.150	.045/.095	.020/.040	0°/15°
S	28	.145/.155	.016/.023	.050/.070	.008/.015	1.54/1.57	.540/.560	.590/.610	.090/.110	.110/.150	.110/.160	.020/.040	0°/15°

* Solder dip finish add 0.003 inches.

NOTE: Dimensions are $\frac{\text{Min}}{\text{Max}}$. Dimensions are in inches.

BSC means basic spacing between centerlines.

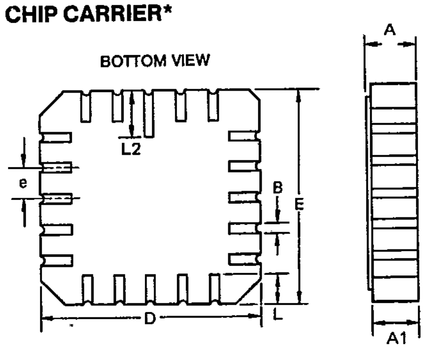
Package Configuration

T .350 CERAMIC LEADLESS CHIP CARRIER*

U .450 CERAMIC LEADLESS CHIP CARRIER*

V .650 CERAMIC LEADLESS CHIP CARRIER*

BOTTOM VIEW



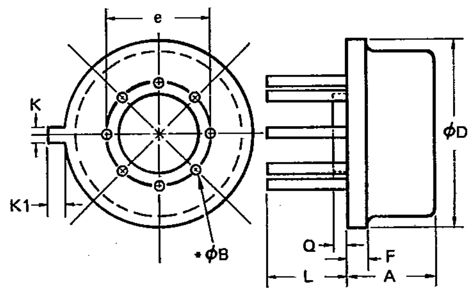
PKG. CODE	LEAD COUNT	DIM. A	DIM. A1	DIM. B	DIM. D	DIM. E	DIM. e	DIM. L	DIM. L2
T	20 / .350 SQ	.073 / .089	.063 / .077	.022 / .028	.342 / .358	.342 / .358	.050 / BSC	.045 / .055	.075 / .095
U	28 / .450 SQ	.074 / .088	.064 / .076	.022 / .028	.442 / .458	.442 / .458	.050 / BSC	.045 / .055	.075 / .095
V	44 / .650 SQ	.073 / .089	.063 / .077	.022 / .028	.643 / .662	.643 / .662	.050 / BSC	.045 / .055	.075 / .095

* Solder dip finish for military parts conform to MIL-M-38510, Type A.

W TO-99 METAL CAN

X TO-100 METAL CAN

BOTTOM VIEW



PKG. CODE	LEAD COUNT	DIM. A	DIM. ϕB	DIM. ϕD	DIM. e	DIM. F	DIM. K	DIM. K1	DIM. L	DIM. Q
W	8 TO-99	.165 / .185	.016 / .018	.345 / .365	.190 / .210	.020 / .040	.028 / .034	.028 / .040	.505 / .550	.015 / .040
X	10 TO-100	.165 / .185	.016 / .018	.345 / .365	.220 / .240	.020 / .040	.028 / .034	.028 / .040	.505 / .550	.015 / .040

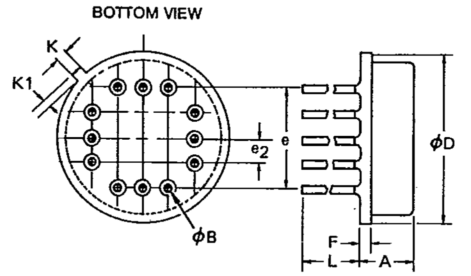
* Solder dip finish add +0.003 inches.

NOTE: Dimensions are $\frac{\text{Min}}{\text{Max}}$. Dimensions are in inches.

BSC means basic spacing between centerlines.

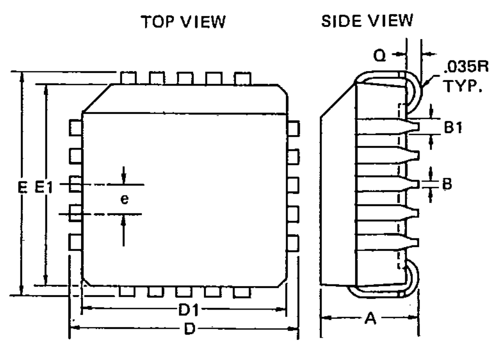
Package Configuration

Y TO-8 METAL CAN



PKG. CODE	LEAD COUNT	DIM. A	DIM. ϕB	DIM. ϕD	DIM. e	DIM. e2	DIM. F	DIM. K	DIM. K1	DIM. L
Y	12 TO-8	.130/.150	.016/.021	.585/.615	.400/BSC	.100/BSC	.020/.040	.027/.034	.027/.045	.500/.550

AA AB AC PLASTIC LEADED CHIP CARRIER



PKG. CODE	LEAD COUNT	DIM. A	DIM. B	DIM. B1	DIM. D/E	DIM. D1/E1	DIM. e	DIM. Q
AA	20	.165/.180	.013/.021	.026/.032	.385/.395	.350/.356	.050/BSC	.020/—
AB	28	.165/.180	.013/.021	.026/.032	.485/.495	.450/.456	.050/BSC	.020/—
AC	44	.165/.180	.013/.021	.026/.032	.685/.695	.650/.656	.050/BSC	.020/—

NOTE: Dimensions are Min/Max. Dimensions are in inches.

BSC means basic spacing between centerlines.