Signetics

74180
Parity Generator/Checker

9-Bit Odd/Even Parity Generator/Checker
Product Specification

Logic Products

FEATURES
- **Word length easily expanded by cascading**
- **Generate even or odd parity**
- **Checks for parity errors**
- **See '280 for faster parity checker**

TYPE	TYPICAL PROPAGATION DELAY, P_O = 0V	TYPICAL SUPPLY CURRENT
74180	36ns	34mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ±5%; T_A = 0°C to +70°C
Plastic DIP	N74180N

NOTE:
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74
$I_0 - I_7$	Data inputs	1ul
P_E, P_O	Parity inputs	2ul
Σ_E, Σ_O	Parity outputs	10ul

NOTE:
A 74 unit load (ul) is understood to be 40μA I_{IH} and −1.6mA I_{IL}.

DESCRIPTION

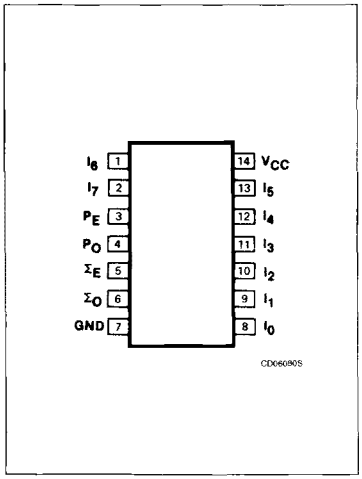
The '180 is a 9-bit parity generator or checker commonly used to detect errors in high speed data transmission or data retrieval systems. Both Even and Odd parity enable inputs and parity outputs are available for generating or checking parity on 8-bits.

True active-HIGH or true active-LOW parity can be generated at both the Even and Odd outputs. True active-HIGH parity is established with Even Parity enable input (P_E) set HIGH and the Odd Parity enable input (P_O) set LOW. True active-LOW parity is established when P_E is LOW and P_O is HIGH. When both enable inputs are at the same logic level, both outputs will be forced to the opposite logic level.

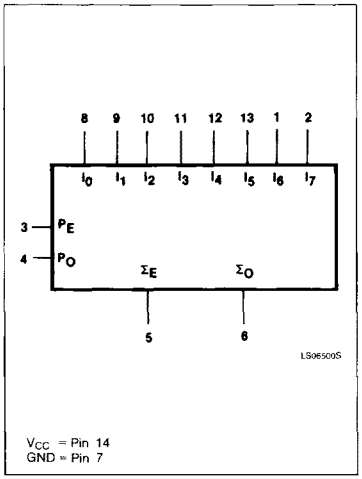
Parity checking of a 9-bit word (8 bits plus parity) is possible by using the two enable inputs plus an inverter as the ninth data input. To check for true active-HIGH parity, the ninth data input is tied to the P_O input and an inverter is connected between the P_O and P_E inputs. To check for true active-LOW parity, the ninth data input is tied to the P_E input and an inverter is connected between the P_E and P_O inputs.

Expansion to larger word sizes is accomplished by serially cascading the '180 in 8-bit increments. The Even and Odd parity outputs of the first stage are connected to the corresponding P_E and P_O inputs, respectively, of the succeeding stage.

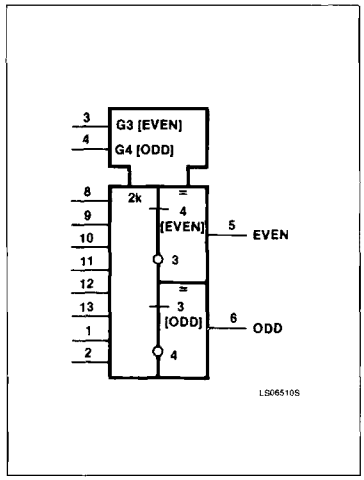
PIN CONFIGURATION



LOGIC SYMBOL

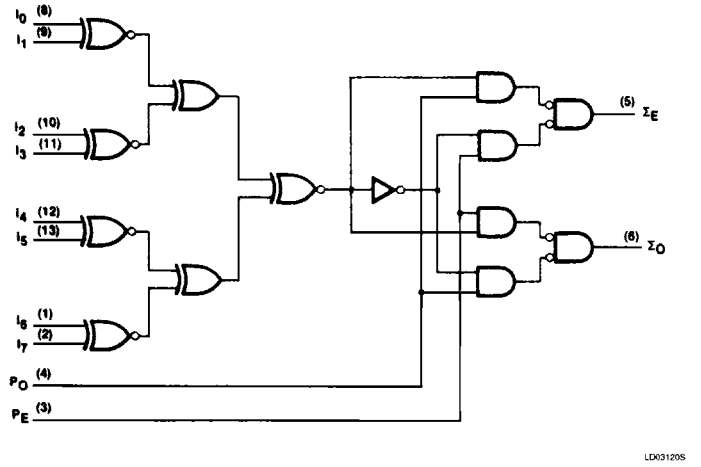


LOGIC SYMBOL (IEEE/IEC)



Parity Generator/Checker — 74180

LOGIC DIAGRAM



( ) = Pin Numbers
V_{CC} = Pin 14
GND = Pin 7

FUNCTION TABLE

INPUTS			OUTPUTS	
Number of HIGH Data Inputs ($I_0 - I_7$)	P_E	P_O	Σ_E	Σ_O
Even	H	L	H	L
Odd	H	L	L	H
Even	L	H	L	H
Odd	L	H	H	L
X	H	H	L	L
X	L	L	H	H

H = HIGH voltage level
L = LOW voltage level
X = Don't care

5

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		74	UNIT
V_{CC}	Supply voltage	7.0	V
V_{IN}	Input voltage	−0.5 to +5.5	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		74			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage	2.0			V
V_{IL}	LOW-level input voltage			+0.8	V
I_{IK}	Input clamp current			−12	mA
I_{OH}	HIGH-level output current			−800	μA
I_{OL}	LOW-level output current			16	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

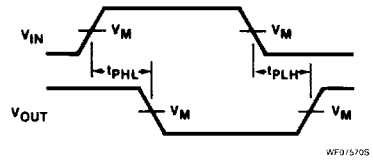
PARAMETER		TEST CONDITIONS[1]		74180			UNIT
				Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OH} = MAX		2.4	3.3		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OL} = MAX			0.2	0.4	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}				−1.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5V				1.0	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.4V	$I_O - I_7$ inputs			40	μA
			P_E, P_O inputs			80	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.4V	$I_O - I_7$ inputs			−1.6	mA
			P_{OE}, P_O inputs			−3.2	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		−18		−55	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX			34	56	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. Measure I_{CC} with P_E and P_O inputs at 4.5V, all other inputs and outputs open.

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

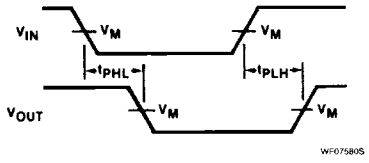
PARAMETER		TEST CONDITIONS	74		UNIT
			C_L = 15pF, R_L = 400Ω		
			Min	Max	
t_{PLH} t_{PHL}	Propagation delay Data to even output	Waveforms 1 & 2, P_O = 0V		60 68	ns
t_{PLH} t_{PHL}	Propagation delay Data to odd output	Waveforms 1 & 2, P_O = 0V		48 38	ns
t_{PLH} t_{PHL}	Propagation delay Data to even output	Waveforms 1 & 2, P_E = 0V		48 38	ns
t_{PLH} t_{PHL}	Propagation delay Data to odd output	Waveforms 1 & 2, P_E = 0V		60 68	ns
t_{PLH} t_{PHL}	Propagation delay P_E or P_O to output	Waveform 1		20 10	ns

AC WAVEFORMS



V_M = 1.3V for 74LS; V_M = 1.5V for all other TTL families.

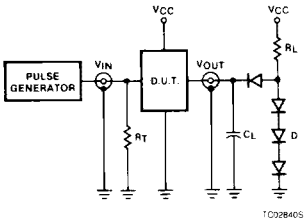
Waveform 1. Waveform For Inverting Outputs



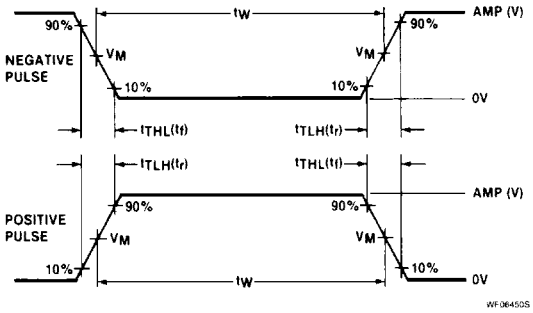
V_M = 1.3V for 74LS; V_M = 1.5V for all other TTL families.

Waveform 2. Waveform For Non-Inverting Outputs

TEST CIRCUITS AND WAVEFORMS



Test Circuit For 74 Totem-Pole Outputs



V_M = 1.3V for 74LS; V_M = 1.5V for all other TTL families.

Input Pulse Definition

DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns

5