Signetics

FAST 74F83
4-Bit Adder

FAST Products

Product Specification

FEATURES

- **High speed 4-bit binary addition**
- **Cascadable in 4-bit increments**
- **Functional equivalent to 'F283 but with center power pins**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F83	7.0ns	36mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
16-Pin Plastic DIP	N74F83N
16-Pin Plastic SOL	N74F83D

DESCRIPTION

The 74F83 adds two 4-bit binary words (A_n plus B_n) plus the incoming carry. The binary sum appears on the sum outputs (Σ_0-Σ_3) and the outgoing carry (C_{OUT}) according to the equation:

$C_{IN} + 2^0(A_0 + B_0) + 2^1(A_1 + B_1) + 2^2(A_2 + B_2) + 2^3(A_3 + B_3)$

$= \Sigma_0 + 2\Sigma_1 + 4\Sigma_2 + 8\Sigma_3 + 16C_{OUT}$

where (+) = plus

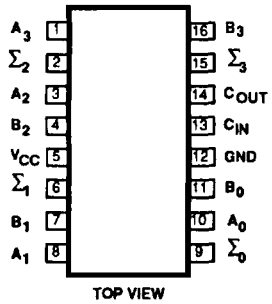
Due to the symmetry of the binary add function, the 'F83 can be used with either all active-High operands (positive logic) or with all active-Low operands (negative logic). See Function Table. With active-High inputs, C_{IN} cannot be left open; it must be held Low when no "carry in" is intended. Interchanging inputs of equal weight does not affect the operation, thus A_0, B_0, C_{IN} can arbitrarily be assigned to pins 10, 11, 13, etc.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

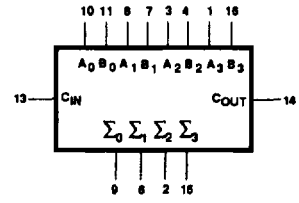
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_0 - A_3	A operand inputs	1.0/2.0	20µA/1.2mA
B_0 - B_3	B operand inputs	1.0/2.0	20µA/1.2mA
C_{IN}	Carry input	1.0/1.0	20µA/0.6mA
C_{OUT}	Carry output	50/33	1.0mA/20mA
Σ_0 - Σ_3	Sum outputs	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION

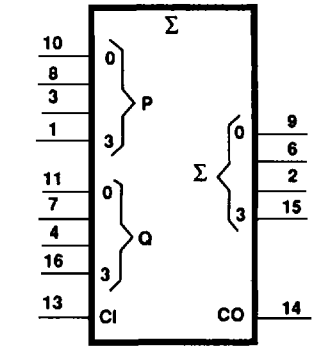


LOGIC SYMBOL

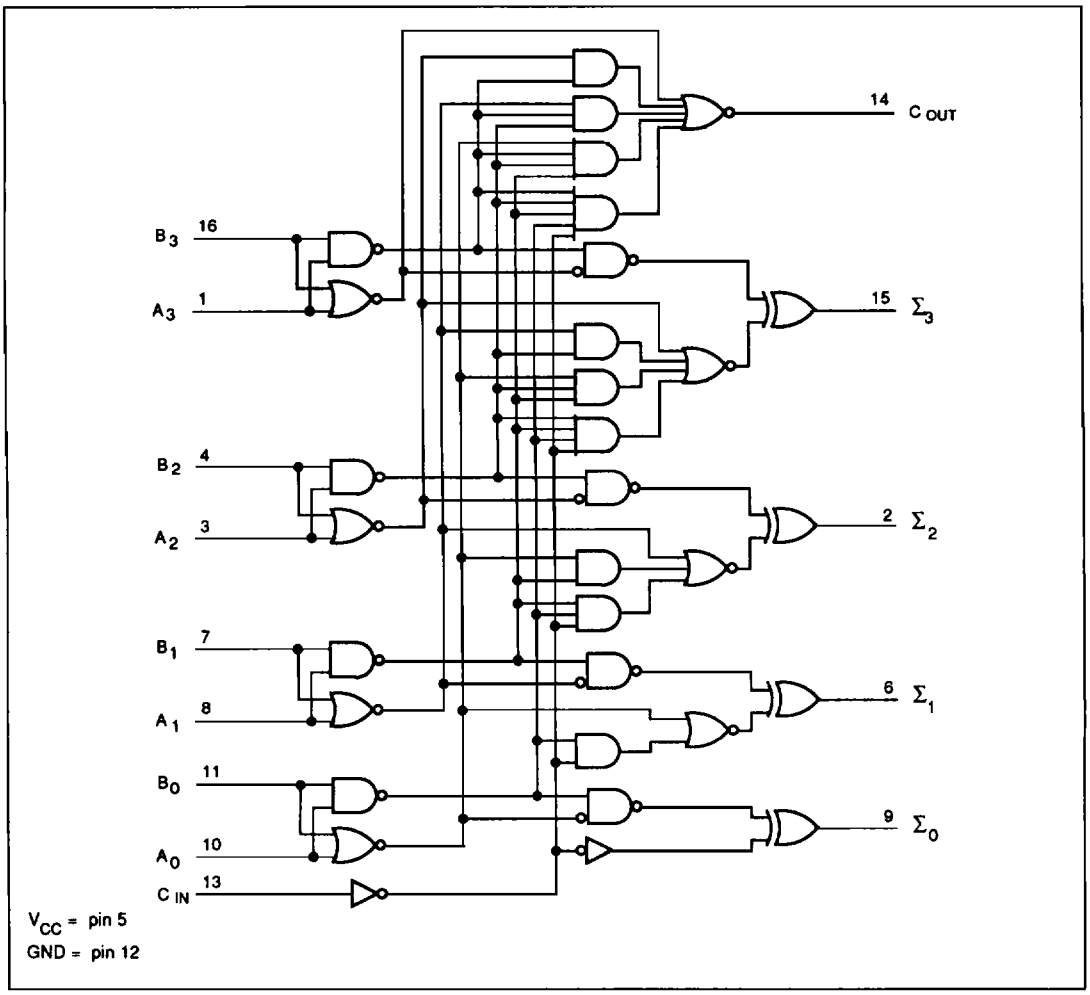


V_{CC} = Pin 5
GND = Pin 12

LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

PINS	C_{IN}	A_0	A_1	A_2	A_3	B_0	B_1	B_2	B_3	Σ_0	Σ_1	Σ_2	Σ_3	C_{OUT}
Logic levels	L	L	H	L	H	H	L	L	H	H	H	L	L	H
Active High	0	0	1	0	1	1	0	0	1	1	1	0	0	1
Active Low	1	1	0	1	0	0	1	1	0	0	0	1	1	0

Example:
1001
1010
10011
(10+9=19)
(carry+5+6=12)

H = High voltage level
L = Low voltage level

Due to pin limitations, the intermediate carries of the 'F83 are not brought out for use as inputs or outputs. However, other means can be used to effectively insert a carry into, or bring a carry out from, an intermediate stage.

Figure a shows how to make a 3-bit adder. Tying the operand inputs of the fourth adder (A_3, B_3) Low makes Σ_3 dependent only on, and equal to, the carry from the third adder.

Using somewhat the same principle, Figure b shows a way of dividing the 'F83 into a 2-bit and a 1-bit adder. The third stage adder (A_2, B_2, Σ_2) is used as means of getting a carry (C_{10}) signal into the fourth stage (via A_2 and B_2) and bringing out the carry from the second stage on Σ_2. Note that as long as A_2 and B_2 are the same, whether High or Low, they do do not influence Σ_2. Similarly, when A_2 and B_2 are the same, the carry into the third stage does not influence the carry out of the third stage.

Figure c shows a method of implementing a 5-input encoder where the inputs are equally weighted. The outputs Σ_0, Σ_1 and Σ_2 present a binary number equal to the number of inputs I_0 - I_4 that are true.

Figure d shows one method of implementing a 5-input majority gate. When three or more of the inputs I_0 - I_4 are true, the output M_4 is true.

APPLICATIONS

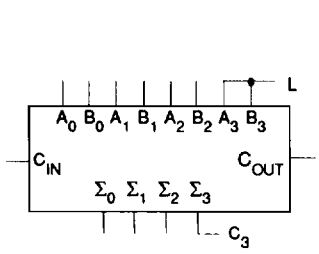


Figure a 3-bit adder

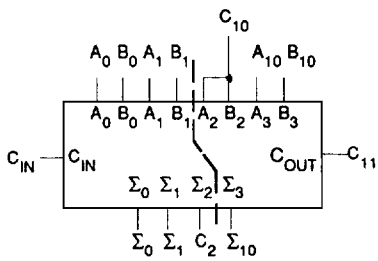


Figure b 2-bit and 1-bit adder

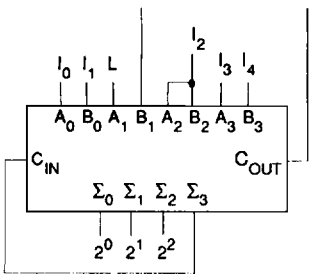


Figure c 5-input Encoder

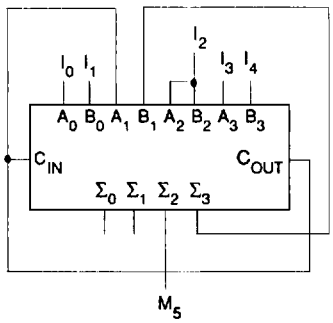


Figure d 5-input majority Gate

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.5			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.30	0.50	V
			V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current	C_{IN} only	V_{CC} = MAX, V_I = 0.5V				-0.6	mA
		A_n, B_n					-1.2	mA
I_{OS}	Short circuit output current[3]		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)		V_{CC} = MAX			36	55	mA

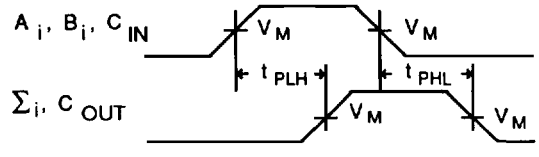
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

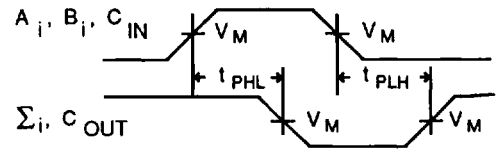
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay C_{IN} to Σ_i	Waveform 1, 2	3.5 4.0	7.0 7.0	9.5 9.5	3.0 3.5	10.5 10.5	ns
t_{PLH} t_{PHL}	Propagation delay A_i or B_i to Σ_i	Waveform 1, 2	3.5 3.5	7.0 7.0	9.5 9.5	2.5 3.5	10.5 10.5	ns
t_{PLH} t_{PHL}	Propagation delay C_{IN} to C_{OUT}	Waveform 2	3.5 3.0	5.7 5.4	7.5 7.0	3.5 2.5	8.5 8.0	ns
t_{PLH} t_{PHL}	Propagation delay A_i or B_i to C_{OUT}	Waveform 1, 2	3.5 2.5	5.7 5.3	7.5 7.0	3.0 2.5	8.5 8.0	ns

AC WAVEFORMS



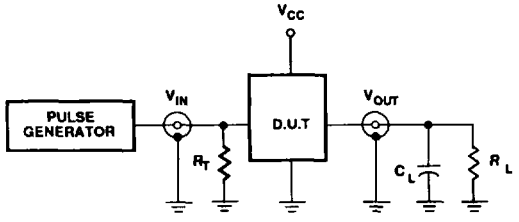
Waveform 1. Propagation Delay
Operands and Carry inputs to Outputs



Waveform 2. Propagation Delay
Operands and Carry inputs to Outputs

NOTE: For all waveforms, V_M = 1.5V

TEST CIRCUIT AND WAVEFORMS



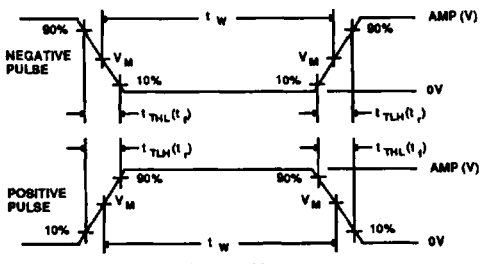
Test Circuit For Totem-Pole Outputs

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns