SEEQ®
Technology, Incorporated

83C94
10BASE-T TWISTED PAIR TRANSCEIVER

PRELIMINARY

April 1993

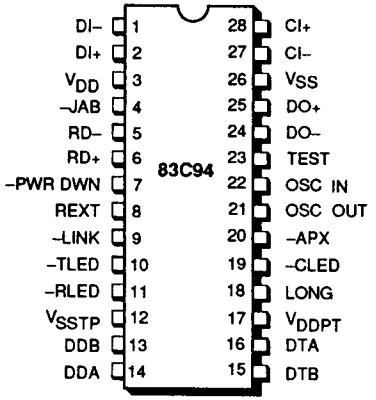
Features

- ***Low Power CMOS Technology – 125 µA Standby (typical)***
- ***Meets IEEE 802.3 10BASE-T standard for link integrity, AUI and twisted pair squelch, collision detection, SQE test, jabber, and AUI loopback***
- ***Direct Interface to SEEQ 8020/8023A Manchester Code Convertor MCC™***
- ***External MAU or AUI Embedded MAU applications***
- ***Autopolarity option to detect and correct inverted received data***
- ***Power-down mode***
- ***High noise rejection using dual differential peak detectors, differential receivers and dynamic squelch threshold voltage***
- ***Direct connect LED drivers for link, collision, jabber, transmit, receive, and polarity reversal***
- ***High-speed receiver architecture minimizes jitter***
- ***Reduced threshold option for long distance (20% increase)***
- ***28-pin DIP or 28-pin PLCC***
- ***Loopback test capability for diagnostics and isolation***

Description

The SEEQ 83C94 low power CMOS 10BASE-T transceiver connects directly to the SEEQ 8020/8023A Manchester Code Convertors and together with either SEEQ's 8003 or 8005 data link controller, the SEEQ Chipset provides a complete Ethernet link solution to IEEE 802.3 10BASE-T standard networks utilizing twisted pair media. The SEEQ 83C94 can be used in embedded MAU and external MAU applications using its AUI features.

DUAL-IN-LINE (DIP)
TOP VIEW



LEADED CHIP CARRIER (PLCC)
TOP VIEW

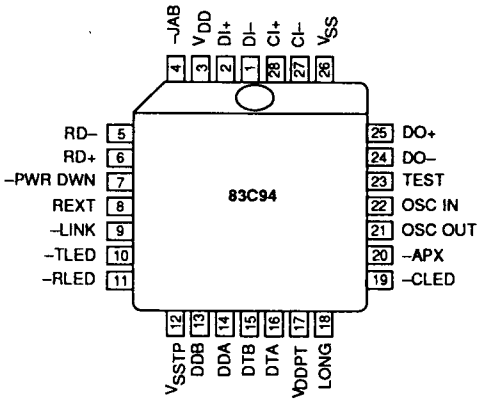


Figure 1. Pin Configuration 83C94

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System Options

External MAU

In external asynchronous MAU applications, the 83C94 is located on a separate circuit board outside the Data Terminal Equipment (DTE) and connected through a standard Ethernet Attachment Unit Interface (AUI) as shown in Figure 2. A more detailed external MAU application is shown on page 12. The AUI signals on the 83C94 are used to transmit data (DI+ and DI–), receive data (DO+ and DO–), and report the occurrence of a collision (CI+ and CI–). The LED indicators reflect the current state of the network, the attached DTE, and the twisted pair link. The 83C94 provides LED outputs for the following MAU functions:

- *–TLED - Transmit*
- *–RLED - Receive*
- *–LINK - Link Integrity*
- *–JAB - Jabber*
- *–CLED - Collision*
- *–APX - Autopolarity Detection & Correction*

Pin Names

Signal Name	Type	External MAU 83C94		Pin Descriptions
		28-pin DIP	28-pin PLCC	
DI–	Output	1	1	DI Minus
DI+	Output	2	2	DI Plus
V_{DD}	Power	3	3	Power
–JAB	Output	4	4	Jabber
RD–	Input	5	5	Receive Minus
RD+	Input	6	6	Receive Plus
–PWR DWN	Input	7	7	Power Down
REXT	Input	8	8	External Resistor
–LINK	In/Out	9	9	Link Integrity
–TLED	Output	10	10	Transmit LED
–RLED	Output	11	11	Receive LED
V_{SSTP}	Ground	12	12	Twisted Pair Driver and Digital Ground
DDB	Output	13	13	Delayed Data B
DDA	Output	14	14	Delayed Data A
DTB	Output	15	15	Data B
DTA	Output	16	16	Data A
V_{DDTP}	Power	17	17	Twisted Pair Driver and Digital Power
LONG	Input	18	18	Long Cable Mode
–CLED	In/Out	19	19	Collision LED
–APX	In/Out	20	20	Auto Polarity
OSC OUT	Output	21	21	Oscillator Output
OSC IN	Input	22	22	Oscillator Input
TEST	Input	23	23	External Test (Manufacturing use only)
DO-	Input	24	24	DO Minus
DO+	Input	25	25	DO Plus
V_{SS}	Ground	26	26	Ground
CI-	Output	27	27	Collision Minus
CI+	Output	28	28	Collision Plus

The AUI and twisted pair interface magnetics and filter circuitry isolate and condition the data signals and reduce radiated emissions. These interface circuits are commonly available as integrated hybrid components.

Embedded MAU

Figure 3 shows a typical embedded MAU application. The 83C94 can directly connect to SEEQ's 8020/8023A MCCs or any Manchester Encoder/Decoder (ENDEC) which supports a standard AUI. In embedded applications, magnetics are not typically necessary for the AUI connection between the 83C94 and the or Manchester Encoder/Decoder. The filters and magnetics used for the twisted pair interface are identical to the external MAU implementation. Integrated hybrid filters with magnetics are available.

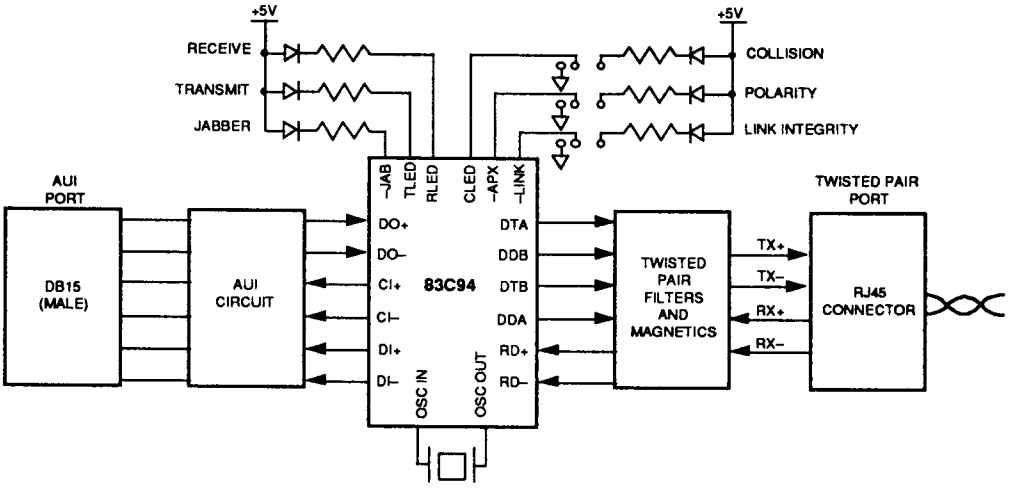

Figure 2. External MAU Application

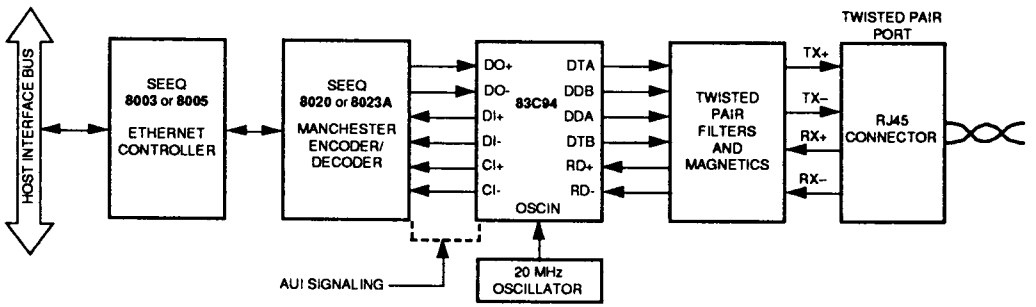

Figure 3. Embedded MAU Application

Pin Descriptions

–APX: Autopolarity LED Driver.

This is an open-drain, 16 mA output with an internal pullup and sampled input. –APX is driven low to indicate that a reversed twisted pair has been detected on the twisted pair receive circuit and corrected. When tied low, –APX disables the autopolarity function.

CI+: Collision In Plus.

This current source output transmits a 10MHz signal to the AUI port when a collision is detected or during a Signal Quality Error (SQE) test.

CI–: Collision In Minus.

This current source output transmits a 10 MHz signal to the AUI port that is the inverse of the CI+ signal.

–CLED: Collision LED Driver.

This is an open-drain, 16mA, stretched output with an internal pullup and sampled input. –CLED is driven low whenever a collision has taken place on the twisted pair. Tie –CLED low to disable the SQE test.

DDA: Delayed Data A.

This output is the DTA signal delayed by 50ns. This driver will source or sink 32 mA. It is low during idle.

DDB: Delayed Data B.

This output is the DTB signal delayed by 50 ns. This driver will source or sink 32 mA. It is low during idle.

DI+: Data In Plus.

This current source output transmits the primary data to the AUI port. It is high during idle.

DI–: Data In Minus.

This current source output transmits the inverse data to the AUI port. It is high during idle.

DO+: Data Out Plus.

This AUI input receives the primary transmit data input from the AUI.

DO–: Data Out Minus.

This AUI input receives the inverse transmit data output from the AUI.

DTA: Data A.

This is the data to be transmitted on the twisted pair. This driver will source or sink 32 mA. It is low during idle.

DTB: Data B.

This is the inverted data to be transmitted on the twisted pair. This driver will source or sink 32 mA. It is low during idle.

–JAB: Jabber LED Driver.

When low, this 16 mA, stretched output indicates that the 83C94 has detected a jabber condition. –JAB is driven high to indicate no jabber condition.

–LINK: Link Integrity LED Driver.

This is an open-drain, 16 mA output with an internal pullup and sampled input. –LINK is driven low when the device has detected a properly functioning twisted pair link. Tie –LINK low to disable the link test.

LONG: Long Cable Mode.

This is an active high input with an internal pulldown. When high, it enables a lower twisted pair receive threshold to enable operation over cables that are longer than 100 meters as recommended in the 10BASE-T standard.

OSCIN: Oscillator In.

This input is connected to a crystal or the output of an external oscillator.

OSCOUT: Oscillator Out.

This output is connected to a crystal or left unconnected if an external oscillator is used.

–PWR DWN: Power Down.

When low, this input places the analog section of the 83C94 in power-down mode which uses the least possible current. This also disables the internal clock to eliminate dynamic current consumption in the digital section.

RD+: Receive Plus.

This is the positive data received from the twisted pair input.

RD–: Receive Minus.

This is the negative data received from the twisted pair input.

REXT: External Resistor.

This resistor sets the drive level of the DI± and CI± current drivers.

–RLED: Receive LED Driver.

This 16 mA, stretched, open-drain output has an internal pullup and is used for status information only. –RLED drives

low when the device is receiving a packet. –RLED is not asserted when the 83C94 is in a link-fail state.

TEST: External Test.
This active high input places the 83C94 in a test mode for manufacturing purposes only. TEST must be tied low for normal operation.

–TLED: Transmit LED Driver.
This is a 16 mA, stretched, open-drain output with an internal pullup. –TLED drives low whenever the 83C94 is transmitting a packet onto the twisted pair. –TLED is not asserted if the 83C94 has detected a jabber condition or is in a link-fail state.

V_{DD}: Power.
This is the V_{DD} supply for the AUI driver, AUI receiver, and twisted pair receiver.

V_{DDTP}: Twisted pair receiver.
This is the V_{DD} supply for the twisted pair driver and digital logic.

V_{SS}: Ground.
This is the ground for the AUI driver, AUI receiver, and twisted pair receiver.

V_{SSTP}: Twisted Pair Ground.
This provides ground for the twisted pair driver and digital logic.

Attachment Unit Interface (AUI)

AUI is a standard Ethernet interface that connects a DTE to a MAU. Of the six differential signals that connect to an AUI, DO+ and DO– receive data from the DTE for transmission onto the twisted pair media. DI+ and DI– are used for data that has been received over the twisted pair media. CI+ and CI– are used to flag a collision and perform the SQE test.

The AUI signals may be connected to:

- *An AUI cable through an isolation transformer.*
- *The AUI signals of any Manchester ENDEC or MCC which supports AUI signaling.*

The 83C94 AUI drivers have been designed to provide balanced differential voltage levels when signaling. The drivers have equal low-high and high-low propagation delays to provide minimal skew when driving the AUI signal. Each driver is designed to drive a 50 to 100 µH transformer with a parallel load of 78Ω and 24 to 39 pF on the primary, and 78Ω on the secondary. Each driver output is capable of sinking and sourcing up to 25 mA. In the idle state, the drivers are designed to draw less than 3 mA.

The AUI receiver uses high-speed differential comparators to preserve the edges and the duty cycle of the incoming data. A peak detector is used to qualify the data received from the AUI port.

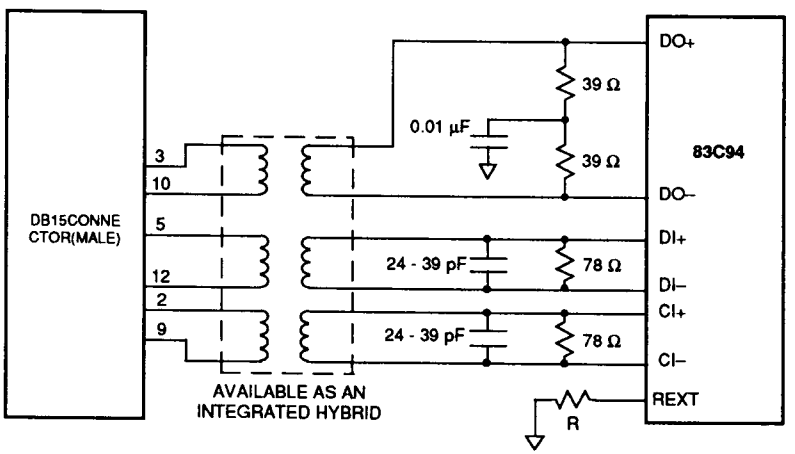

Figure 4. AUI Circuit

In external MAU applications, the AUI magnetics and associated AUI circuitry shown in Figure 4 isolate the MAU from the AUI cable and they reduce the common-mode energy injected into the AUI. An integrated hybrid transformer designed for AUI applications is recommended for the magnetic isolation portion of the circuit. In embedded applications, the transformer is typically not needed. Refer to the VENDOR INFORMATION section on page 13 for specific parts.

AUI Driver Current

The external resistor which is connected from the REXT pin to ground controls the AUI driver current. The AUI driver current output is determined by the following relationship:

$$I_{AO} \cong \frac{185}{R_{EXT}\ (K\Omega)}\ mA$$

In embedded MAU applications the AUI current may be reduced since driving an AUI cable is not a factor in the interface. To meet the 10BASE-T specification in external MAU applications, REXT is typically 10KΩ.

AUI Driver Ramp-Up

When idle, the AUI drivers ramp to V_{DD} slowly to avoid undershoot below the negative threshold of the connected AUI receiver. Figure 5 demonstrates AUI undershoot caused by bringing the drivers to an idle state too fast. Because the connected AUI receiver is looking for an incoming negative pulse, undershoot can result in an invalid unsquelch condition. An internal digital-to-analog converter ensures that the driver ramp-up occurs over approximately 8µs. This allows a smooth transition into an idle AUI state as shown in Figure 6.

Twisted Pair Interface

Figure 7 shows the twisted pair interface used in both external and internal MAU implementations. Of the six signals used by the 83C94 to interface to the twisted pair

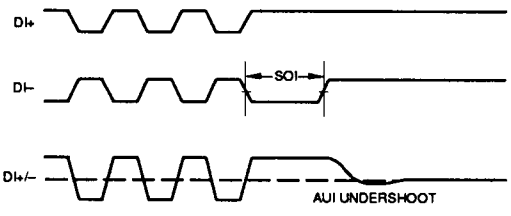

Figure 5. Fast AUI Driver Ramp-Up

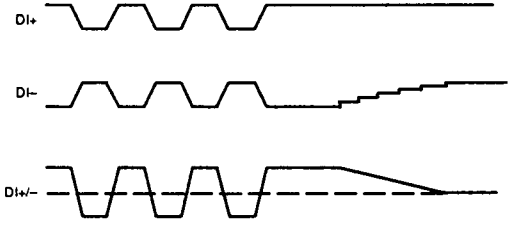

Figure 6. Ideal AUI Driver Ramp-Up

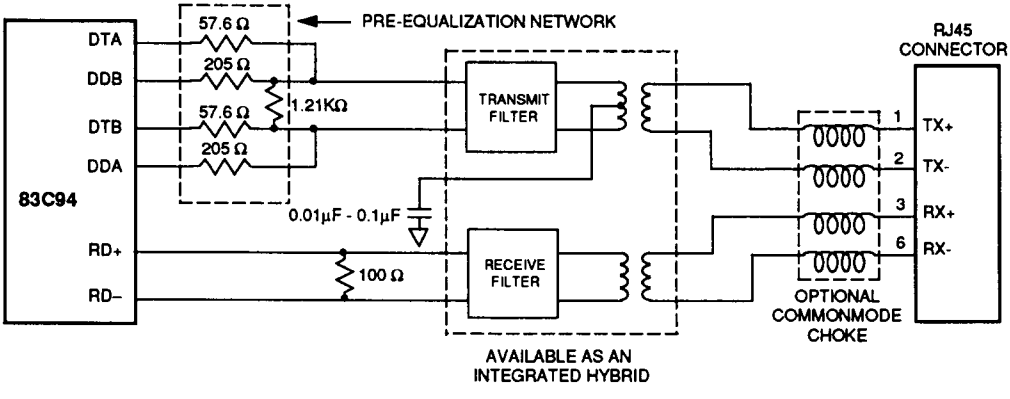

Figure 7. Twisted Pair Interface Circuit

media, four differential signals are used to drive the twisted pair cable. These drivers, when combined with the summing resistor network shown in Figure 7, provide the signal pre-equalization required by the 10BASE-T standard. Two differential input signals are used to receive data from the twisted pair.

Two drivers, DTA and DTB, are the primary data outputs. The remaining drivers, DDA and DDB, provide 1/2 bit-time (50 ns) delayed versions of the primary data outputs. Because output driver skew caused common-mode energy, the 83C94 drivers are designed to have equal rise and fall times as well as balanced low-high and high-low propagation delays to provide optimal signal symmetry. It is critical that the board trace capacitance added to each data driver to equal and at a minimum. All twisted pair drivers are capable of sourcing and sinking 32 mA. When in idle, DTA, DTB, DDA, and DDB drive low.

The 83C94 twisted pair receive circuitry uses a high-speed differential comparator designed to preserve the edge timing of the incoming data. The comparator architecture significantly minimizes the bit jitter added by the transceiver. Dual peak detectors are used by the twisted pair squelch circuitry to qualify both positive and negative signal peaks. Data is considered valid only if three peaks of alternating polarity are detected within a 400 ns window. This greatly improves the noise immunity of the twisted pair receiver. The threshold of the peak detectors is dynamically controlled to further enhance the immunity to noise. The thresholds are initially set high for high noise rejection. Once the data has been qualified, the thresholds are reduced.

The twisted pair magnetics and filters shown in Figure 7 isolate the MAU from the twisted pair media and reduce the radiated emissions. An optional common-mode choke can further reduce emissions of common-mode energy but tested board designs have demonstrated the choke to be unnecessary. Common-mode energy is typically measured at only 25 mV peak in designs without a choke. Components which integrate the transformers and filters are available. Refer to the VENDOR INFORMATION section on page 13 for specific parts.

Transmit Equalization

Signal equalization reduces the signal jitter caused by interference at the end of a long twisted pair cable. A twisted pair cable attenuates a 10 MHz signal more than a 5 MHz signal. Equalization is required to decrease the relative power in the 5 MHz component of the Manchester encoded signal transmitted by the 83C94. This causes the 10 MHz and 5 MHz components of the signal to have approximately the same power content at the far end of the twisted pair.

A "10" or "01" bit pattern generates a Manchester encoded signal which has a 5 MHz component as shown in Figure 8. In a "10" bit pattern, there is a positive signal transition in the middle of the first bit cell followed by a negative transition in the middle of the second. The distance between the transitions of a "01" bit pattern is also 100ns. This 5 MHz signal is known as a "long bit." Similarly, the distance

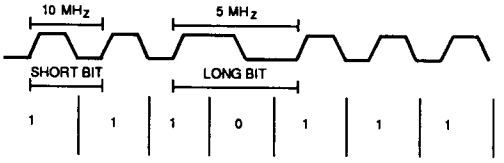

Figure 8. Manchester Encoding

between the transitions of a "11" or "00" bit pattern is 50 ns. This signal generates the 10 MHz component and is known as a "short bit."

The 5 MHz component power is reduced by lowering the voltage amplitude of the second half of all long bits as shown in Figure 9. This is accomplished with two pairs of output drivers in the 84C94. DTA and DTB are the transmit data. DDA and DDB are the transmit data delayed by 1/2 bit-time (50 ns). These four data outputs are summed together as shown in Figure 7. the values of the five network resistors

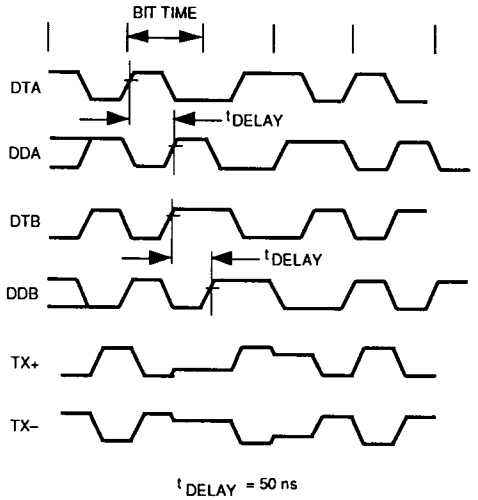

Figure 9. Pre-equalization Example

must be selected to allow the twisted pair line to be terminated in 96Ω.

Driver Delay Calibration

The 83C94 uses an internal, self-calibrating delay line to ensure that the primary twisted pair data outputs (DTA and DTB) and the delayed data outputs (DDA and DDB) maintain a consistent 50 ns ±3 ns delay. Recalibration can require up to 3.2 µs. If a packet is received during recalibration, the delay line defaults to its previous value. The delay line recalibrates on each of the following conditions:

- The end of each transmitted packet.
- Power-on-reset.
- Power up from power-down mode.
- Every 13 ms.

Functional Description

The 83C94 twisted pair transceiver is composed of several functions as shown in Figure 10. The 83C94 supports complete 10BASE-T functionality as well as several enhanced functions such as link integrity, autopolarity detection and correction, smart-squelch logic, power-on-reset and power-down mode, an on-chip crystal oscillator, stretched one-shot LED drivers, collision detection, long distance mode, integrated analog interface circuitry, and dual twisted pair peak detectors.

Link Integrity

During periods of inactivity, link pulses are generated and received by both MAUs at either end of the twisted pair to ensure that the able has not been broken or shorted. A positive, 100 ns Link Integrity signal is generated by the 83C94 and transmitted on the twisted pair every 13 ms during periods of no transmission activity. The 83C94 assumes a link-good state if it sees valid link-pulse activity on the twisted pair receive circuit. If neither receive data or a link pulse (positive or negative) is seen on the receive circuit within 105 ms, the 83C94 enters a link-fail state. If a link-fail condition occurs, four consecutive positive link pulses (or eight negative link pulses) must be received before a link-good condition is assumed. Only link pulses spaced greater than 3 ms and less than 105 ms are considered valid.

In a link-fail state, the 83C94 disables normal Transmit, Receive, AUI loopback, Collision, and SQE test functions. NOTE: The reception of a packet will place the device in a link-good state, but the packet will not be relayed to the AUI DI circuit. Subsequent packets will be transferred normally as long as the device remains in a link-good state.

A link-good state is flagged by the 83C94 externally by driving the –LINK pin low. The Link Integrity function is disabled by tying the –LINK pin to ground which forces the 83C94 into a link-good state. The 83C94 ceases to send link pulses when the link test is disabled; this is required to be compatible with prestandard repeaters.

The 10BASE-T standard recommends that the Link Integrity LED should light when the 83C94 is in a link-good state (includes jumper disable of this function which is a forced link-good state).

Autopolarity

Because twisted pair differential signals can easily be inverted due to wiring errors, the 83C94 incorporates autopolarity detection and correction circuitry. Polarity circuitry monitors the twisted pair receiver peak detectors to determine if normal or inverted data is being received over the twisted pair wire. This is performed by an algorithm that monitors the polarity of the received state-of-idle (SOI) and link pulses. If the signal is inverted, the 83C94 automatically corrects the data internally. The autopolarity function is reset on power-up or when a link failure is detected.

When the 83C94 detects inverted polarity, the –APX pin is driven low. The autopolarity function may be disabled by typing –APX to ground.

Squelch Logic

AUI Squelch

The AUI squelch circuitry dynamically adjusts the sensitivity of the AUI data comparator. At the beginning of a transmission, the AUI squelch is in a high noise rejection squelch state. When the first negative edge appears on the DO± circuit, the AUI data comparator is released by the squelch circuitry, assumes an unsquelch state, and begins receiving data. The AUI squelch circuitry is returned to a squelch state by:

- A normal Start Of Idle (SOI) signal.
- A missing SOI signal.

A missing SOI signal is assumed when no transitions have occurred on the AUI DO± circuit for 175 ns. In this case, an SOI signal is generated and appended to the data which is transmitted onto the twisted pair.

Twisted Pair Squelch

The twisted pair squelch circuitry dynamically adjusts the sensitivity of the twisted pair data comparator and the

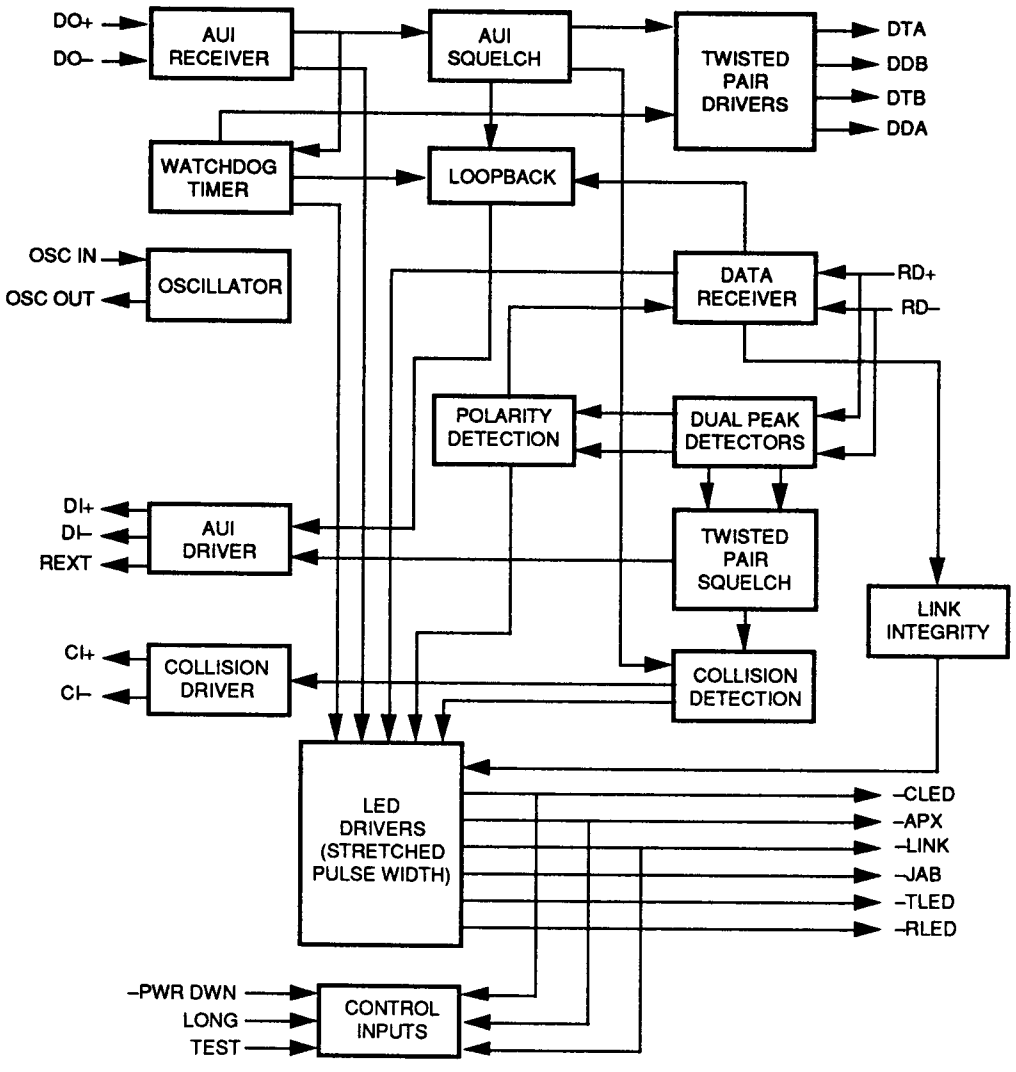

Figure 10. Chip Block Diagram

threshold levels of the dual twisted pair receiver peak detectors. Before signals begin to arrive on the RD± twisted pair circuit, the 83C94 is in a high noise rejection, squelch state. When in a squelch state, no data is transmitted on the AUI DI± circuit. To qualify incoming data, the smart squelch circuitry monitors the peak detectors for three peaks of alternating polarity that occur within a 400 ns window. Once a signal has been qualified by the squelch circuitry, the 83C94 assumes an unsquelch state and reduces the peak detector threshold.

Figure 11 illustrates a signal representing a packet received on the RD± differential circuit. At the beginning of each packet there is a preamble (64 bits) consisting of alternating ones and zeros. This transmits a 5 MHz Manchester signal on the twisted pair. Because a twisted pair cable attenuates a 5 MHz signal less than a 10 MHz signal, higher peak detector thresholds, V_{TPS} and V_{TNS}, can be used by the squelch circuitry to qualify an incoming packet. This offers the greatest possible noise rejection. As shown in Figure 11, when data begins arriving, the 10 MHz Manchester signal may have less amplitude because of pre-equalization errors. The threshold levels must be reduced in the unsquelch state so that all incoming data is guaranteed to be seen by the peak detectors. Because the peak detectors continue to monitor the signal for the Start of Idle (SOI) pulse, the reduced thresholds keep the squelch circuitry from detecting the end of a packed prematurely.

If the 83C94 detects activity on the twisted pair RD± circuit while the DTE is transmitting on the AUI DO± circuit, then a collision condition is occurring. In this case, incoming data is qualified by the squelch circuitry on five peaks of alternating polarity. This provides additional protection against false collisions from impulse noise that may exist on the twisted pair cable caused by cross-talk and nearby electrical equipment.

The twisted pair smart squelch circuitry is returned to a squelch state by any of these conditions:

- *A normal Start Of Idle (SOI) signal.*
- *An inverted SOI signal.*
- *A missing SOI signal.*

A missing SOI signal is assumed when no transitions have occurred on the RD± circuit for 175 ns after a packet has been received. In this case, a normal SOI signal is generated and appended to the data which is transmitted to the DTE on the AUI DI± circuit.

Power-On-Reset

The 83C94 uses a power-on-reset sequence to place itself into a known digital state, to allow the analog sections to stabilize, and to calibrate the internal delay line. Depending on the power-down condition, initialization requires the following lengths of time:

- *Power-on-reset: 105 ms*
- *Power-down mode: 410 µs*

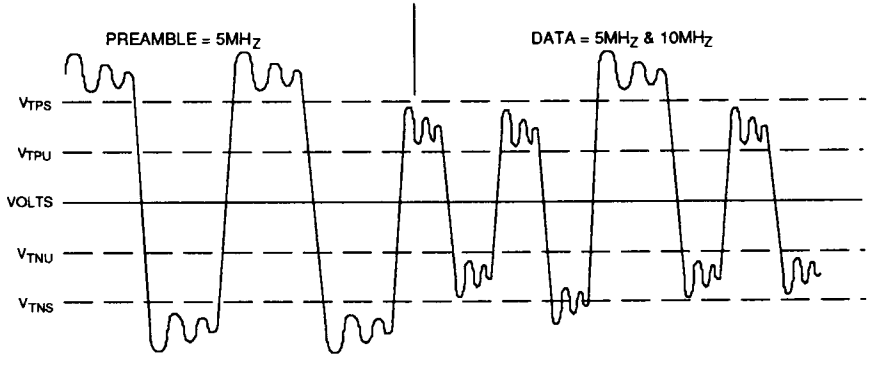

Figure 11. Incoming Twisted Pair Signal

Power-Down Mode

The power-down function is ideal for embedded, lap-top computer applications. In power-down mode, the 83C94 typically pulls only 125 µA. When driving the –PWRDWN pin low, the 83C94 assumes a power-down state. When –PWRDWN is pulled high, normal transceiver operation will resume after the 410 µs calibration sequence is completed.

On-Chip Oscillator

A Pierce-type, crystal oscillator circuit designed for use with an inexpensive, 20 MHz series or parallel resonant crystal is provided on-chip. Tuning capacitors and a start-up resistor are also supplied internally.

Parameter	Min.	Typ.	Max.
CRYSTAL: Freq. Tolerance Motion Resistance Frequency		 20MHz	 0.5% 25Ω
OSCILLATOR: Duty Cycle	40%		60%

If an external oscillator is used, connect the 20 MHz clock to the OSCIN pin and leave the OSCOUT pin floating.

Status Indicators: LED Control

The 83C94 provides six LED driver outputs. There are two types of LED signals: output only and sampled. All LED drivers except APX and –LINK have a stretched time constant of 26.2 ms to ensure that they can be seen by the human eye.

Output LED Drivers

The LED outputs –TLED, –RLED, and –JAB are 16 mA drivers. These signals are used for status information only.

–TLED drives low when the 83C94 is transmitting a packet. –TLED is not asserted if the 83C94 has detected a jabber condition or is in a link-fail state.

–RLED drives low when the 83C94 is receiving a packet. –RLED is not asserted when the 83C94 is in a link-fail state.

–JAB drives low when the device has detected a jabber condition.

Sampled LED Drivers

The –APX, –CLED, and –LINK pins are 16 mA drivers which are used to set the configuration of the 83C94 as well as drive LED status indicators. Every 26.2 ms, these pins are released and allowed to float for 800 µs. During this time, they are sampled by the 83C94. If the signals are externally unconnected or tied to an LED, they will float high due to an internal 100 µA pullup. If the signals are externally tied low, they will remain low. Outside the sampling window, these drivers are placed in an output state and used to drive the LED indicators.

–APX is driven low to indicate that a reversed twisted pair has been detected on the receive circuit and corrected. Tie –APX low to disable the autopolarity function.

–CLED is driven low when a collision has taken place. Tie –CLED low to disable SQE function.

–LINK is driven low when the 83C94 detects a properly functioning twisted pair link. Tie –LINK low to disable the link test. The 10BASE-T standard recommends that the Link LED should be green.

Collision Detection

Collision detection logic determines when transmit and receive signals occur simultaneously on the twisted pair cable. The 83C94 signals the occurrence of a collision by asserting a 10 MHz signal on the AUI C± circuit and by driving the –CLED pin low. Collisions will not be reported when the device is in a link-fail state. The collision signal is also applied to the C± signals when the device has detected a jabber condition or when the SQE test is being performed. The collision function cannot be disabled.

Long Mode

Tying the LONG pin to V_{DD} places the 83C94 in long mode. In long mode, the thresholds of the internal twisted pair receiver peak detectors are lowered to support longer cable lengths. In normal mode, the 83C94 supports twisted pair cable with up to 11.5 dB of attenuation. In long mode, an additional 3 dB of attenuation is supported. Tying the LONG pin to V_{SS} causes the 83C94 to use standard 10BASE-T threshold levels.

SQE Test

The Signal Quality Error (SQE) test is used to test the AUI collision signaling circuitry (C±). After each packet transmission, an SQE signal (also referred to as "heartbeat" signal) is sent to the DTE over the AUI C± circuit. The DTE expects this signal and should flag an error and cease transmission if it does not exist. The SQE test can be disabled by grounding the –CLED pin. This is done in applications that do not support the SQE function (as in repeaters). Tying the –CLED pin low does not affect collision detection functionality but it will disable the collision LED driver.

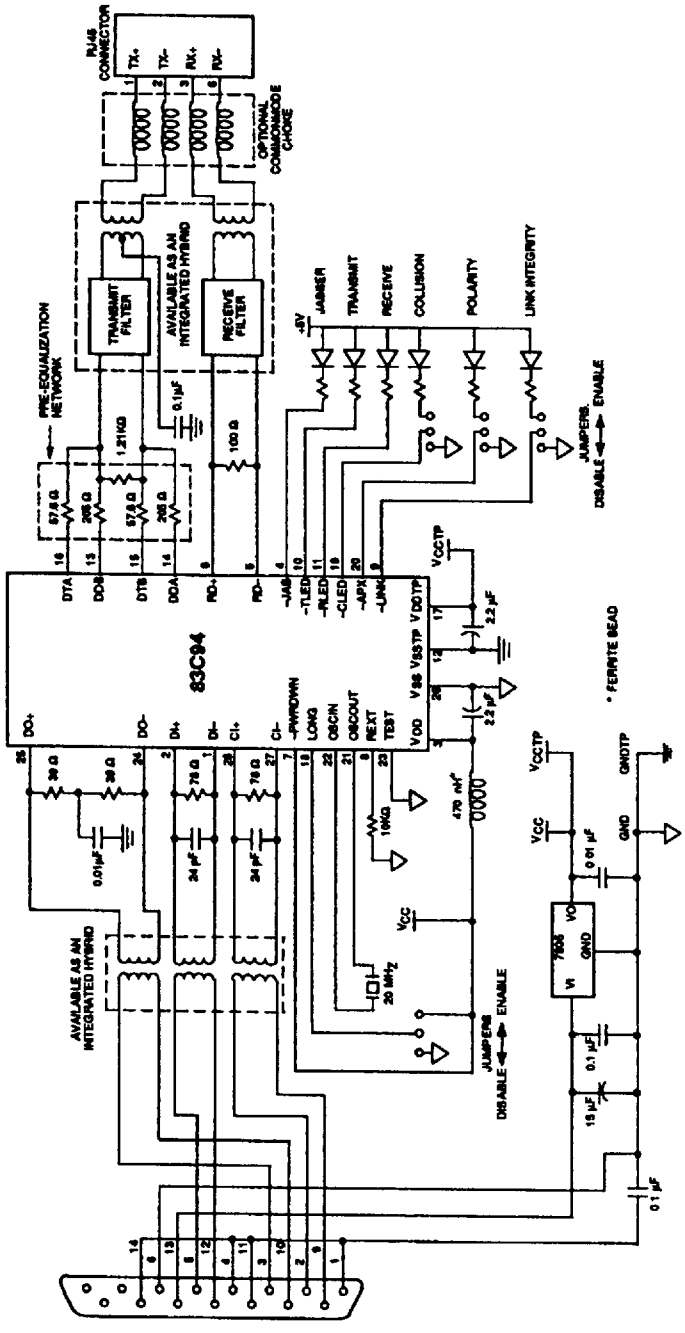

Figure 12. External MAU Schematic

Jabber

Jabber is a self-interrupt function that keeps a damaged node from continuously transmitting on the network. The 83C94 will isolate a "jabbering" DTE from the network if it surpasses a 26.2 ms maximum allowed transmit time. If a transmission exceeds this duration, the jabber function inhibits transmission, discontinues AUI loopback, and sends a collision signal on the AUI CI± circuit. The 83C94 will release the jabber state after the DTE has been idle for at least 420 ms.

The 83C94 drives the –JAB LED signal low when a jabber condition is detected. The jabber function cannot be disabled.

AUI Loopback

When transmitting, the 83C94 retransmits any data it receives on the AUI DO± circuit back to the AUI DI± circuit in order to provide loopback of the transmitted signal. This is done to confirm that the MAU is properly receiving data.

If the 83C94 begins receiving data over the twisted pair during a transmission, a collision state is flagged and it stops AUI loopback. During the collision, the 83C94 begins transmitting the incoming (twisted pair) data over the AUI DI± circuit.

Vendor Information

Attachment Unit Interface

Integrated hybrid transformers designed for AUI applications can be obtained from:

- *Pulse Engineering part #64502.*
- *Valor Electronics part #LT6032*
- *Bel Fuse part #0553-1006-AB.*
- *Coilcraft LAX-ET304.*
- *Any equivalent part.*

Twisted Pair Interface

Components which integrate the transformers and filters are available from:

- *Pulse Engineering part #65421.*
- *Valor Electronics part #PT3877.*
- *Bel Fuse part #A556-2006-DE.*
- *Coilcraft MI320-A.*
- *Any equivalent part.*

Absolute Maximum Stress Range

Temperature
Storage ..... –55°C to +150°C
Under Bias ..... –65°C to +135°C

V_{DD} Supply Voltage ..... –0.5 to 7.0V
V_{IN} Input Voltage ..... V_{SS}–0.5 to V_{DD} +0.5 V
T_L Lead Temperature (soldering 10 sec max.) – 250°C

COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating and only functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximumn rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

	83C94
Temperature Range (Ambient)	0°C to + 70°C
V_{DD} Power Supply	5V± 5%

DC Characteristics

(V_{DD} = 4.75V to 5.25V, V_{SS} = 0V, T_A = 0°C to 70°C)

Symbol	Parameter	Minimum	Maximum	Units
V_{IL}	Digital Low Input Voltage	V_{SS} –0.5	0.8	V
V_{IH}	Digital High Input Voltage	3.85	0.5 + V_{DD}	V
V_{OL}	Digital Low Output Voltage (V_{DD} = 4.5V)		0.4	
V_{OH}	Digital High output Voltage (V_{DD} = 4.5V)	2.4	V	
I_{IL}	Digital Input Leakage Current (V_{DD} = 5.5V)		±10	µA
I_{OL}	Digital Output Leakage Current (V_{DD} = 5.5V)		±10	µA

AUI (V_{DD} = 4.75V to 5.25V, V_{SS} = 0V, T_A = 0°C to 70°C)

Symbol	Parameter	Minimum	Maximum	Units
V_{AOL}	Low Output Voltage for DI+, DI–, CI+, CI–	V_{DD} –2.5	V_{DD} –0.75	V
V_{AOH}	High Output Voltage for DI+, DI–, CI+, CI–	V_{DD} –1.5	V_{DD} –0.25	V
I_{AO}	DI+/– and CI+/– Output Current		25	mA
V_{AIB}	DO+/– Open Circuit Input Voltage (bias)	2.5	V_{DD} –1.0	V
V_{AICM}	DO+/– Common-mode Input Range (V_{DD} = 5V)	2.0	V_{DD} +0.25	V
V_{ASQ}	DO+/– Squelch Threshold	–140	–230	mV
V_{ASW}	DO+/– Switching Threshold	–15	15	mV
V_{ADI}	DI+/– and CI+/– Differential Idle Output (R1 = 78Ω)	–40	40	mV
V_{ADV}	DI+/– and CI+/– Differential Peak Output (R1 = 78Ω)	500	820	mV
R_{AU}	DI+/– and CI+/– Output Resistance		75	Ω

Twisted Pair (V_{DD} = 4.75V to 5.25V, V_{SS} = 0V, T_A = 0°C to 70°C)

Symbol	Parameter	Minimum	Maximum	Units
R_{TI}	RD+/– Differential Input Resistance	3		KΩ
V_{TIB}	RD+ and RD– Open Circuit Input Voltage (bias)	–2.75	V_{DD} –1.0	V
V_{TIV}	RD+/– Differential Input Voltage Range (V_{DD} = 5V)	–3.1	3.1	V
V_{TPS}	RD+/– Positive Squelch Threshold	300	585	mV
V_{TNS}	RD+/– Negative Squelch Threshold	–585	–300	mV
V_{TPU}	RD+/– Positive Unsquelch Threshold	200	350	mV
V_{TNU}	RD+/– Negative Unsquelch Threshold	–350	–200	mV
V_{TSW}	RD+/– Switching Threshold	–15	15	mV
V_{TOH}	DTA, DTB, DDA, DDB High Output Voltage (I = 32 mA, V_{SSTP} = 0V)	V_{DDTP} – 0.44	V_{DDTP}	V
V_{TOL}	DTA, DTB, DDA, DDB Low Output Voltage (I = 32 mA, V_{DDTP} = 0V)	V_{SSTP}	V_{SSTP} +0.44	V
I_{TO}	DTA, DTB, DDA, DDB Output Current		32	mA
R_{TO}	DTA, DTB, DDA, DDB Output Resistance		13.5	Ω

Power Supply (V_{DD} = 4.75V to 5.25V, V_{SS} = 0V, T_A = 0°C to 70°C)

Symbol	Parameter	Typical	Maximum	Units
I_{DDC}	Power Supply Current with Crystal (–PWR DWN = High, V_{DD} = 5V)	32	50	mA
I_{DDO}	Power Supply Current with Oscillator (–PWR DWN = High, V_{DD} = 5V)	26	42	mA
I_{PD}	Power Supply Current in Power-Down Mode (–PWR DWN = Low)	125	300	µA

AC Characteristics

Figure 13. Output Driver Timing (V_{DD} = 4.75V to 5.25V, V_{SS} = 0V, T_A = 0°C to 70°C)

Num.	Parameter	Min.	Typ.	Max.	Units
1	DTA to DTB Skew	–1.5		+1.5	ns
2	DTA to DDA and DTB to DDB Delay	46		53	ns
3	DDA to DDB Skew	–1.5		+1.5	ns
4	DI+ to DI– and CI+ to CI– Skew	–1.5		1.5	ns

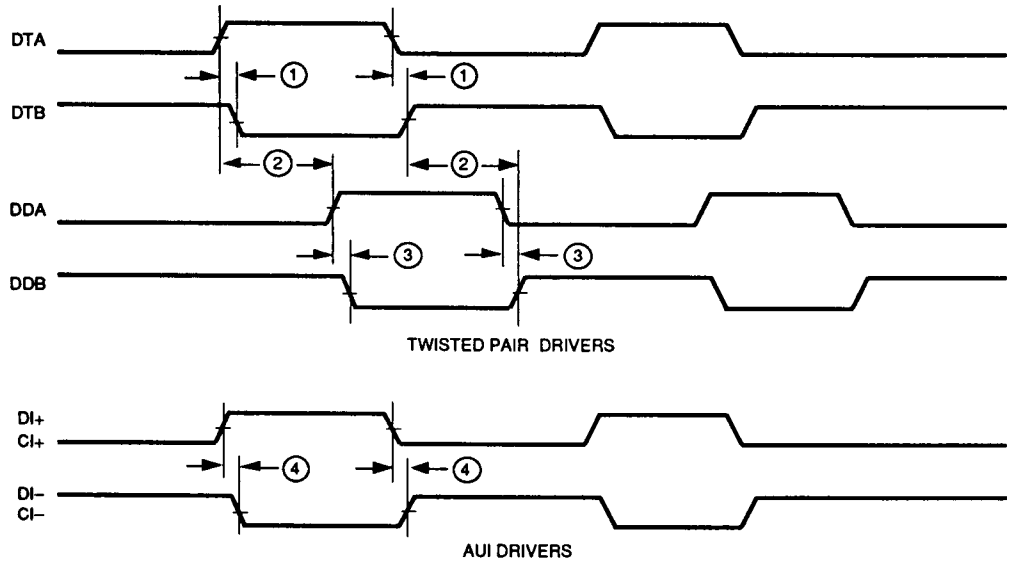

Figure 13. Output Driver Timing

AC Characteristics

Figure 14. Transmit Timing (V_{DD} = 4.75V to 5.25V, V_{SS} = 0V, T_A = 0°C t 70°C)

Num.	Parameter	Min.	Typ.	Max.	Units
5	DO+/– to AUI Loopback on DI+/–	100		250	ns
6	DO+/– to DI+/– Propagation Delay			75	ns
7	Minimum AUI Start of Idle (SOI) Pulse Width	200			ns
8	DO+/– to Twisted Pair (DTA) Propagation Delay			75	ns
9	Start of Idle Generated on Twisted Pair	250		400	ns
10	DO+/– to Unsquelch – Bit Loss			2	Bits
11	DO+/– to –TLED			400	ns
12	–TLED Pulse Width		26.2		ms

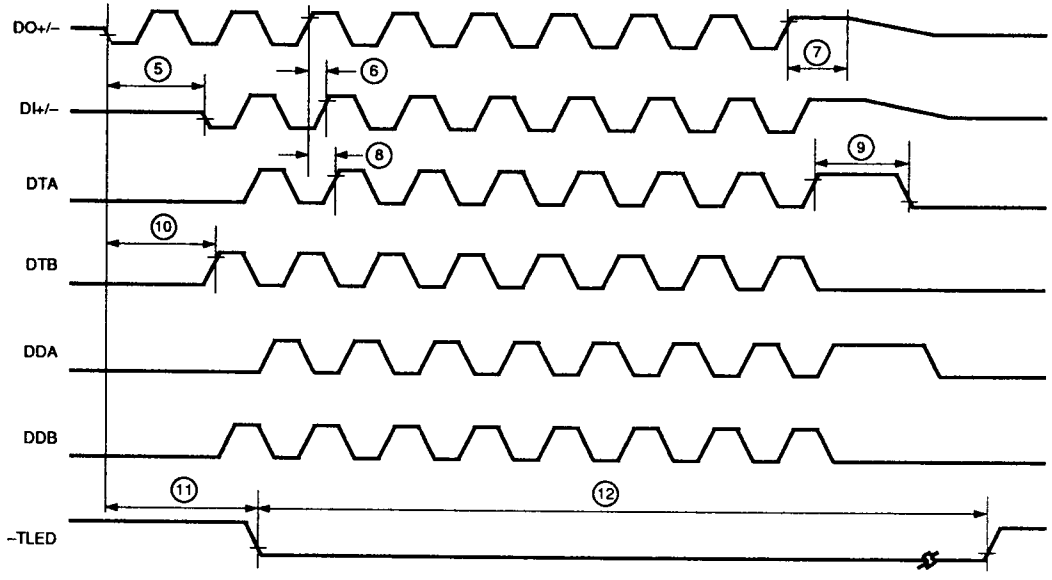

Figure 14. Transmit Timing

AC Characteristics

Figure 15. Receive Timing (V_{DD} = 4.75V to 5.25V, V_{SS} = 0V, T_A = 0°C to 70°C)

Num.	Parameter	Min.	Typ.	Max.	Units
13	Minimum Twisted Pair SOI Pulse Width	200			ns
14	RD+/– to Unsquelch			5	Bits
15	RD+/– to DI+/– Propagation Delay			75	ns
16	DI+/– Ramp Up			8	µs
17	RD+/– to –RLED			600	ns
18	–RLED Pulse Width		26.2		ms

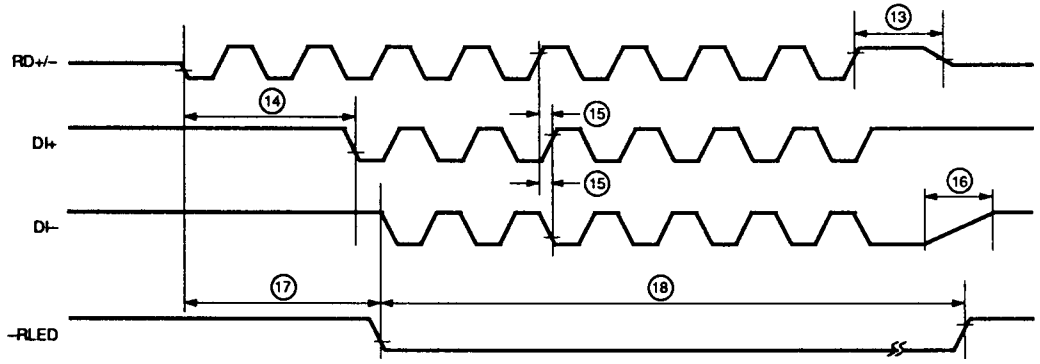

Figure 15. Receive Timing

AC Characteristics

Figure 16. Collision Timing (V_{DD} = 4.75V to 5.25V, V_{SS} = 0V, T_A = 0°C to 70°C)

Num.	Parameter	Min.	Typ.	Max.	Units
19	Collision Signal OFF Delay (CI+/–)			900	ns
20	Collision to –CLED			600	ns
21	–CLED Pulse Width		26.2		ms
22	Collision Signal ON Delay (CI+/–)			900	ns
23	Collision Signal Period (CI+/–)		100		ns
24	Collision to End of AUI Loopback on DI+/–			800	ns
25	Collision to Receive Data on DI+/–			900	ns
26	CI+/– Ramp Up			8	µs
27	Start of AUI Loopback to End of Collision	100			ns

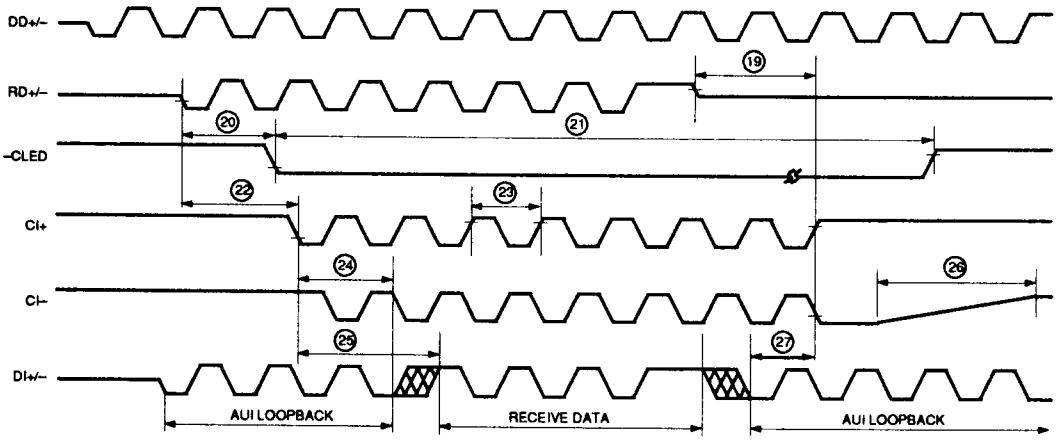

Figure 16. Collision Timing

AC Characteristics

Figure 17. SQE Test Timing (V_{DD} = 4.75V to 5.25V, V_{SS} = 0V, T_A = 0°C to 70°C)

Num.	Parameter	Min.	Typ.	Max.	Units
28	End of Transmission (DO+/–) to SQE Test (CI+/–)	600		1600	ns
29	SQE Test Length	500		1500	ns
30	SQE Test Signal Period		100		ns

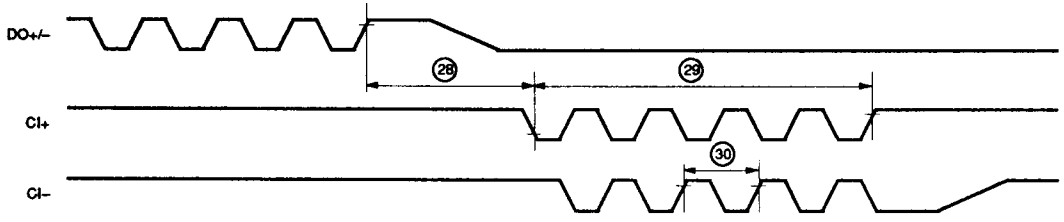

Figure 17. SQE Test Timing

AC Characteristics

Figure 18. Link Test Timing (V_{DD} = 4.75V to 5.25V, V_{SS} = 0V, T_A = 0°C to 70°C)

Num.	Parameter	Min.	Typ.	Max.	Units
31	DTA Link Pulse Width		100		ns
32	DDA, DDB Link Pulse Width		50		ns
33	Duration Between Transmitted Link Pulses	8	13	24	ms
34	Duration Between Received Link Pulses	3		105	ms

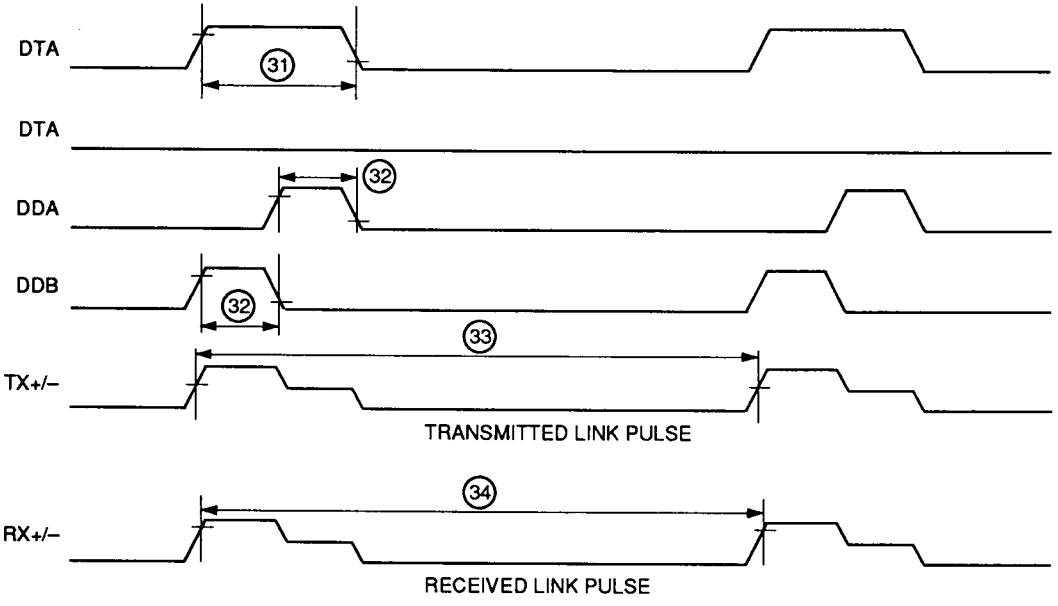

Figure 18 . Link Test Timing

Ordering Information

The 83C94 is available in a 28-pin Plastic Leaded Chip Carrier (PLCC) or a 28-pin Dual-In-line Package (DIP). Use the following part numbers to order the desired package.

PART NUMBER