

Signetics

FAST Products

FEATURES

- High impedance NPN base inputs for reduced loading (20 μ A in High and Low states)
- Independent registers for A and B buses
- Multiplexed real-time and stored data
- Choice of non-inverting and inverting data paths
- Open Collector outputs
- 300 mil wide 24-pin Slim Dip package

DESCRIPTION

The 74F647 and 74F649 Transceivers/Registers consist of bus transceiver circuits with open-collector outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes to a High logic level. Output Enable (\overline{OE}) and DIR pins are provided to control the transceiver function. In the transceiver mode, data present at the high impedance port may be stored in either the A or B register or both. The select (SAB, SBA) controls can multiplex stored and real-time (transparent mode) data. The DIR determines which bus will receive data when the Output Enable, \overline{OE} is active Low. In the isolation mode (Output Enable, \overline{OE} = High), data from Bus A may be stored in the B register and/or data from Bus B may be stored in the A register.

FAST 74F647, 74F649 Transceivers/Registers

74F647 Octal Transceiver/Register, Non-Inverting (Open Collector)

74F649 Octal Transceivers/Register, Inverting (Open Collector)

Product Specification

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F647	65MHz	125mA
74F649	65MHz	125mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$; $T_A = 0^\circ C$ to $+70^\circ C$
24-Pin Plastic Slim DIP (300mil)	N74F647N, N74F649N
24-Pin Plastic SOL ¹	N74F647D, N74F649D

NOTE : 1. Thermal mounting techniques are recommended. See SMD Process Applications (page 17) for a discussion of thermal consideration for surface mounted devices.

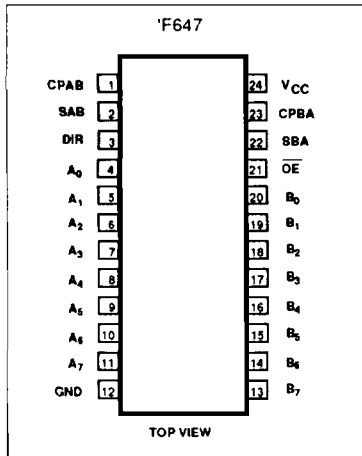
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$A_0 - A_7$	A inputs	1.0/0.033	20 μ A/20 μ A
$B_0 - B_7$	B inputs	1.0/0.033	20 μ A/20 μ A
CPAB	A-to-B clock inputs	1.0/0.033	20 μ A/20 μ A
CPBA	B-to-A clock inputs	1.0/0.033	20 μ A/20 μ A
SAB	A-to-B select input	1.0/0.033	20 μ A/20 μ A
SBA	B-to-A select input	1.0/0.033	20 μ A/20 μ A
DIR	Data flow Directional control enable input	1.0/0.033	20 μ A/20 μ A
\overline{OE}	Output Enable input	1.0/0.033	20 μ A/20 μ A
$A_0 - A_7$	A outputs	OC/106.7	OC/64mA
$B_0 - B_7$	B outputs	OC/106.7	OC/64mA

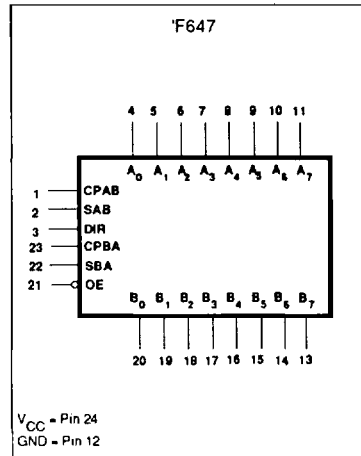
NOTE:

One (1.0) FAST Unit Load is defined as: 20 μ A in the High state and 0.6mA in the Low state.
OC=Open-Collector

PIN CONFIGURATION

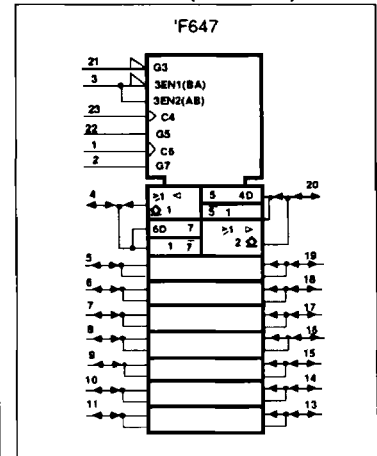


LOGIC SYMBOL



V_{CC} = Pin 24
GND = Pin 12

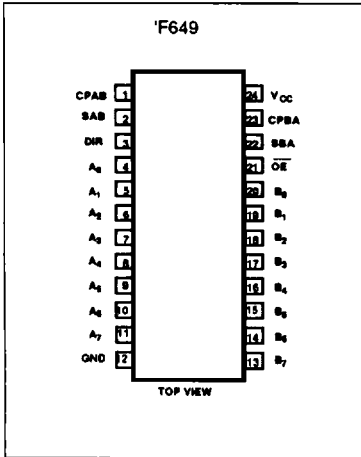
LOGIC SYMBOL (IEEE/IEC)



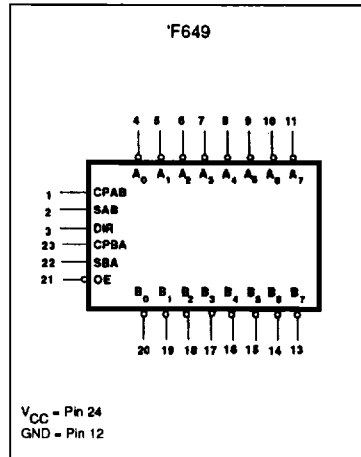
Transceivers/Registers

FAST 74F647, 74F649

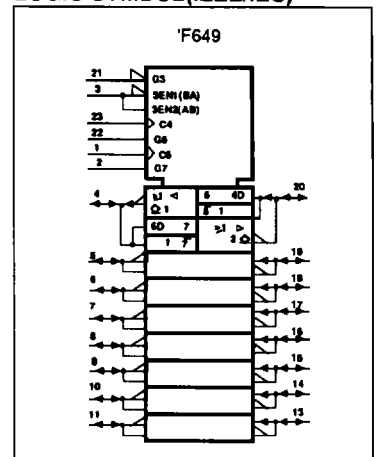
PIN CONFIGURATION



LOGIC SYMBOL



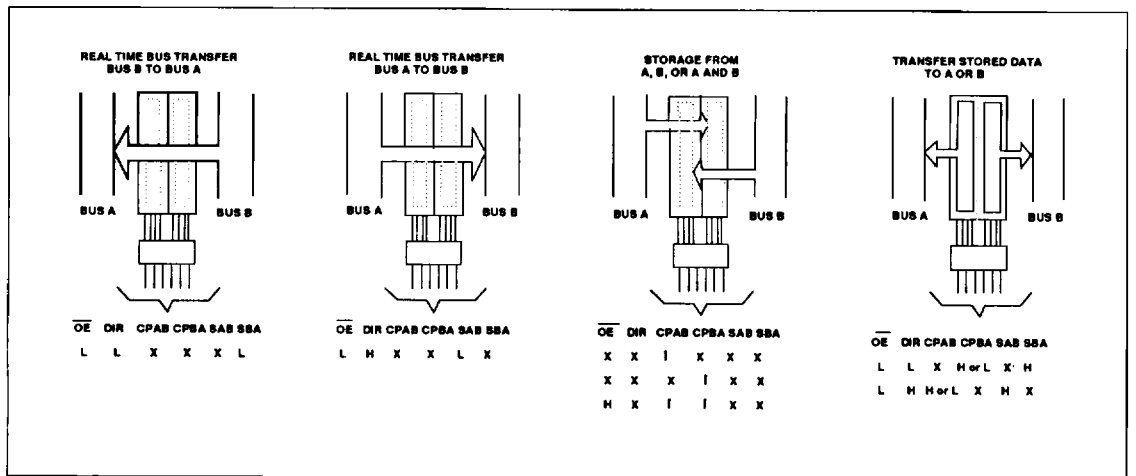
LOGIC SYMBOL (IEEE/IEC)



When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one

of the two busses, A or B, may be driven at a time. The following examples demonstrate the four fundamental bus-man-

agement functions that can be performed with the 'F647 and 'F649.



Transceivers/Registers

FAST 74F647, 74F649

FUNCTION TABLE

INPUTS						DATA I/O		OPERATING MODE	
OE	DIR	CPAB	CPBA	SAB	SBA	A ₀ -A ₇	B ₀ -B ₇	'F647	'F649
X	X	↑	X	X	X	Input	Unspecified*	Store A, B unspecified*	Store A, B unspecified*
X	X	X	↑	X	X	Unspecified*	Input	Store A, B unspecified*	Store A, B unspecified*
H	X	↑	↑	X	X	Input	Input	Store A and B data Isolation, hold storage	Store A and B data Isolation, hold storage
H	X	H or L	H or L	X	X	Input	Input	Store A and B data Isolation, hold storage	Store A and B data Isolation, hold storage
L	L	X	X	X	L	Output	Input	Real time B data to A bus Stored B data to A bus	Real time B data to A bus Stored B data to A bus
L	L	X	H or L	X	H	Output	Input	Real time B data to A bus Stored B data to A bus	Real time B data to A bus Stored B data to A bus
L	H	H or L	X	L	X	Input	Output	Real time A data to B bus Stored A data to B bus	Real time A data to B bus Stored A data to B bus
L	H	X	X	H	X	Input	Output	Real time A data to B bus Stored A data to B bus	Real time A data to B bus Stored A data to B bus

H= High voltage level

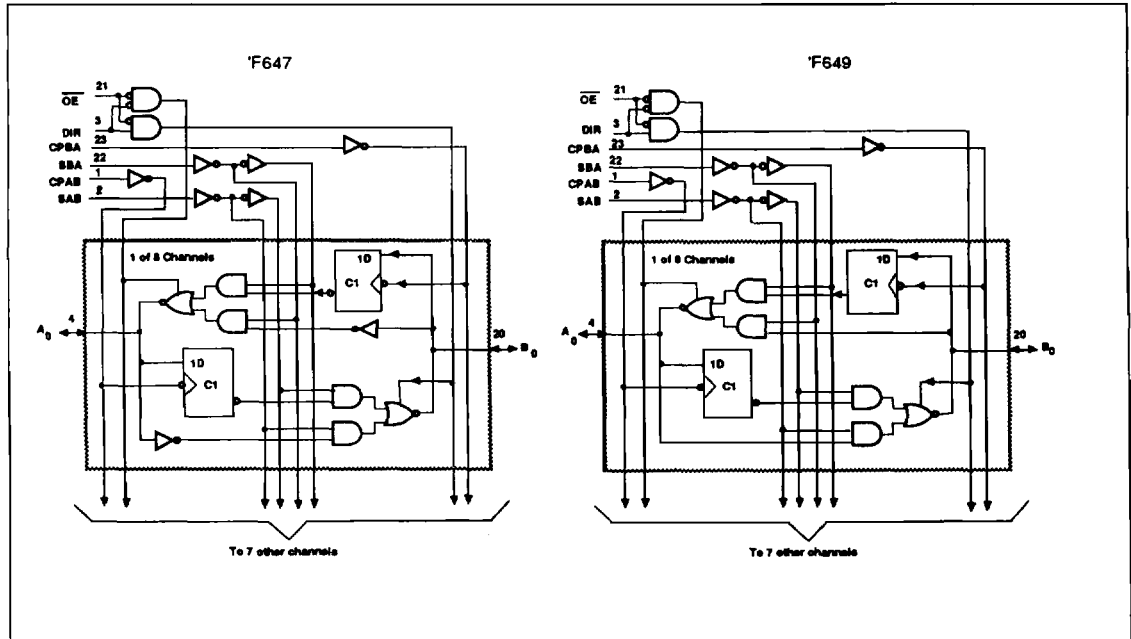
L= Low voltage level

X=Don't care

↑ =Low-to-High clock transition

*= The data output function may be enabled or disabled by various signals at the OE and DIR inputs. Data input functions are always enable, i.e., data at the bus pins will be stored on every Low-to-High transition of the clock.

LOGIC DIAGRAM



Transceivers/Registers

FAST 74F647, 74F649

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	128	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
V_{OH}	High-level output voltage			4.5	V
I_{OL}	Low-level output current			64	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS ¹	LIMITS			UNIT	
			Min	Typ ²	Max		
I_{OH}	High-level output current	$V_{CC} = \text{MIN}, V_{IL} = \text{MAX}, V_{IH} = \text{MIN}, V_{OH} = \text{MAX}$			250	μA	
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}$ $V_{IL} = \text{MAX}$ $V_{IH} = \text{MIN}$	$I_{OL} = 48\text{mA}$	$\pm 10\%V_{CC}$	0.38	0.55	V
			$I_{OL} = 64\text{mA}$	$\pm 5\%V_{CC}$	0.42	0.55	V
V_I	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = I_{IK}$			-0.73	-1.2	V
I_I	Input current at maximum input voltage	others	$V_{CC} = 0.0\text{V}, V_I = 7.0\text{V}$			100	μA
		A_n, B_n	$V_{CC} = 5.5\text{V}, V_I = 5.5\text{V}$			1	mA
I_{IH}	High-level input current	$V_{CC} = \text{MAX}, V_I = 2.7\text{V}$				20	μA
I_{IL}	Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.5\text{V}$				-20	μA
I_{CC}	Supply current (total)	I_{CCH}	$V_{CC} = \text{MAX}$		105	145	mA
		I_{CCL}			145	200	mA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at $V_{CC} = 5\text{V}, T_A = 25^\circ\text{C}$.

Transceivers/Registers

FAST 74F647, 74F649

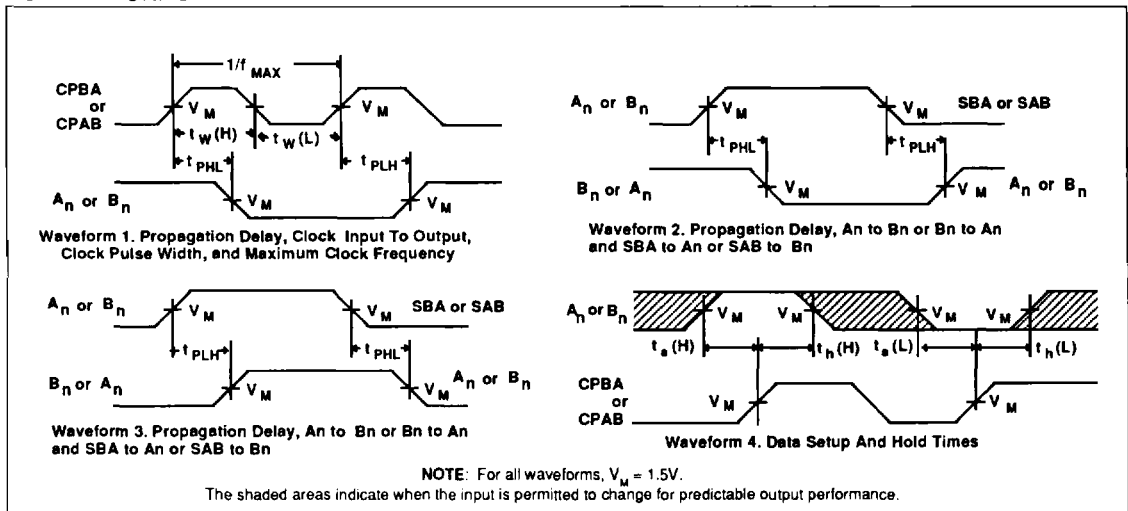
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			$T_A = +25^\circ\text{C}$ $V_{CC} = 5\text{V}$ $C_L = 50\text{pF}$ $R_L = 500\Omega$			$T_A = 0^\circ\text{C to } +70^\circ\text{C}$ $V_{CC} = 5\text{V} \pm 10\%$ $C_L = 50\text{pF}$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	50	65		40		MHz
t_{PLH} t_{PHL}	Propagation delay CPAB to B_n or CPBA to A_n	Waveform 1	10.0 5.5	15.0 8.5	18.0 11.0	10.0 5.5	19.5 12.0	ns
t_{PLH} t_{PHL}	Propagation delay A_n to B_n or B_n to A_n	Waveform 2 Waveform 3	10.5 4.0	13.5 7.0	16.5 9.5	10.5 4.0	19.0 10.5	ns
t_{PLH} t_{PHL}	Propagation delay SBA to A_n or SAB to B_n	Waveform 2 Waveform 3	10.5 4.0	14.5 7.0	17.5 9.5	10.5 4.0	20.0 10.5	ns
t_{PLH} t_{PHL}	Propagation delay OE to A_n or B_n	Waveform 2 Waveform 3	13.0 6.5	17.0 10.0	20.0 12.5	13.0 6.5	22.5 13.5	ns
t_{PLH} t_{PHL}	Propagation delay DIR to A_n or B_n	Waveform 2 Waveform 3	13.0 7.0	17.0 15.0	20.0 18.0	13.0 7.0	22.5 20.0	ns

AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			$T_A = +25^\circ\text{C}$ $V_{CC} = 5\text{V}$ $C_L = 50\text{pF}$ $R_L = 500\Omega$			$T_A = 0^\circ\text{C to } +70^\circ\text{C}$ $V_{CC} = 5\text{V} \pm 10\%$ $C_L = 50\text{pF}$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low A_n to CPBA or B_n to CPAB	Waveform 4	4.0 4.0			5.0 5.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low A_n to CPBA or B_n to CPAB	Waveform 4	0 0			0 0		ns
$t_w(H)$ $t_w(L)$	Pulse width, High or Low CPAB or CPBA	Waveform 1	4.5 6.0			4.5 6.5		ns

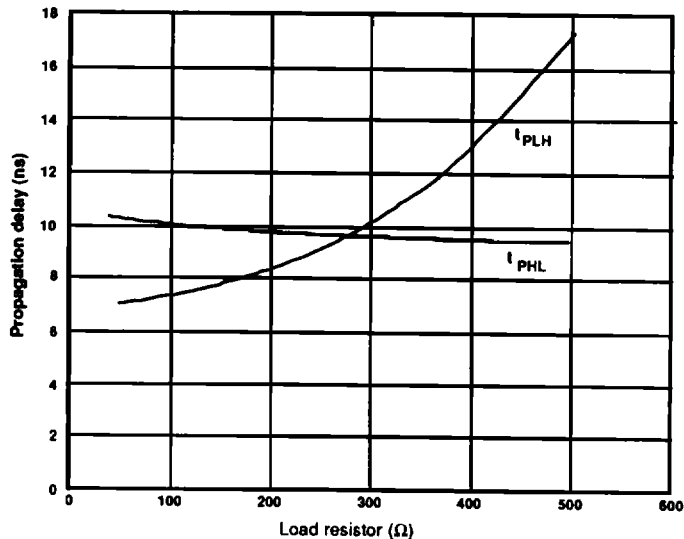
AC WAVEFORMS



Transceivers/Registers

FAST 74F647, 74F649

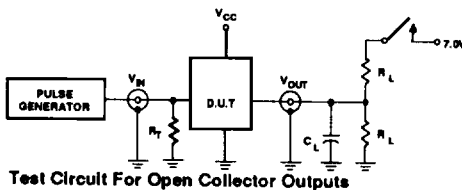
TYPICAL PROPAGATION DELAYS VERSUS LOAD FOR OPEN COLLECTOR OUTPUTS



NOTE:

When using Open-Collector parts, the value of the pull-up resistor greatly affects the value of the t_{PLH} . For example, changing the specified pull-up resistor value from 500Ω to 100Ω will improve the t_{PLH} up to 50% with only a slight increase in the t_{PHL} . However, if the value of the pull-up resistor is changed, the user must make certain that the total I_{OL} current through the resistor and the total I_L of the receivers does not exceed the I_{OL} maximum specification.

TEST CIRCUIT AND WAVEFORMS

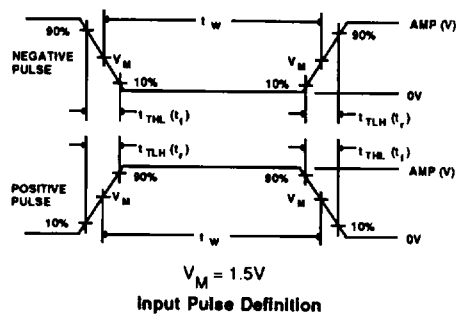


SWITCH POSITION

TEST	SWITCH
Open Collector	closed
All other	open

DEFINITIONS

- R_L = Load resistor; see AC CHARACTERISTICS for value.
- C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
- R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns