# DRAM

# 256K x 16 DRAM

## 3.3V, FAST PAGE MODE, OPTIONAL SELF REFRESH



## FEATURES

- Industry-standard x16 pinouts, timing, functions and packages
- High-performance CMOS silicon-gate process
- Single +3.3V ±0.3V power supply*
- Low power, 0.3mW standby; 150mW active, typical
- All device pins are fully LVTTL-compatible
- 512-cycle refresh in 8ms (MT4LC16257) or 64ms (MT4LC16257 S)
- Refresh modes: $\overline{RAS}$ ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR), HIDDEN and optional Extended and SELF
- FAST PAGE MODE access cycle
- BYTE WRITE access cycle
- BYTE READ access cycle
- Symmetrical addressing (nine rows, nine columns)

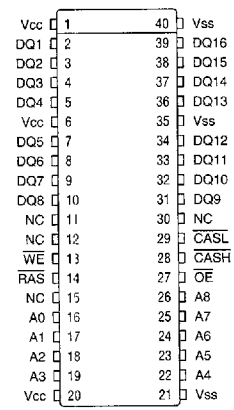
## OPTIONS — MARKING

- Timing
  - 60ns access — -6*
  - 70ns access — -7
  - 80ns access — -8
- Refresh Rate
  - 512-cycle refresh in 8ms — None
  - 512-cycle refresh in 64ms, SELF REFRESH — S
- Packages
  - Plastic SOJ (400 mil) — DJ
  - Plastic TSOP (400 mil) — TG
- Part Number Example: MT4LC16257DJ-7 S

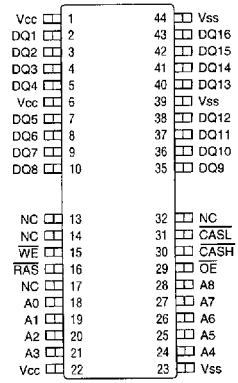
*60ns specifications are limited to a Vcc range of ±0.15V

## PIN ASSIGNMENT (Top View)

### 40-Pin SOJ (DA-7)




### 40/44-Pin TSOP (DB-4)




## KEY TIMING PARAMETERS

| SPEED | tRC | tRAC | tPC | tAA | tCAC | tRP |
|---|---|---|---|---|---|---|
| -6 | 110ns | 60ns | 35ns | 30ns | 15ns | 40ns |
| -7 | 130ns | 70ns | 40ns | 35ns | 20ns | 50ns |
| -8 | 150ns | 80ns | 45ns | 40ns | 20ns | 60ns |

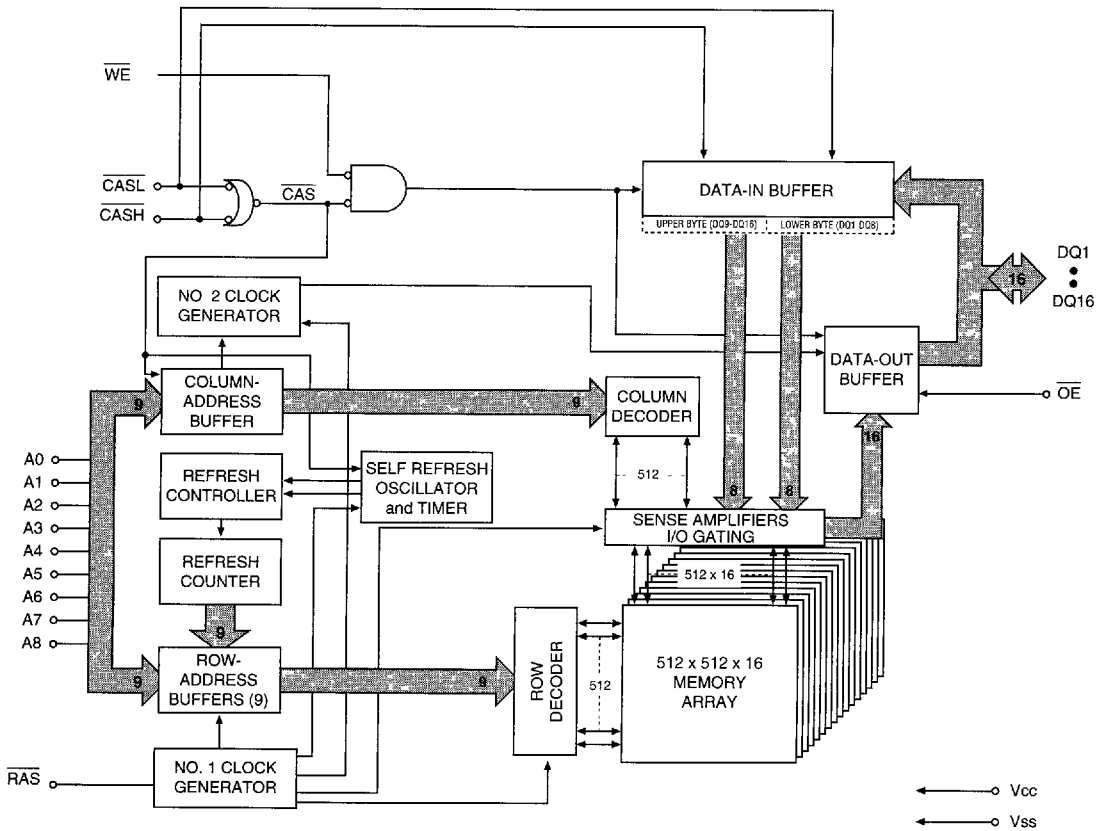
## GENERAL DESCRIPTION

The MT4LC16257(S) is a randomly accessed solid-state memory containing 4,194,304 bits organized in a x16 configuration. The MT4LC16257(S) has both BYTE WRITE and WORD WRITE access cycles via two $\overline{CAS}$ pins. $\overline{CASL}$ and $\overline{CASH}$ function in an identical manner to $\overline{CAS}$ in that either $\overline{CASL}$ or $\overline{CASH}$ will generate an internal $\overline{CAS}$.

The MT4LC16257(S) $\overline{CAS}$ function and timing are determined by the first $\overline{CAS}$ ($\overline{CASL}$ or $\overline{CASH}$) to transition LOW and by the last to transition back HIGH. Use of only one of the two results in a BYTE WRITE cycle. $\overline{CASL}$ transitioning LOW selects a WRITE cycle for the lower byte (DQ1-DQ8) and $\overline{CASH}$ transitioning LOW selects a WRITE cycle for the upper byte (DQ9-DQ16). BYTE READ cycles are achieved through $\overline{CASL}$ or $\overline{CASH}$ in the same manner during READ cycles for the MT4LC16257(S).

FPM DRAM

## FUNCTIONAL BLOCK DIAGRAM



## FUNCTIONAL DESCRIPTION

Each bit is uniquely addressed through the 18 address bits during READ or WRITE cycles. These are entered 9 bits (A0-A8) at a time. $\overline{RAS}$ is used to latch the first 9 bits and $\overline{CAS}$ the latter 9 bits.

The $\overline{CAS}$ control also determines whether the cycle will be a refresh cycle ($\overline{RAS}$ ONLY) or an active cycle (READ, WRITE or READ WRITE) once $\overline{RAS}$ goes LOW.

The $\overline{CASL}$ and $\overline{CASH}$ inputs internally generate a $\overline{CAS}$ signal functioning in an identical manner to the single $\overline{CAS}$ input on the other 256K x 16 DRAMs. The key difference is each $\overline{CAS}$ controls its corresponding DQ tristate logic (in conjunction with $\overline{OE}$ and $\overline{WE}$). $\overline{CASL}$ controls DQ1 through DQ8 and $\overline{CASH}$ controls DQ9 through DQ16.

The $\overline{CAS}$ function is determined by the first $\overline{CAS}$ ($\overline{CASL}$ or $\overline{CASH}$) to transition LOW and the last one to transition back HIGH. The two $\overline{CAS}$ controls provide BYTE READ and BYTE WRITE cycle capabilities.

A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. Taking $\overline{WE}$ LOW will initiate a WRITE cycle, selecting DQ1 through DQ16. If $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, the output pin(s) remain open (High- Z) until the next $\overline{CAS}$ cycle. If $\overline{WE}$ goes LOW after $\overline{CAS}$ goes LOW and data reaches the output pins, data-out (Q) is activated and retains the selected cell data as long as $\overline{CAS}$ and $\overline{OE}$ remain LOW (regardless of $\overline{WE}$ or $\overline{RAS}$). This late $\overline{WE}$ pulse results in a READ WRITE cycle.

The 16 data inputs and 16 data outputs are routed through 16 pins using common I/O and pin direction is controlled by $\overline{OE}$.

FAST PAGE MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row-address-defined (A0-A8) page boundary. The FAST PAGE MODE cycle is always initiated with a row-address strobed-in by $\overline{RAS}$ followed by a column-address strobed-in by $\overline{CAS}$. $\overline{CAS}$ may be toggled by holding $\overline{RAS}$ LOW and strobing-in different column-addresses, thus executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the FAST PAGE MODE operation.

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. The chip is also preconditioned for the next cycle during the $\overline{RAS}$ high time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE) or $\overline{RAS}$ refresh cycle ($\overline{RAS}$ ONLY, CBR, or HIDDEN) so that all 512 combinations of $\overline{RAS}$ addresses (A0-A8) are executed at least every 8ms, regardless of sequence. The CBR REFRESH cycle will also invoke the refresh counter and controller for row-address control.

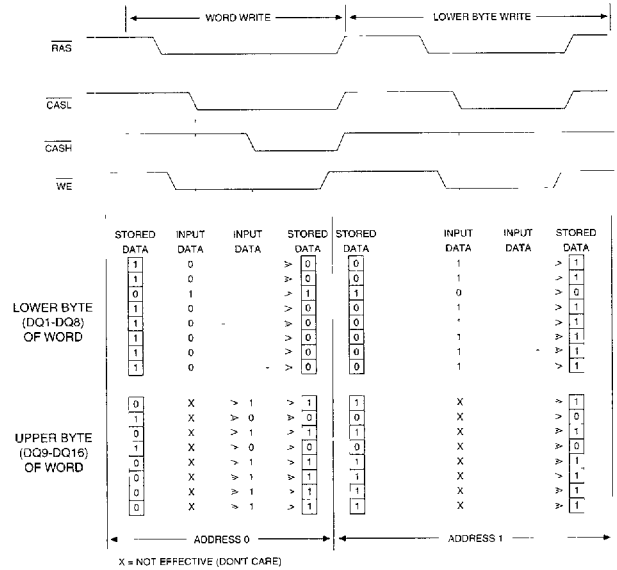



**Figure 1**
**WORD AND BYTE WRITE EXAMPLE**

### BYTE ACCESS CYCLE

The BYTE WRITE mode is determined by the use of $\overline{CASL}$ and $\overline{CASH}$. Enabling $\overline{CASL}$ will select a lower BYTE WRITE cycle (DQ1-DQ8) while enabling $\overline{CASH}$ will select an upper BYTE WRITE cycle (DQ9-DQ16). Enabling both $\overline{CASL}$ and $\overline{CASH}$ selects a WORD WRITE cycle.

The MT4LC16257(S) can be viewed as two 256K x 8 DRAMS which have common input controls, with the exception of the $\overline{CAS}$ inputs. Figure 1 illustrates the MT4LC16257(S) BYTE WRITE and WORD WRITE cycles.

The MT4LC16257(S) also has BYTE READ and WORD READ cycles, since it uses two $\overline{CAS}$ inputs to control its byte accesses. Figure 2 illustrates the MT4LC16257(S) BYTE READ and WORD READ cycles.

## REFRESH

An optional SELF REFRESH mode is also available. The "S" version allows the user the choice of a fully static low-power data retention mode or a dynamic refresh mode at the extended refresh period.

The optional SELF REFRESH feature is initiated by performing a CBR REFRESH cycle and holding $\overline{RAS}$ LOW for the specified $^{t}RASS$. Additionally, the "S" version allows for an extended refresh rate of 125µs per row if using distributed CBR REFRESH. This refresh rate can be applied during normal operation or during a standby mode.

The SELF REFRESH mode is terminated by driving $\overline{RAS}$ HIGH for a minimum time of $^{t}RPS$ ($\approx ^{t}RC$). This delay allows for the completion of any internal refresh cycles that may be in process at the time of the $\overline{RAS}$ LOW-to-HIGH transition. If the DRAM controller uses a distributed CBR REFRESH sequence, a burst refresh is not required upon exiting SELF REFRESH mode. However, if the DRAM controller utilizes $\overline{RAS}$ ONLY or burst refresh sequence, all rows must be refreshed within 300µs prior to the resumption of normal operation.

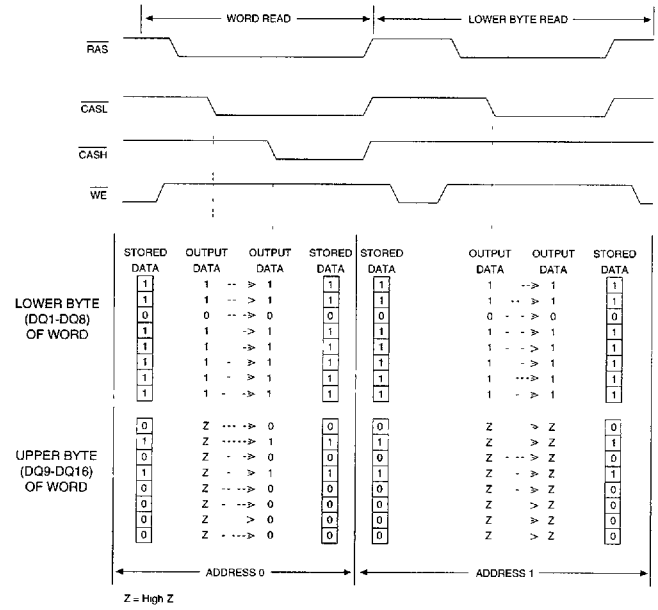



**Figure 2**
**WORD AND BYTE READ EXAMPLE**

## TRUTH TABLE

| FUNCTION | | RAS | CASL | CASH | WE | OE | ADDRESSES tR | ADDRESSES tC | DQs | NOTES |
|---|---|---|---|---|---|---|---|---|---|---|
| Standby | | H | H→X | H→X | X | X | X | X | High-Z | |
| READ: WORD | | L | L | L | H | L | ROW | COL | Data-Out | |
| READ: LOWER BYTE | | L | L | H | H | L | ROW | COL | Lower Byte, Data-Out<br>Upper Byte, High-Z | |
| READ: UPPER BYTE | | L | H | L | H | L | ROW | COL | Lower Byte, High-Z<br>Upper Byte, Data-Out | |
| WRITE: WORD (EARLY WRITE) | | L | L | L | L | X | ROW | COL | Data-In | |
| WRITE: LOWER BYTE (EARLY) | | L | L | H | L | X | ROW | COL | Lower Byte, Data-In<br>Upper Byte, High-Z | |
| WRITE: UPPER BYTE (EARLY) | | L | H | L | L | X | ROW | COL | Lower Byte, High-Z<br>Upper Byte, Data-In | |
| READ WRITE | | L | L | L | H→L | L→H | ROW | COL | Data-Out, Data-In | 1, 2 |
| PAGE-MODE READ | 1st Cycle | L | H→L | H→L | H | L | ROW | COL | Data-Out | 2 |
| | 2nd Cycle | L | H→L | H→L | H | L | n/a | COL | Data-Out | 2 |
| PAGE-MODE WRITE | 1st Cycle | L | H→L | H→L | L | X | ROW | COL | Data-In | 1 |
| | 2nd Cycle | L | H→L | H→L | L | X | n/a | COL | Data-In | 1 |
| PAGE-MODE READ-WRITE | 1st Cycle | L | H→L | H→L | H→L | L→H | ROW | COL | Data-Out, Data-In | 1, 2 |
| | 2nd Cycle | L | H→L | H→L | H→L | L→H | n/a | COL | Data-Out, Data-In | 1, 2 |
| HIDDEN REFRESH | READ | L→H→L | L | L | H | L | ROW | COL | Data-Out | 2 |
| | WRITE | L→H→L | L | L | L | X | ROW | COL | Data-In | 1, 3 |
| RAS-ONLY REFRESH | | L | H | H | X | X | ROW | n/a | High-Z | |
| CBR REFRESH | | H→L | L | L | X | X | X | X | High-Z | 4 |
| SELF REFRESH (MT4C16257 S only) | | H→L | L | X | X | X | X | X | High-Z | |

**NOTE:** 1. These WRITE cycles may also be BYTE WRITE cycles (either CASL or CASH active).
2. These READ cycles may also be BYTE READ cycles (either CASL or CASH active).
3. EARLY WRITE only.
4. At least one of the two CAS signals must be active (CASL or CASH).

## ABSOLUTE MAXIMUM RATINGS*

Voltage on $V_{CC}$ Supply Relative to $V_{SS}$ ..... -1V to +4.6V
Operating Temperature, $T_A$ (ambient) ..... 0°C to +70°C
Storage Temperature (plastic) ..... -55°C to +150°C
Power Dissipation ..... 1.2W
Short Circuit Output Current ..... 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 6, 7) (0°C ≤ $T_A$ ≤ 70°C; $V_{CC}$ = +3.3V ±0.3V**)

| PARAMETER/CONDITION | SYMBOL | MIN | MAX | UNITS | NOTES |
|---|---|---|---|---|---|
| Supply Voltage | $V_{CC}$** | 3.0 | 3.6 | V | |
| Input High (Logic 1) Voltage, all inputs | $V_{IH}$ | 2.0 | $V_{CC}$+1 | V | |
| Input Low (Logic 0) Voltage, all inputs | $V_{IL}$ | -1.0 | 0.8 | V | |
| INPUT LEAKAGE CURRENT<br>Any input 0V ≤ $V_{IN}$ ≤ Vcc<br>(All other pins not under test = 0V) | $I_I$ | -2 | 2 | µA | |
| OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ $V_{OUT}$ ≤ 3.6V) | $I_{OZ}$ | -10 | 10 | µA | |
| OUTPUT LEVELS<br>Output High Voltage ($I_{OUT}$ = -2mA) | $V_{OH}$ | 2.4 | | V | |
| Output Low Voltage ($I_{OUT}$ = 2mA) | $V_{OL}$ | | 0.4 | V | |

**60ns specifications are limited to a $V_{CC}$ range of ±0.15V.

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 6, 7) ($V_{CC}$ = +3.3V ±0.3V**)

| PARAMETER/CONDITION | SYMBOL | MAX -6** | MAX -7 | MAX -8 | UNITS | NOTES |
|---|---|---|---|---|---|---|
| STANDBY CURRENT: (TTL)<br>($\overline{RAS}$ = $\overline{CAS}$ = $V_{IH}$) | | $I_{CC1}$ | 1 | 1 | 1 | mA |
| STANDBY CURRENT: (CMOS)<br>($\overline{RAS}$ = $\overline{CAS}$ = $V_{CC}$ -0.2V) | $I_{CC2}$ | 500 | 500 | 500 | µA | 25 |
| | $I_{CC2}$ (S only) | 100 | 100 | 100 | µA | 25 |
| OPERATING CURRENT: Random READ/WRITE<br>Average power supply current<br>($\overline{RAS}$, $\overline{CAS}$, Address Cycling: $^tRC$ = $^tRC$ [MIN]) | $I_{CC3}$ | 120 | 110 | 100 | mA | 3, 4, 40 |
| OPERATING CURRENT: FAST PAGE MODE<br>Average power supply current<br>($\overline{RAS}$ = $V_{IL}$, $\overline{CAS}$, Address Cycling:<br>$^tPC$ = $^tPC$ [MIN]; $^tCP$, $^tASC$ = 10ns) | $I_{CC4}$ | 70 | 60 | 50 | mA | 3, 4, 40 |
| REFRESH CURRENT: $\overline{RAS}$ ONLY<br>Average power supply current<br>($\overline{RAS}$ Cycling, $\overline{CAS}$ = $V_{IH}$: $^tRC$ = $^tRC$ [MIN]) | $I_{CC5}$ | 120 | 110 | 100 | mA | 3 |
| REFRESH CURRENT: CBR<br>Average power supply current<br>($\overline{RAS}$, $\overline{CAS}$, Address Cycling: $^tRC$ = $^tRC$ [MIN]) | $I_{CC6}$ | 120 | 110 | 100 | mA | 3, 5 |
| REFRESH CURRENT: Extended (S version only)<br>Average power supply current, $\overline{CAS}$ = 0.2V or CBR cycling;<br>$^tRAS$ = $^tRAS$ (MIN); $\overline{WE}$, A0-A8 and $D_{IN}$ = Vcc-0.2V or 0.2V<br>($D_{IN}$ may be left open) | $I_{CC7}$ (S only) | 150 | 150 | 150 | µA | 3, 5 |
| REFRESH CURRENT: SELF (S version only)<br>Average power supply current, CBR cycling with $^tRAS \geq {}^tRASS$ (MIN)<br>and $\overline{CAS}$ held LOW; $\overline{WE}$ = Vcc-0.2V; A0-A8 and<br>$D_{IN}$ = Vcc-0.2V or 0.2V ($D_{IN}$ may be left open) | $I_{CC8}$ (S only) | 150 | 150 | 150 | µA | 5, 41 |

**60ns specifications are limited to a $V_{CC}$ range of ±0.15V.

## CAPACITANCE

| PARAMETER | SYMBOL | MAX | UNITS | NOTES |
|---|---|---|---|---|
| Input Capacitance: A0-A8 | $C_{I1}$ | 5 | pF | 2 |
| Input Capacitance: $\overline{RAS}$, $\overline{CASL}$, $\overline{CASH}$, $\overline{WE}$, $\overline{OE}$ | $C_{I2}$ | 7 | pF | 2 |
| Input/Output Capacitance: DQ (SOJ, TSOP) | $C_{IO}$ | 7 | pF | 2 |

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) ($V_{CC}$ = +3.3V ±0.3V*)

| AC CHARACTERISTICS | | -6* | | -7 | | -8 | | | |
|---|---|---|---|---|---|---|---|---|---|
| PARAMETER | SYM | MIN | MAX | MIN | MAX | MIN | MAX | UNITS | NOTES |
| Access time from column-address | $^tAA$ | | 30 | | 35 | | 40 | ns | |
| Column-address hold time (referenced to $\overline{RAS}$) | $^tAR$ | 50 | | 55 | | 60 | | ns | |
| Column-address setup time | $^tASC$ | 0 | | 0 | | 0 | | ns | 29 |
| Row-address setup time | $^tASR$ | 0 | | 0 | | 0 | | ns | |
| Column-address to $\overline{WE}$ delay time | $^tAWD$ | 55 | | 60 | | 65 | | ns | 21 |
| Access time from $\overline{CAS}$ | $^tCAC$ | | 15 | | 20 | | 20 | ns | 15, 31 |
| Column-address hold time | $^tCAH$ | 10 | | 15 | | 15 | | ns | 29 |
| $\overline{CAS}$ pulse width | $^tCAS$ | 15 | 10,000 | 20 | 10,000 | 20 | 10,000 | ns | 37 |
| $\overline{CAS}$ hold time entering SELF REFRESH | $^tCHD$ | 10 | | 10 | | 10 | | ns | 41 |
| $\overline{CAS}$ hold time (CBR REFRESH) | $^tCHR$ | 10 | | 10 | | 10 | | ns | 5, 30 |
| Last $\overline{CAS}$ going LOW to first $\overline{CAS}$ returning HIGH | $^tCLCH$ | 10 | | 10 | | 10 | | ns | 32 |
| $\overline{CAS}$ to output in Low-Z | $^tCLZ$ | 3 | | 3 | | 3 | | ns | 31 |
| $\overline{CAS}$ precharge time | $^tCP$ | 10 | | 10 | | 10 | | ns | 16, 34 |
| Access time from $\overline{CAS}$ precharge | $^tCPA$ | | 35 | | 40 | | 45 | ns | 31 |
| $\overline{CAS}$ to $\overline{RAS}$ precharge time | $^tCRP$ | 8 | | 10 | | 10 | | ns | 30 |
| $\overline{CAS}$ hold time | $^tCSH$ | 60 | | 70 | | 80 | | ns | 30 |
| $\overline{CAS}$ setup time (CBR REFRESH) | $^tCSR$ | 10 | | 10 | | 10 | | ns | 5, 29 |
| $\overline{CAS}$ to $\overline{WE}$ delay time | $^tCWD$ | 40 | | 45 | | 45 | | ns | 21, 29 |
| Write command to $\overline{CAS}$ lead time | $^tCWL$ | 15 | | 20 | | 20 | | ns | 26, 30 |
| Data-in hold time | $^tDH$ | 10 | | 15 | | 15 | | ns | 22, 31 |
| Data-in hold time (referenced to $\overline{RAS}$) | $^tDHR$ | 45 | | 55 | | 60 | | ns | |
| Data-in setup time | $^tDS$ | 0 | | 0 | | 0 | | ns | 22, 31 |
| Output disable time | $^tOD$ | 3 | 15 | 3 | 15 | 3 | 15 | ns | 28, 39 |
| Output Enable time | $^tOE$ | | 15 | | 20 | | 20 | ns | 31 |
| $\overline{OE}$ hold time from $\overline{WE}$ during READ-MODIFY-WRITE cycle | $^tOEH$ | 15 | | 20 | | 20 | | ns | 27 |
| Output buffer turn-off delay | $^tOFF$ | 3 | 15 | 3 | 15 | 3 | 15 | ns | 20, 28, 31 |
| $\overline{OE}$ setup prior to $\overline{RAS}$ during HIDDEN REFRESH cycle | $^tORD$ | 0 | | 0 | | 0 | | ns | |

*60ns specifications are limited to a $V_{CC}$ range of ±0.15V.

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (Vcc = +3.3V ±0.3V*)

| AC CHARACTERISTICS | | -6* | | -7 | | -8 | | | |
|---|---|---|---|---|---|---|---|---|---|
| PARAMETER | SYM | MIN | MAX | MIN | MAX | MIN | MAX | UNITS | NOTES |
| FAST-PAGE-MODE READ or WRITE cycle time | tPC | 35 | | 40 | | 45 | | ns | 33 |
| FAST-PAGE-MODE READ-WRITE cycle time | tPRWC | 85 | | 95 | | 100 | | ns | 33 |
| Access time from $\overline{RAS}$ | tRAC | | 60 | | 70 | | 80 | ns | 14 |
| $\overline{RAS}$ to column-address delay time | tRAD | 15 | 30 | 15 | 35 | 15 | 40 | ns | 18 |
| Row-address hold time | tRAH | 10 | | 10 | | 10 | | ns | |
| Column-address to $\overline{RAS}$ lead time | tRAL | 30 | | 35 | | 40 | | ns | |
| $\overline{RAS}$ pulse width | tRAS | 60 | 10,000 | 70 | 10,000 | 80 | 10,000 | ns | |
| $\overline{RAS}$ pulse width (PAGE MODE) | tRASP | 60 | 100,000 | 70 | 100,000 | 80 | 100,000 | ns | |
| $\overline{RAS}$ pulse width entering SELF REFRESH | tRASS | 100 | | 100 | | 100 | | µs | 41 |
| Random READ or WRITE cycle time | tRC | 110 | | 130 | | 150 | | ns | |
| $\overline{RAS}$ to $\overline{CAS}$ delay time | tRCD | 20 | 45 | 20 | 50 | 20 | 60 | ns | 17, 29 |
| Read command hold time (referenced to $\overline{CAS}$) | tRCH | 0 | | 0 | | 0 | | ns | 19, 26, 30 |
| Read command setup time | tRCS | 0 | | 0 | | 0 | | ns | 26, 29 |
| Refresh period (512 cycles) MT4LC16257 / MT4LC16257 S | tREF | | 8/64 | | 8/64 | | 8/64 | ms | |
| $\overline{RAS}$ precharge time | tRP | 40 | | 50 | | 60 | | ns | |
| $\overline{RAS}$ to $\overline{CAS}$ precharge time | tRPC | 10 | | 10 | | 10 | | ns | |
| $\overline{RAS}$ precharge time exiting SELF REFRESH | tRPS | 110 | | 130 | | 150 | | µs | 41 |
| Read command hold time (referenced to $\overline{RAS}$) | tRRH | 0 | | 0 | | 0 | | ns | 19 |
| $\overline{RAS}$ hold time | tRSH | 15 | | 20 | | 20 | | ns | 38 |
| READ WRITE cycle time | tRWC | 150 | | 175 | | 195 | | ns | |
| $\overline{RAS}$ to $\overline{WE}$ delay time | tRWD | 85 | | 95 | | 105 | | ns | 21 |
| Write command to $\overline{RAS}$ lead time | tRWL | 15 | | 20 | | 20 | | ns | 26 |
| Transition time (rise or fall) | tT | 3 | 50 | 3 | 50 | 3 | 50 | ns | |
| Write command hold time | tWCH | 10 | | 10 | | 10 | | ns | 26, 38 |
| Write command hold time (referenced to $\overline{RAS}$) | tWCR | 45 | | 55 | | 60 | | ns | 26 |
| Write command setup time | tWCS | 0 | | 0 | | 0 | | ns | 21, 26, 29 |
| Write command pulse width | tWP | 10 | | 10 | | 10 | | ns | 26 |

*60ns specifications are limited to a Vcc range of ±0.15V.

## NOTES

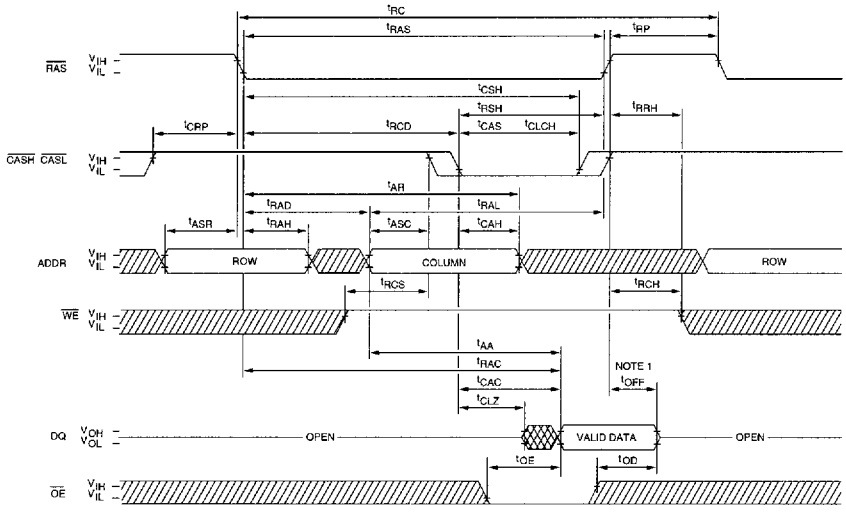
1. All voltages referenced to $V_{SS}$.
2. This parameter is sampled. $V_{CC}$ = +3.3V; f = 1 MHz.
3. $I_{CC}$ is dependent on cycle rates.
4. $I_{CC}$ is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \le T_A \le 70°C$) is assured.
7. An initial pause of 100µs is required after power-up followed by eight $\overline{RAS}$ refresh cycles ( $\overline{RAS}$ ONLY or CBR) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-ups should be repeated any time the $^tREF$ refresh requirement is exceeded.
8. AC characteristics assume $^tT$ = 5ns.
9. $V_{IH}$ (MIN) and $V_{IL}$ (MAX) are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH}$ and $V_{IL}$ (or between $V_{IL}$ and $V_{IH}$).
10. In addition to meeting the transition rate specification, all input signals must transit between $V_{IH}$ and $V_{IL}$ (or between $V_{IL}$ and $V_{IH}$) in a monotonic manner.
11. If $\overline{CAS}$ = $V_{IH}$, data output is High-Z.
12. If $\overline{CAS}$ = $V_{IL}$, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to one TTL gates and 50pF, $V_{OL}$ = 0.80 and $V_{OH}$ = 2.0V.
14. Assumes that $^tRCD < ^tRCD$ (MAX). If $^tRCD$ is greater than the maximum recommended value shown in this table, $^tRAC$ will increase by the amount that $^tRCD$ exceeds the value shown.
15. Assumes that $^tRCD \ge ^tRCD$ (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the Q buffer, $\overline{CAS}$ must be pulsed HIGH for $^tCP$.
17. Operation within the $^tRCD$ (MAX) limit ensures that $^tRAC$ (MAX) can be met. $^tRCD$ (MAX) is specified as a reference point only; if $^tRCD$ is greater than the specified $^tRCD$ (MAX) limit, access time is controlled exclusively by $^tCAC$.
18. Operation within the $^tRAD$ limit ensures that $^tRCD$ (MAX) can be met. $^tRAD$ (MAX) is specified as a reference point only; if $^tRAD$ is greater than the specified $^tRAD$ (MAX) limit, access time is controlled exclusively by $^tAA$.
19. Either $^tRCH$ or $^tRRH$ must be satisfied for a READ cycle.
20. $^tOFF$ (MAX) defines the time at which the output achieves the open circuit condition; it is not a reference to $V_{OH}$ or $V_{OL}$. The 3ns minimum is a parameter guaranteed by design.
21. $^tWCS$, $^tRWD$, $^tAWD$ and $^tCWD$ are restrictive operating parameters in LATE WRITE and READ-MODIFY-WRITE cycles only. If $^tWCS \ge ^tWCS$ (MIN), the cycle is an EARLY WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $^tRWD \ge ^tRWD$ (MIN), $^tAWD \ge ^tAWD$ (MIN) and $^tCWD \ge ^tCWD$ (MIN), the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of Q (at access time and until $\overline{CAS}$ or $\overline{OE}$ goes back to $V_{IH}$) is indeterminate. $\overline{OE}$ held HIGH and $\overline{WE}$ taken LOW after $\overline{CAS}$ goes LOW results in a LATE WRITE ($\overline{OE}$-controlled) cycle.
22. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY WRITE cycles and $\overline{WE}$ leading edge in LATE WRITE or READ-MODIFY-WRITE cycles.
23. During a READ cycle, if $\overline{OE}$ is LOW then taken HIGH before $\overline{CAS}$ goes HIGH, Q goes open. If $\overline{OE}$ is tied permanently LOW, a LATE WRITE or READ-MODIFY-WRITE operation is not possible.
24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW and $\overline{OE}$ = HIGH.
25. All other inputs at $V_{CC}$ -0.2V.
26. Write command is defined as $\overline{WE}$ going LOW on the MT4LC16257(S).
27. LATE WRITE and READ-MODIFY-WRITE cycles must have both $^tOD$ and $^tOEH$ met ($\overline{OE}$ HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide the previously written data if $\overline{CAS}$ remains LOW and $\overline{OE}$ is taken back LOW after $^tOEH$ is met. If $\overline{CAS}$ goes HIGH prior to $\overline{OE}$ going back LOW, the DQs will remain open.
28. The DQs open during READ cycles once $^tOD$ or $^tOFF$ occur. If $\overline{CAS}$ goes HIGH before $\overline{OE}$, the DQs will open regardless of the state of the $\overline{OE}$. If $\overline{CAS}$ stays LOW while $\overline{OE}$ is brought HIGH, the DQs will open. If $\overline{OE}$ is brought back LOW ($\overline{CAS}$ still LOW), the DQs will provide the previously read data.
29. The first $\overline{CAS}$x edge to transition LOW.
30. The last $\overline{CAS}$x edge to transition HIGH.
31. Output parameter (DQx) is referenced to corresponding $\overline{CAS}$ input, DQ1-DQ8 by $\overline{CASL}$ and DQ9-DQ16 by $\overline{CASH}$.

## NOTES (continued)

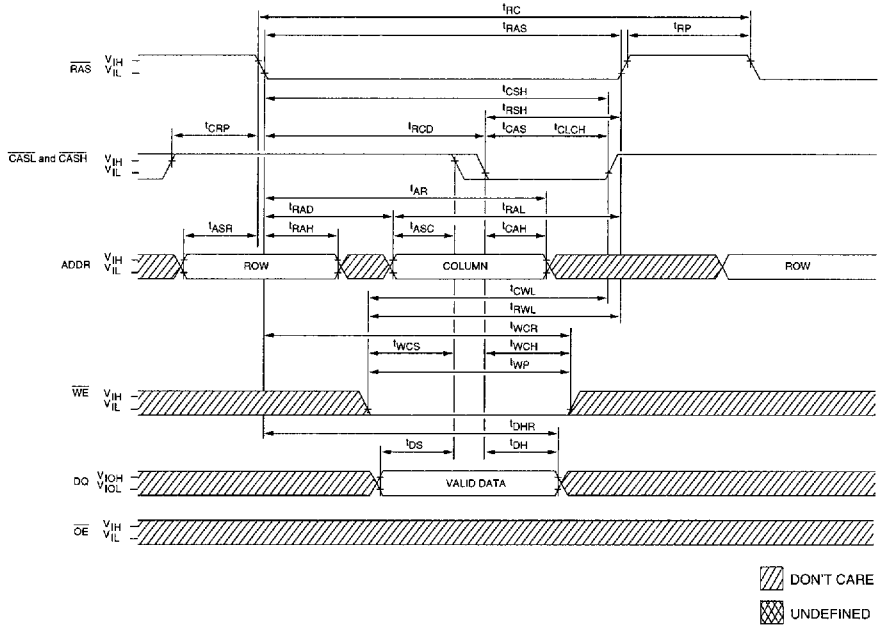
32. Last falling $\overline{CAS}$x edge to first rising $\overline{CAS}$x edge.
33. Last rising $\overline{CAS}$x edge to next cycle's last rising $\overline{CAS}$x edge.
34. Last rising $\overline{CAS}$x edge to first falling $\overline{CAS}$x edge.
35. First DQs controlled by the first $\overline{CAS}$x to go LOW.
36. Last DQs controlled by the last $\overline{CAS}$x to go HIGH.
37. Each $\overline{CAS}$x must meet minimum pulse width.
38. Last $\overline{CAS}$x to go LOW.
39. All DQs controlled, regardless of $\overline{CASL}$ and $\overline{CASH}$.
40. Column-address changed once while $\overline{RAS}$ = $V_{IL}$ and $\overline{CAS}$ = $V_{IH}$.
41. If the DRAM controller uses a burst refresh, a burst refresh of all rows must be executed upon exiting SELF REFRESH.

FPM DRAM

## READ CYCLE

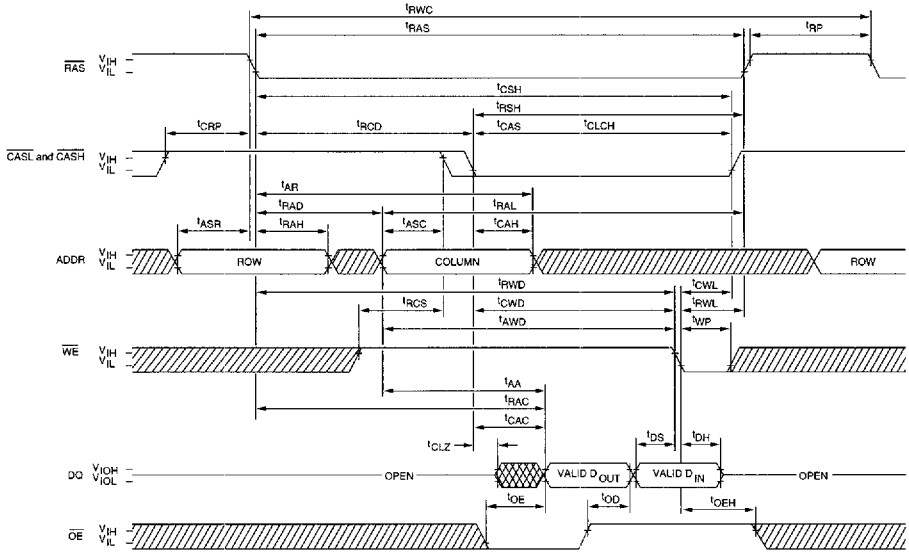



## EARLY WRITE CYCLE

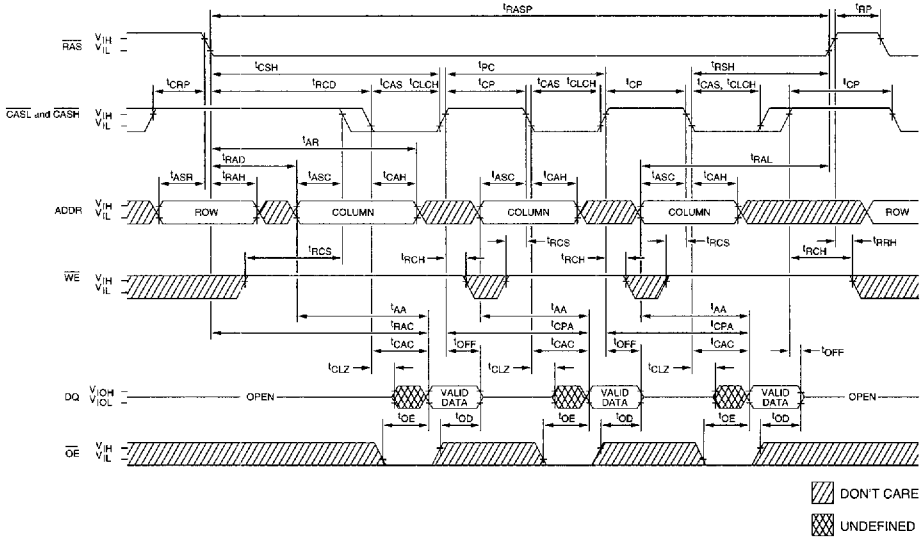


## READ WRITE CYCLE

(LATE WRITE and READ-MODIFY-WRITE cycles)




## FAST-PAGE-MODE READ CYCLE



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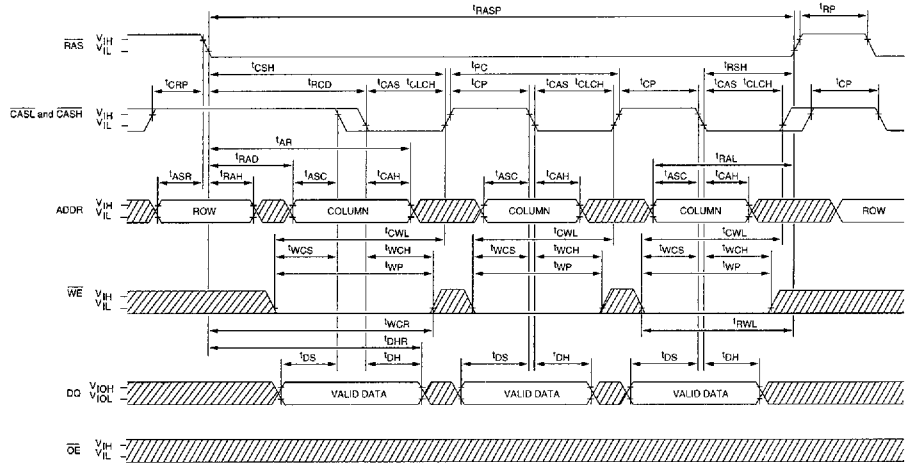
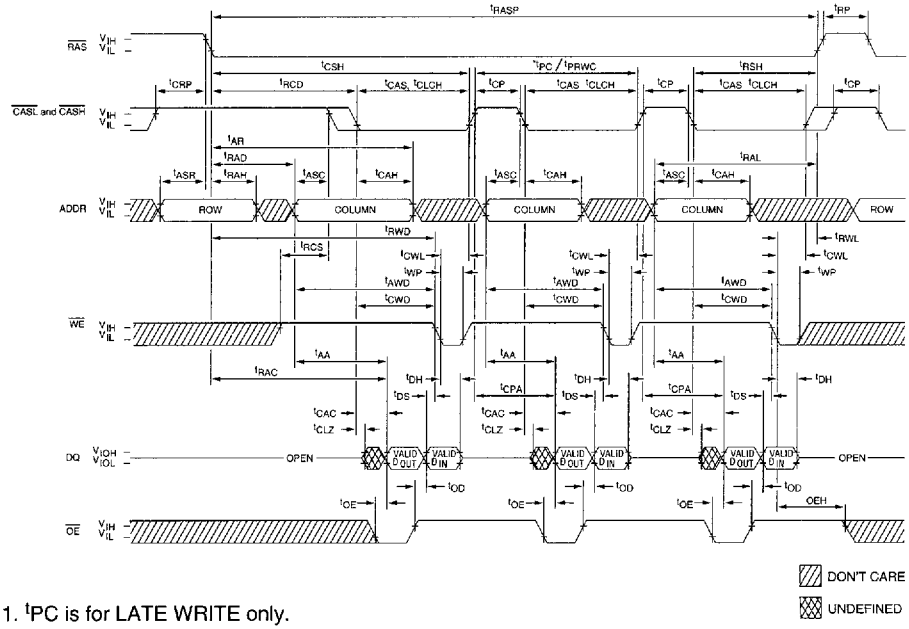
## FAST-PAGE-MODE EARLY WRITE CYCLE



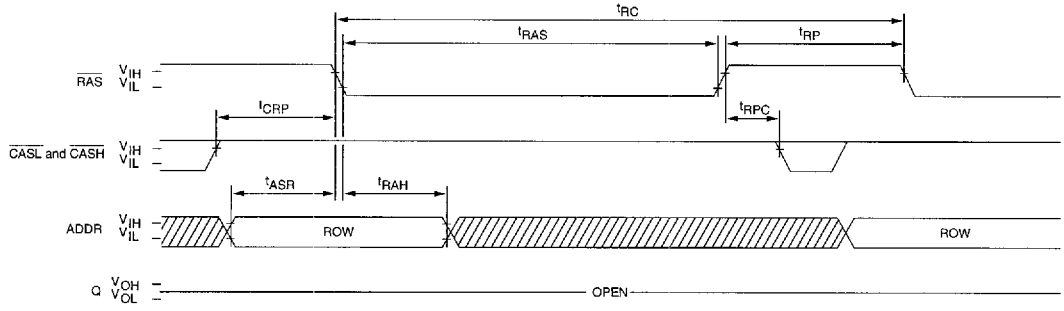

## FAST-PAGE-MODE READ-WRITE CYCLE

(LATE WRITE and READ-MODIFY-WRITE cycles)

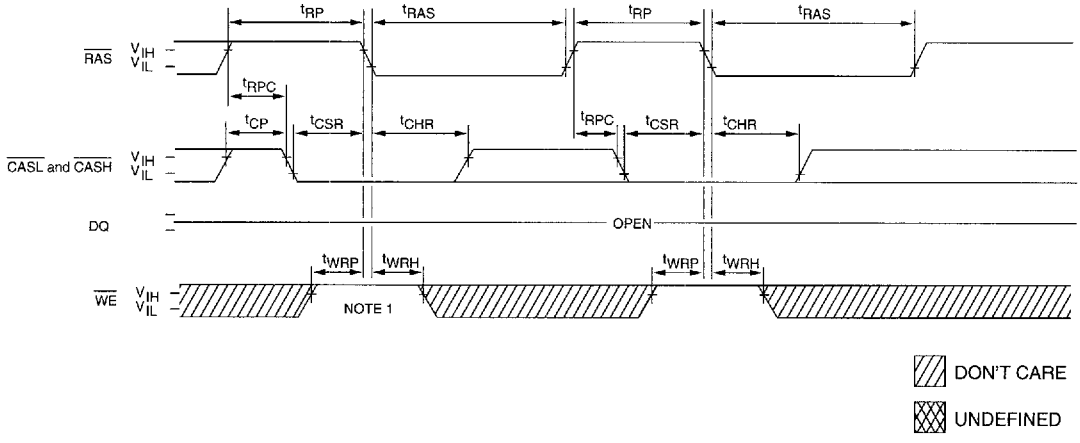



***NOTE:** 1. tPC is for LATE WRITE only.

## RAS-ONLY REFRESH CYCLE
(OE and WE = DON'T CARE)

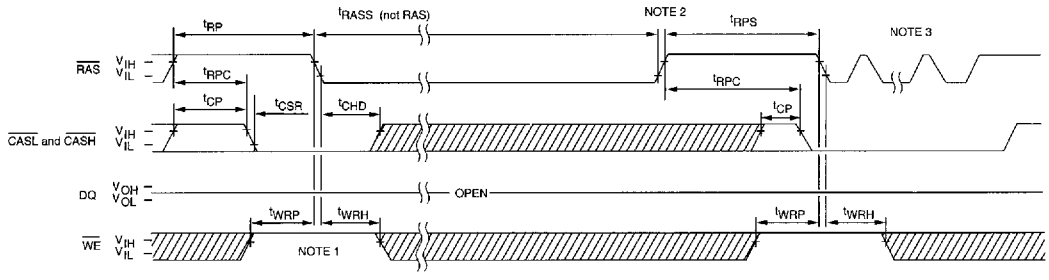



## CBR REFRESH CYCLE
(Addresses and OE = DON'T CARE)

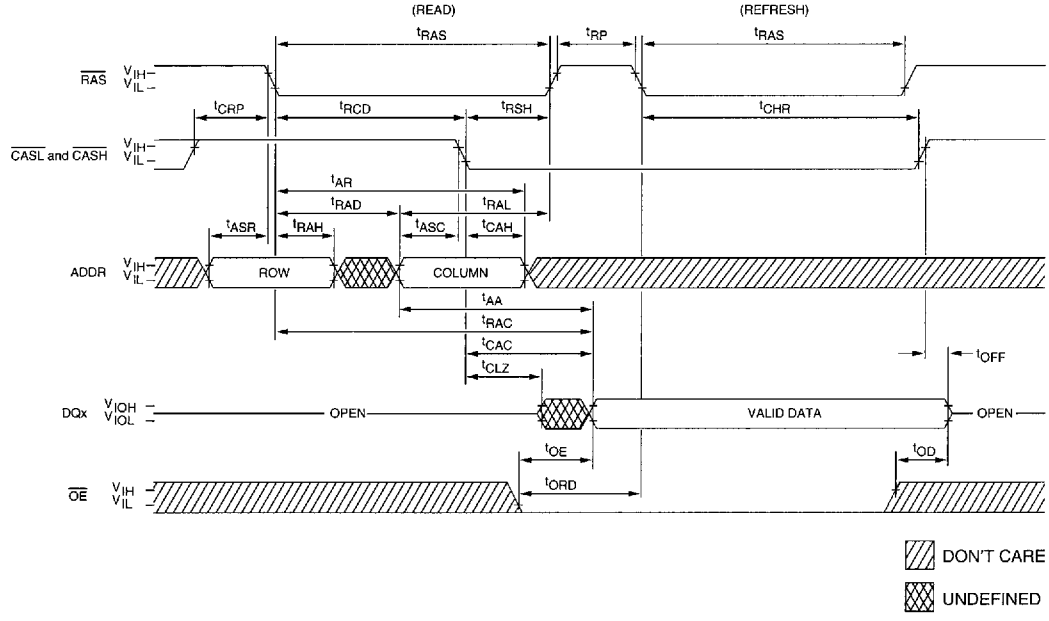



**NOTE:** 1. tWRP and tWRH are for system design reference only. The WE signal is actually a "don't care" at RAS time during a CBR REFRESH. However, WE should be held HIGH at RAS time during a CBR REFRESH to ensure compatibility with other DRAMs which require WE HIGH at RAS time during a CBR REFRESH.

## SELF REFRESH CYCLE
(Addresses and $\overline{OE}$ = DON'T CARE)




## HIDDEN REFRESH CYCLE [24]
($\overline{WE}$ = HIGH; $\overline{OE}$ = LOW)




**NOTE:**
1. tWRP and tWRH are for system design reference only. The $\overline{WE}$ signal is actually a "don't care" at $\overline{RAS}$ time during a CBR REFRESH. However, $\overline{WE}$ should be held HIGH at $\overline{RAS}$ time during a CBR REFRESH to ensure compatibility with other DRAMs which require $\overline{WE}$ HIGH at $\overline{RAS}$ time during a CBR REFRESH.
2. Once tRASS (MIN) is met and $\overline{RAS}$ remains LOW, the DRAM will enter SELF REFRESH mode.
3. Once tRPS is satisfied, a compete burst of all rows should be executed.