5 Electrical Characteristics

5.1 Absolute Maximum Ratings Over Free-Air Temperature Range (Unless Otherwise Noted)†

Supply voltage range, V_{CC} (see Note 1) ..... −0.5 V to 6 V
Input voltage range, at any input, V_I ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) (see Note 2) ..... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) (see Note 3) ..... ±20 mA
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range, T_{stg} ..... −65°C to 150°C
Case temperature for 10 seconds, T_C ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to GND.
2. This applies to all inputs.
3. This applies to all outputs.

5.2 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
Input voltage, V_I		0		V_{CC}	V
High-level input voltage, V_{IH}		2		V_{CC}	V
Low-level input voltage, V_{IL}		0		0.8	V
Clock frequency	BCLK		25	33	MHz
	SCLK		49.152		
Operating free-air temperature, T_A		0		70	°C
Virtual junction temperature range, T_J		0		115	°C

5.3 Electrical Characteristics Over Recommended Ranges of Supply Voltage and Operating Free-Air Temperature (Unless Otherwise Noted)

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage		I_{OH} = −4 mA	V_{CC} − 0.8			V
V_{OL}	Low-level output voltage		I_{OL} = 4 mA			0.5	V
V_{IT+}	Positive-going input threshold voltage		Phy interface			0.7 V_{CC}	V
			All other inputs (see Note 4)			2	
V_{IT-}	Negative-going input threshold voltage		Phy interface	0.2 V_{CC}			V
			All other inputs (see Note 4)	0.8			
I_{IL}	Low-level input current		V_I = GND			−1	µA
I_{IH}	High-level input current		V_I = V_{CC}			1	µA
I_{OZ}	High-impedance-state output current		V_I = V_{CC} or GND (see Note 5)			±10	µA
I_{CC}	Supply current		No load on outputs, SCLK = 49.152 MHz BCLK = 25 MHz		150		mA
C_i	Input capacitance	Input terminals	V_{CC} = 5 V, TA = 25°C		5		pF
		Bidirectional terminals			13		
C_o	Output capacitance				8		pF

† All typical values are at V_{CC} = 5 V and T_A = 25°C.

NOTES: 4. This applies for all inputs except SCLK, BCLK, and $\overline{\text{RESET}}$.

5. All outputs are in the high-impedance state.

5.4 Host-Interface Timing Requirements Over Operating Free-Air Temperature Range

PARAMETER		MIN	MAX	UNIT
t_{c1}	Cycle time, BCLK (see Figure 6–1)	30		ns
$t_{w1(H)}$	Pulse duration, BCLK high (see Figure 6–1)	10		ns
$t_{w1(L)}$	Pulse duration, BCLK low (see Figure 6–1)	10		ns
t_{su1}	Setup time, DATA[0:31] before BCLK↑ (see Figure 6–2)	4		ns
t_{h1}	Hold time, DATA[0:31] after BCLK↑ (see Figure 6–2)	2		ns
t_{su2}	Setup time, ADDR[0:7] before BCLK↑ (see Figures 6–2 and 6–3)	12		ns
t_{h2}	Hold time, ADDR[0:7] after BCLK↑ (see Figures 6–2 and 6–3)	2		ns
t_{su3}	Setup time, $\overline{\text{CS}}$ before BCLK↑ (see Figures 6–2 and 6–3)	12		ns
t_{h3}	Hold time, $\overline{\text{CS}}$ after BCLK↑ (see Figures 6–2 and 6–3)	2		ns
t_{su4}	Setup time, $\overline{\text{WR}}$ before BCLK↑ (see Figures 6–2 and 6–3)	12		ns
t_{h4}	Hold time, $\overline{\text{WR}}$ after BCLK↑ (see Figures 6–2 and 6–3)	2		ns

5.5 Host-Interface Switching Characteristics Over Operating Free-Air Temperature Range, C_L = 45 pF (unless otherwise noted)

	PARAMETER	MIN	MAX	UNIT
t_{d1}	Delay time, BCLK↑ to $\overline{CA}$ (see Figure 6–2)	4	16	ns
t_{d2}	Delay time, BCLK↑ to $\overline{CA}$ (see Figure 6–2)	4	16	ns
t_{d3}	Delay time, BCLK↑ to DATA[0:31] valid (see Figure 6–3)	4	24	ns
t_{d4}	Delay time, BCLK↑ to DATA[0:31] invalid (see Figure 6–3)	4	24	ns

5.6 Phy-Interface Timing Requirements Over Operating Free-Air Temperature Range

	PARAMETER	MIN	MAX	UNIT
t_{c2}	Cycle time, SCLK (see Figure 6–4)	20.24	20.45	ns
$t_{w2(H)}$	Pulse duration, SCLK high (see Figure 6–4)	9		ns
$t_{w2(L)}$	Pulse duration, SCLK low (see Figure 6–4)	9		ns
t_{su5}	Setup time, DATA[0:7] before SCLK↑ (see Figure 6–6)	6		ns
t_{h5}	Hold time, DATA[0:7] after SCLK↑ (see Figure 6–6)	0		ns
t_{su6}	Setup time, CTL[0:1] before SCLK↑ (see Figure 6–6)	6		ns
t_{h6}	Hold time, CTL[0:1] after SCLK↑ (see Figure 6–6)	0		ns

5.7 Phy-Interface Switching Characteristics Over Operating Free-Air Temperature Range, C_L = 45 pF (unless otherwise noted)

	PARAMETER	MIN	MAX	UNIT
t_{d5}	Delay time, SCLK↑ to D[0:7] valid (see Figure 6–5)	3	14	ns
t_{d6}	Delay time, SCLK↑ to D[0:7] (see Figure 6–5)	3	14	ns
t_{d7}	Delay time, SCLK↑ to D[0:7] invalid (see Figure 6–5)	3	14	ns
t_{d8}	Delay time, SCLK↑ to CTL[0:1] valid (see Figure 6–5)	3	14	ns
t_{d9}	Delay time, SCLK↑ to CTL[0:1] (see Figure 6–5)	3	14	ns
t_{d10}	Delay time, SCLK↑ to CTL[0:1] invalid (see Figure 6–5)	3	14	ns
t_{d11}	Delay time, SCLK↑ to LREQ (see Figure 6–7)	3	14	ns

5.8 Miscellaneous Timing Requirements Over Operating Free-Air Temperature Range (see Figure 6–9)

	PARAMETER	MIN	MAX	UNIT
t_{c3}	Cycle time, CYCLEIN	124.99	125.01	µs
$t_{w3(H)}$	Pulse duration, CYCLEIN high	62		µs
$t_{w3(L)}$	Pulse duration, CYCLEIN low	62		µs

5.9 Miscellaneous Signal Switching Characteristics Over Operating Free-Air Temperature Range

	PARAMETER	MIN	MAX	UNIT
t_{d12}	Delay time, SCLK↑ to $\overline{INT}$ low (see Figure 6–8)	4	18	ns
t_{d13}	Delay time, SCLK↑ to $\overline{INT}$ high (see Figure 6–8)	4	18	ns
t_{d14}	Delay time, SCLK↑ to CYCLEOUT high (see Figure 6–10)	4	16	ns
t_{d15}	Delay time, SCLK↑ to CYCLEOUT low (see Figure 6–10)	4	16	ns