CDP68HC05P4B Electrical Specifications

Absolute Maximum Ratings

Supply Voltage, V_{DD} . . . . . -0.5V to +7V
Input Voltage, V_{IN} . . . . . V_{SS} - 0.3V to V_{DD} + 0.3V
Self-Check Mode (IRQ Pin Only), V_{IN} . . . V_{SS} - 0.3V to 2 x V_{DD} + 0.3V
Current Drain Per Pin Excluding V_{DD} and V_{SS}, I 40mA

Operating Conditions

Voltage Range . . . . . +1.8V to +6.0V
Temperature Range
CDP68HC05P4B . . . . . -40°C to 85°C
CDP68HCL05P4B . . . . . 0°C to 70°C
CDP68HSC05P4B . . . . . -40°C to 85°C
Input High Voltage . . . . . ($0.8 \times V_{DD}$) to V_{DD}

Thermal Information

Thermal Resistance (Typical, Note 1) θ_{JA} (°C/W)
28 Ld PDIP . . . . . 55°
20 Ld SOIC . . . . . 100°
28 Ld SOIC . . . . . 70°
Maximum Junction Temperature . . . . . 150°C
Maximum Storage Temperature Range (T_{STG}) . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

DC Electrical Specifications HC Product Type , V_{DD} = 5.0V

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CDP68HC05P4B V_{DD} = 5V ±10%, V_{SS} = 0V, T_A = -40°C to 85°C (Note 2)						
Output Voltage	V_{OL}	I_{LOAD} < 10µA	-	-	0.1	V
	V_{OH}		V_{DD} - 0.1	-	-	V
Output High Voltage PA0-7. PB5-7, PC2-7, PD5	V_{OH}	I_{LOAD} = -0.8mA	V_{DD} - 0.8	-	-	V
PC0-1	V_{OH}	I_{LOAD} = -5.0mA	V_{DD} - 0.8	-	-	V
Output Low Voltage PA0-7. PB5-7, PC2-7, PD5	V_{OL}	I_{LOAD} = 1.6mA	-	-	0.4	V
PC0-1	V_{OL}	I_{LOAD} = 15.0mA	-	-	0.4	V
Input High Voltage PA0-7, PB5-7, PC0-7, PD5, PD7/TCAP, $\overline{RESET}$, $\overline{IRQ}$, OSC1	V_{IH}		0.7•V_{DD}	-	V_{DD}	V
Input Low Voltage PA0-7, PB5-7, PC0-7, PD5, PD7/TCAP, $\overline{RESET}$, $\overline{IRQ}$, OSC1	V_{IL}		V_{SS}	-	0.2•V_{DD}	V
Data Retention Mode	V_{RM}	T_A = 0°C to 70°C	1.2	-	-	V
Supply Current RUN (Note 6)	I_{DD}	f_{OSC} = 4.2MHz External Square Wave	-	3.1	5	mA
WAIT (Notes 7, 9)	I_{DD}		-	1.1	3.5	mA
STOP (Note 8)	I_{DD}	T_A = 25°C	-	1.0	15	µA
STOP (Note 8)	I_{DD}	T_A = -40°C to 85°C	-	4.0	30	µA
STOP with Wake Up Timer Enabled	I_{DD}	T_A = 25°C	-	10	-	µA
Wake Up Timer RC Oscillator Frequency	f_{RCO}	T_A = 25°C	-	13	-	kHz
I/O Ports Hi-Z Leakage Current: PA0-7. PB5-7, PC0-7, PD5	I_{IL}		-	-	±10	µA
Input Current: $\overline{RESET}$, $\overline{IRQ}$, OSC1, TCAP/PD7	I_{IN}		-	-	±1	µA
Capacitance Ports (As Input or Output, Note 3) $\overline{RESET}$, $\overline{IRQ}$, OSC1	C_{OUT}		-	-	12	pF
	C_{IN}		-	-	8	pF

DC Electrical Specifications HC Product Type , V_{DD} = 5.0V (Continued)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Pullup Current (Note 10)	I_{IN}		5		250	µA
Input Hysteresis Voltage: PA0-7	V_{HYS}		-	0.5	-	V
Input Hysteresis Voltage: $\overline{RESET}$, $\overline{IRQ}$, OSC1, TCAP	V_{HYS}		0.1•V_{DD}	1.0	0.5•V_{DD}	V

Control Timing HC Product Type, V_{DD} = 5.0V

PARAMETER	SYMBOL	MIN	MAX	UNITS
CDP68HC05P4B V_{DD} = 5V ±10%, V_{SS} = 0V, T_A = -40°C to 85°C				
Frequency Of Operation				
Crystal Option	f_{OSC}	-	4.2	MHz
External Clock Option	f_{OSC}	DC	4.2	MHz
Internal Operating Frequency				
Crystal (f_{OSC} ÷ 2)	f_{OP}	-	2.1	MHz
External Clock (f_{OSC} ÷ 2)	f_{OP}	DC	2.1	MHz
Cycle Time (See Figure 15)	t_{CYC}	476	-	ns
Crystal Oscillator Start-up Time for AT-cut Crystal (See Figure 15)	t_{OXOV}	-	100	ms
Stop Recovery Start-up Time (AT-cut Crystal Oscillator) (See Figure 1)	t_{ILCH}	-	100	ms
$\overline{RESET}$ Pulse Width (See Figure 15)	t_{RL}	1.5	-	t_{CYC}
Timer				
Resolution (Note 12)	t_{RES}	4	-	t_{CYC}
Input Capture Pulse Width (See Figures 2, 23)	t_{TH}, t_{TL}	125	-	ns
Input Capture Pulse Period (See Figures 2, 23)	t_{TLTL}	(Note 13)	-	t_{CYC}
Interrupt Pulse Width Low (Edge-Triggered) (See Figure 16B)	t_{ILIH}	125	-	ns
Interrupt Pulse Period (See Figure 16B)	t_{ILIH}	(Note11)	-	t_{CYC}
OSC1 Pulse Width	t_{OH}, t_{OL}	90	-	ns

DC Electrical Specifications HC Product Type , V_{DD} = 3.3V

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CDP68HC05P4B V_{DD} = 3.3V ±10%, V_{SS} = 0V, T_A = -40°C to 85°C (Note 2)						
Output Voltage	V_{OL}	I_{LOAD} < 10µA	-	-	0.1	V
	V_{OH}		V_{DD} - 0.1	-	-	V
Output High Voltage						
PA0-7. PB5-7, PC2-7, PD5	V_{OH}	I_{LOAD} = -0.2mA	V_{DD} - 0.3	-	-	V
PC0-1	V_{OH}	I_{LOAD} = -1.5mA	V_{DD} - 0.3	-	-	V
Output Low Voltage						
PA0-7. PB5-7, PC2-7, PD5	V_{OL}	I_{LOAD} = 0.4mA	-	-	0.3	V
PC0-1	V_{OL}	I_{LOAD} = 6.0mA	-	-	0.3	V
Input High Voltage						
PA0-7, PB5-7, PC0-7, PD5, PD7/TCAP, $\overline{RESET}$, $\overline{IRQ}$, OSC1	V_{IH}		0.7•V_{DD}	-	V_{DD}	V

DC Electrical Specifications HC Product Type , V_{DD} = 3.3V (Continued)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Low Voltage PA0-7, PB5-7, PC0-7, PD5, PD7/TCAP, $\overline{RESET}$, $\overline{IRQ}$, OSC1	V_{IL}		V_{SS}	-	0.2•V_{DD}	V
Data Retention Mode	V_{RM}	T_A = 0°C to 70°C	1.2	-	-	V
Supply Current RUN (Note 6)	I_{DD}	f_{OSC} = 2.1MHz External Square Wave	-	0.8	2.5	mA
WAIT (Notes 7, 9)	I_{DD}		-	0.35	1.4	mA
STOP (Note 8)	I_{DD}	T_A = 25°C	-	0.5	10	µA
STOP (Note 8)	I_{DD}	T_A = -40°C to 85°C	-	2	20	µA
STOP with Wake Up Timer Enabled	I_{DD}	T_A = 25°C	-	10	-	µA
Wake Up Timer RC Oscillator Frequency	f_{RCO}	T_A = 25°C	-	13	-	kHz
I/O Ports Hi-Z Leakage Current: PA0-7. PB5-7, PC0-7, PD5	I_{IL}		-	-	±10	µA
Input Current: $\overline{RESET}$, $\overline{IRQ}$, OSC1, TCAP/PD7	I_{IN}		-	-	±1	µA
Capacitance Ports (As Input or Output, Note 3) $\overline{RESET}$, $\overline{IRQ}$, OSC1	C_{OUT}		-	-	12	pF
	C_{IN}		-	-	8	pF
Input Pullup Current (Note 10)	I_{IN}		5		100	µA
Input Hysteresis Voltage: PA0-7	V_{HYS}		-	0.5	-	V
Input Hysteresis Voltage: $\overline{RESET}$, $\overline{IRQ}$, OSC1, TCAP	V_{HYS}		0.1•V_{DD}	1.0	0.5•V_{DD}	V

Control Timing HC Product Type, V_{DD}= 3.3V

PARAMETER	SYMBOL	MIN	MAX	UNITS
CDP68HC05P4B V_{DD} = 3.3V ±10%, V_{SS} = 0V, T_A = -40°C to 85°C (Note 2)				
Frequency Of Operation Crystal Option	f_{OSC}	-	2.1	MHz
External Clock Option	f_{OSC}	DC	2.1	MHz
Internal Operating Frequency Crystal (f_{OSC} ÷ 2)	f_{OP}	-	1.05	MHz
External Clock (f_{OSC} ÷ 2)	f_{OP}	DC	1.05	MHz
Cycle Time (See Figure 15)	t_{CYC}	952	-	ns
Crystal Oscillator Start-up Time for AT-cut Crystal (See Figure 15)	t_{OXOV}	-	100	ms
Stop Recovery Start-up Time (AT-cut Crystal Oscillator) (See Figure 1)	t_{ILCH}	-	100	ms
$\overline{RESET}$ Pulse Width (See Figure 15)	t_{RL}	1.5	-	t_{CYC}
Timer Resolution (Note 12)	t_{RES}	4.0	-	t_{CYC}
Input Capture Pulse Width (See Figures 2, 23)	t_{TH}, t_{TL}	250	-	ns
Input Capture Pulse Period (See Figures 2, 23)	t_{TLTL}	(Note 13)	-	t_{CYC}
Interrupt Pulse Width Low (Edge-Triggered) (See Figure 16B)	t_{ILIH}	250	-	ns
Interrupt Pulse Period (See Figure 16B)	t_{ILIH}	(Note 11)	-	t_{CYC}
OSC1 Pulse Width	t_{OH}, t_{OL}	200	-	ns

CDP68HCL05P4B Electrical Specifications

DC Electrical Specifications HCL Product Type, V_{DD} = 5.0V

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CDP68HCL05P4B V_{DD} = 5V ±10%, V_{SS} = 0V, T_A = 0°C to 70°C (Note 2)						
Output Voltage	V_{OL}	I_{LOAD} < 10µA	-	-	0.1	V
	V_{OH}		V_{DD} - 0.1	-	-	V
Output High Voltage						
PA0-7. PB5-7, PC2-7, PD5	V_{OH}	I_{LOAD} = -0.8mA	V_{DD} - 0.8	-	-	V
PC0-1	V_{OH}	I_{LOAD} = -5.0mA	V_{DD} - 0.8	-	-	V
Output Low Voltage						
PA0-7. PB5-7, PC2-7, PD5	V_{OL}	I_{LOAD} = 1.6mA	-	-	0.4	V
PC0-1	V_{OL}	I_{LOAD} = 15.0mA	-	-	0.4	V
Input High Voltage PA0-7, PB5-7, PC0-7, PD5, PD7/TCAP, $\overline{RESET}$, $\overline{IRQ}$, OSC1	V_{IH}		0.7•V_{DD}	-	V_{DD}	V
Input Low Voltage PA0-7, PB5-7, PC0-7, PD5, PD7/TCAP, $\overline{RESET}$, $\overline{IRQ}$, OSC1	V_{IL}		V_{SS}	-	0.2•V_{DD}	V
Data Retention Mode	V_{RM}	T_A = 0°C to 70°C	1.2	-	-	V
Supply Current						
RUN (Note 6)	I_{DD}	f_{OSC} = 4.2MHz External Square Wave	-	3.0	4.25	mA
WAIT (Notes 7, 9)	I_{DD}		-	1.1	2.25	mA
STOP (Note 8)	I_{DD}	T_A = 25°C	-	0.5	15	µA
STOP (Note 8)	I_{DD}	T_A = 0°C to 70°C	-	2.0	25	µA
STOP with Wake Up Timer Enabled	I_{DD}	T_A = 25°C	-	10	-	µA
Wake Up Timer RC Oscillator Frequency	f_{RCO}	T_A = 25°C	-	13	-	kHz
I/O Ports Hi-Z Leakage Current: PA0-7. PB5-7, PC0-7, PD5	I_{IL}		-	-	±10	µA
Input Current: $\overline{RESET}$, $\overline{IRQ}$, OSC1, TCAP/PD7	I_{IN}		-	-	±1	µA
Capacitance Ports (As Input or Output, Note 3) $\overline{RESET}$, $\overline{IRQ}$, OSC1	C_{OUT}		-	-	12	pF
	C_{IN}		-	-	8	pF
Input Pullup Current (Note 10)	I_{IN}		5		250	µA
Input Hysteresis Voltage: PA0-7	V_{HYS}		-	0.5	-	V
Input Hysteresis Voltage: $\overline{RESET}$, $\overline{IRQ}$, OSC1, TCAP	V_{HYS}		0.1•V_{DD}	1.0	0.5•V_{DD}	V

Control Timing HCL Product Type, V_{DD} = 5.0V

PARAMETER	SYMBOL	MIN	MAX	UNITS
CDP68HCL05P4B V_{DD} = 5V 10%, V_{SS} = 0V, T_A = 0°C to 70°C				
Frequency Of Operation				
Crystal Option	f_{OSC}	-	4.2	MHz
External Clock Option	f_{OSC}	DC	4.2	MHz
Internal Operating Frequency				
Crystal (f_{OSC} ÷ 2)	f_{OP}	-	2.1	MHz

Control Timing HCL Product Type, V_{DD} = 5.0V (Continued)

PARAMETER	SYMBOL	MIN	MAX	UNITS
External Clock ($f_{OSC} \div 2$)	f_{OP}	DC	2.1	MHz
Cycle Time (See Figure 15)	t_{CYC}	476	-	ns
Crystal Oscillator Start-up Time for AT-cut Crystal (See Figure 15)	t_{OXOV}	-	100	ms
Stop Recovery Start-up Time (AT-cut Crystal Oscillator) (See Figure 1)	t_{ILCH}	-	100	ms
$\overline{RESET}$ Pulse Width (See Figure 15)	t_{RL}	1.5	-	t_{CYC}
Timer				
Resolution (Note 12)	t_{RES}	4	-	t_{CYC}
Input Capture Pulse Width (See Figures 2, 23)	t_{TH}, t_{TL}	125	-	ns
Input Capture Pulse Period (See Figures 2, 23)	t_{TLTL}	(Note 13)	-	t_{CYC}
Interrupt Pulse Width Low (Edge-Triggered) (See Figure 16B)	t_{ILIH}	125	-	ns
Interrupt Pulse Period (See Figure 16B)	t_{ILIH}	(Note 11)	-	t_{CYC}
OSC1 Pulse Width	t_{OH}, t_{OL}	90	-	ns

DC Electrical Specifications HCL Product Type, V_{DD} = 2.5V - 3.6V

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CDP68HCL05P4B V_{DD} = 2.5V - 3.6V ±10%, V_{SS} = 0V, T_A = 0°C to 70°C (Note 2)						
Output Voltage	V_{OL}	I_{LOAD} < 10µA	-	-	0.1	V
	V_{OH}		V_{DD} - 0.1	-	-	V
Output High Voltage						
PA0-7. PB5-7, PC2-7, PD5	V_{OH}	I_{LOAD} = -0.2mA	V_{DD} - 0.3	-	-	V
PC0-1	V_{OH}	I_{LOAD} = -1.5mA	V_{DD} - 0.3	-	-	V
Output Low Voltage						
PA0-7. PB5-7, PC2-7, PD5	V_{OL}	I_{LOAD} = 0.4mA	-	-	0.3	V
PC0-1	V_{OL}	I_{LOAD} = 6.0mA	-	-	0.3	V
Input High Voltage PA0-7, PB5-7, PC0-7, PD5, PD7/TCAP, $\overline{RESET}$, $\overline{IRQ}$, OSC1	V_{IH}		0.7•V_{DD}	-	V_{DD}	V
Input Low Voltage PA0-7, PB5-7, PC0-7, PD5, PD7/TCAP, $\overline{RESET}$, $\overline{IRQ}$, OSC1	V_{IL}		V_{SS}	-	0.2•V_{DD}	V
Data Retention Mode	V_{RM}	T_A = 0°C to 70°C	1.2	-	-	V
Supply Current						
RUN (Note 6)	I_{DD}	f_{OSC} = 2.0MHz External Square Wave	-	0.8	1.6	mA
WAIT (Notes 7, 9)	I_{DD}		-	0.35	1.0	mA
STOP (Note 8)	I_{DD}	T_A = 25°C	-	0.2	5.0	µA
STOP (Note 8)	I_{DD}	T_A = 0°C to 70°C	-	2.0	10	µA
STOP with Wake Up Timer Enabled	I_{DD}	T_A = 25°C	-	10	-	µA
Supply Current						
RUN (Note 6)	I_{DD}	f_{OSC} = 1.0MHz External Square Wave	-	400	800	µA
WAIT (Notes 7, 9)	I_{DD}		-	200	500	µA
STOP (Note 8)	I_{DD}	T_A = 25°C	-	0.6	5.0	µA

DC Electrical Specifications HCL Product Type, V_{DD} = 2.5V - 3.6V (Continued)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
STOP (Note 8)	I_{DD}	T_A = 0°C to 70°C	-	2.0	10	µA
STOP with Wake Up Timer Enabled	I_{DD}	T_A = 25°C	-	10	-	µA
Wake Up Timer RC Oscillator Frequency	f_{RCO}	T_A = 25°C	-	13	-	kHz
I/O Ports Hi-Z Leakage Current: PA0-7. PB5-7, PC0-7, PD5	I_{IL}		-	-	±10	µA
Input Current: $\overline{RESET}$, $\overline{IRQ}$, OSC1, TCAP/PD7	I_{IN}		-	-	±1	µA
Capacitance Ports (As Input or Output, Note 3) $\overline{RESET}$, $\overline{IRQ}$, OSC1	C_{OUT}		-	-	12	pF
	C_{IN}		-	-	8	pF
Input Pullup Current (Note 10)	I_{IN}		5		100	µA
Input Hysteresis Voltage: PA0-7	V_{HYS}		-	0.5	-	V
Input Hysteresis Voltage: $\overline{RESET}$, $\overline{IRQ}$, OSC1, TCAP	V_{HYS}		0.1•V_{DD}	1.0	0.5•V_{DD}	V

Control Timing HCL Product Type, V_{DD}= 2.4V - 3.6V

PARAMETER	SYMBOL	MIN	MAX	UNITS
CDP68HCL05P4B V_{DD} = 2.4V to 3.6V, V_{SS} = 0V, T_A = 0°C to 70°C (V_{DC} = 3.6)				
Frequency Of Operation				
Crystal Option	f_{OSC}	-	2.1	MHz
External Clock Option	f_{OSC}	DC	2.1	MHz
Internal Operating Frequency				
Crystal (f_{OSC} ÷ 2)	f_{OP}	-	1.05	MHz
External Clock (f_{OSC} ÷ 2)	f_{OP}	DC	1.05	MHz
Cycle Time (See Figure 15)	t_{CYC}	952	-	ns
Crystal Oscillator Start-up Time for AT-cut Crystal (See Figure 15)	t_{OXOV}	-	100	ms
Stop Recovery Start-up Time (AT-cut Crystal Oscillator) (See Figure 1)	t_{ILCH}	-	100	ms
$\overline{RESET}$ Pulse Width (See Figure 15)	t_{RL}	1.5	-	t_{CYC}
Timer				
Resolution (Note 12)	t_{RES}	4.0	-	t_{CYC}
Input Capture Pulse Width (See Figures 2, 23)	t_{TH}, t_{TL}	250	-	ns
Input Capture Pulse Period (See Figures 2, 23)	t_{TLTL}	(Note 11)	-	t_{CYC}
Interrupt Pulse Width Low (Edge-Triggered) (See Figure 16B)	t_{ILIH}	250	-	ns
Interrupt Pulse Period (See Figure 16B)	t_{ILIH}	(Note 13)	-	t_{CYC}
OSC1 Pulse Width	t_{OH}, t_{OL}	200	-	ns

DC Electrical Specifications HCL Product Type, V_{DD} = 1.8V - 2.4V

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CDP68HCL05P4B V_{DD} = 1.8V - 2.4V, V_{SS} = 0V, T_A = 0°C to 70°C, Unless Otherwise Specified						
Output Voltage	V_{OL}	I_{LOAD} < 10µA	-	-	0.1	V
	V_{OH}		V_{DD} - 0.1	-	-	V

DC Electrical Specifications HCL Product Type, V_{DD} = 1.8V - 2.4V (Continued)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage						
PA0-7. PB5-7, PC2-7, PD5	V_{OH}	I_{LOAD} = -0.1mA	V_{DD} - 0.3	-	-	V
PC0-1	V_{OH}	I_{LOAD} = -0.75mA	V_{DD} - 0.3	-	-	V
Output Low Voltage						
PA0-7. PB5-7, PC2-7, PD5	V_{OL}	I_{LOAD} = 0.2mA	-	-	0.3	V
PC0-1	V_{OL}	I_{LOAD} = 3.0mA	-	-	0.3	V
Input High Voltage PA0-7, PB5-7, PC0-7, PD5, PD7/TCAP, $\overline{RESET}$, $\overline{IRQ}$, OSC1	V_{IH}		0.7•V_{DD}	-	V_{DD}	V
Input Low Voltage PA0-7, PB5-7, PC0-7, PD5, PD7/TCAP, $\overline{RESET}$, $\overline{IRQ}$, OSC1	V_{IL}		V_{SS}	-	0.2•V_{DD}	V
Data Retention Mode	V_{RM}	T_A = 0°C to 70°C	1.2	-	-	V
Supply Current						
RUN (Note 6)	I_{DD}	f_{OSC} = 1.0MHz External Square Wave	-	300	600	µA
WAIT (Notes 7, 9)	I_{DD}		-	200	400	µA
STOP (Note 8)	I_{DD}	T_A = 25°C	-	0.1	2	µA
STOP (Note 8)	I_{DD}	T_A = 0°C to 70°C	-	2.0	5	µA
STOP with Wake Up Timer Enabled	I_{DD}	T_A = 25°C	-	10	-	µA
Wake Up Timer RC Oscillator Frequency	f_{RCO}	T_A = 25°C	-	13	-	kHz
I/O Ports Hi-Z Leakage Current: PA0-7. PB5-7, PC0-7, PD5	I_{IL}		-	-	±10	µA
Input Current: $\overline{RESET}$, $\overline{IRQ}$, OSC1, TCAP/PD7	I_{IN}		-	-	±1	µA
Capacitance Ports (As Input or Output, Note 3) $\overline{RESET}$, $\overline{IRQ}$, OSC1	C_{OUT}		-	-	12	pF
	C_{IN}		-	-	8	pF
Input Pullup Current (Note 10)	I_{IN}		5		50	µA
Input Hysteresis Voltage: PA0-7	V_{HYS}		-	0.5	-	V
Input Hysteresis Voltage: $\overline{RESET}$, $\overline{IRQ}$, OSC1, TCAP	V_{HYS}		0.1•V_{DD}	1.0	0.5•V_{DD}	V

Control Timing HCL Product Type, V_{DD} = 1.8V - 2.4V

PARAMETER	SYMBOL	MIN	MAX	UNITS
CDP68HCL05P4B V_{DD} = 1.8V to 2.4V, V_{SS} = 0V, T_A = 0°C to 70°C (V_{DC} = 2.4)				
Frequency Of Operation				
Crystal Option	f_{OSC}	-	1.0	MHz
External Clock Option	f_{OSC}	DC	1.0	MHz
Internal Operating Frequency				
Crystal (f_{OSC} ÷ 2)	f_{OP}	-	0.5	MHz
External Clock (f_{OSC} ÷ 2)	f_{OP}	DC	0.5	MHz
Cycle Time (See Figure 15)	t_{CYC}	2000	-	ns
Crystal Oscillator Start-up Time for AT-cut Crystal (See Figure 15)	t_{OXOV}	-	100	ms

Control Timing HCL Product Type, V_{DD} = 1.8V - 2.4V (Continued)

PARAMETER	SYMBOL	MIN	MAX	UNITS
Stop Recovery Start-up Time (AT-cut Crystal Oscillator) (See Figure 1)	t_{ILCH}	-	100	ms
$\overline{\text{RESET}}$ Pulse Width (See Figure 15)	t_{RL}	1.5	-	t_{CYC}
Timer				
Resolution (Note 12)	t_{RES}	4.0	-	t_{CYC}
Input Capture Pulse Width (See Figures 2, 23)	t_{TH}, t_{TL}	500	-	ns
Input Capture Pulse Period (See Figures 2, 23)	t_{TLTL}	(Note 13)	-	t_{CYC}
Interrupt Pulse Width Low (Edge-Triggered) (See Figure 16B)	t_{ILIH}	500	-	ns
Interrupt Pulse Period (See Figure 16B)	t_{ILIH}	(Note 11)	-	t_{CYC}
OSC1 Pulse Width	t_{OH}, t_{OL}	400	-	ns

CDP68HSC05P4B Electrical Specifications

DC Electrical Specifications HSC Product Type , V_{DD} = 5.0V

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CDP68HSC05P4B V_{DD} = 5V ±10%, V_{SS} = 0V, T_A = -40°C to 85°C (Note 2)						
Output Voltage	V_{OL}	I_{LOAD} < 10µA	-	-	0.1	V
	V_{OH}		V_{DD} - 0.1	-	-	V
Output High Voltage						
PA0-7. PB5-7, PC2-7, PD5	V_{OH}	I_{LOAD} = -0.8mA	V_{DD} - 0.8	-	-	V
PC0-1	V_{OH}	I_{LOAD} = -5.0mA	V_{DD} - 0.8	-	-	V
Output Low Voltage						
PA0-7. PB5-7, PC2-7, PD5	V_{OL}	I_{LOAD} = 1.6mA	-	-	0.4	V
PC0-1	V_{OL}	I_{LOAD} = 15.0mA	-	-	0.4	V
Input High Voltage PA0-7, PB5-7, PC0-7, PD5, PD7/TCAP, $\overline{RESET}$, $\overline{IRQ}$, OSC1	V_{IH}		0.7•V_{DD}	-	V_{DD}	V
Input Low Voltage PA0-7, PB5-7, PC0-7, PD5, PD7/TCAP, $\overline{RESET}$, $\overline{IRQ}$, OSC1	V_{IL}		V_{SS}	-	0.2•V_{DD}	V
Data Retention Mode	V_{RM}	T_A = 0°C to 70°C	1.2	-	-	V
Supply Current						
RUN (Note 6)	I_{DD}	f_{OSC} = 8.0MHz External Square Wave	-	6.0	7.0	mA
WAIT (Notes 7, 9)	I_{DD}		-	2.0	3.5	mA
STOP (Note 8)	I_{DD}	T_A = 25°C	-	1.0	15	µA
STOP (Note 8)	I_{DD}	T_A = -40°C to 85°C	-	4.0	30	µA
STOP with Wake Up Timer Enabled	I_{DD}	T_A = 25°C	-	10	-	µA
Wake Up Timer RC Oscillator Frequency	f_{RCO}	T_A = 25°C	-	13	-	kHz
I/O Ports Hi-Z Leakage Current: PA0-7. PB5-7, PC0-7, PD5	I_{IL}		-	-	±10	µA
Input Current: $\overline{RESET}$, $\overline{IRQ}$, OSC1, TCAP/PD7	I_{IN}		-	-	±1	µA
Capacitance Ports (As Input or Output, Note 3) $\overline{RESET}$, $\overline{IRQ}$, OSC1	C_{OUT}		-	-	12	pF
	C_{IN}		-	-	8	pF
Input Pullup Current (Note 10)	I_{IN}		5		250	µA
Input Hysteresis Voltage: PA0-7	V_{HYS}		-	0.5	-	V
Input Hysteresis Voltage: $\overline{RESET}$, $\overline{IRQ}$, OSC1, TCAP	V_{HYS}		0.1•V_{DD}	1.0	0.5•V_{DD}	V

Control Timing HSC Product Type, V_{DD} = 5.0V

PARAMETER	SYMBOL	MIN	MAX	UNITS
CDP68HSC05P4B V_{DD} = 5V ±10%, V_{SS} = 0V, T_A = -40°C to 85°C (Note 2)				
Frequency Of Operation Crystal Option	f_{OSC}	-	8.0	MHz
External Clock Option	f_{OSC}	DC	8.0	MHz
Internal Operating Frequency Crystal (f_{OSC} ÷ 2)	f_{OP}	-	4.0	MHz

Control Timing HSC Product Type, V_{DD} = 5.0V (Continued)

PARAMETER	SYMBOL	MIN	MAX	UNITS
External Clock ($f_{OSC} \div 2$)	f_{OP}	DC	4.0	MHz
Cycle Time (See Figure 15)	t_{CYC}	250	-	ns
Crystal Oscillator Start-up Time for AT-cut Crystal (See Figure 15)	t_{OXOV}	-	100	ms
Stop Recovery Start-up Time (AT-cut Crystal Oscillator) (See Figure 1)	t_{ILCH}	-	100	ms
$\overline{RESET}$ Pulse Width (See Figure 15)	t_{RL}	1.5	-	t_{CYC}
Timer				
Resolution (Note 12)	t_{RES}	4	-	t_{CYC}
Input Capture Pulse Width (See Figures 2, 23)	t_{TH}, t_{TL}	63	-	ns
Input Capture Pulse Period (See Figures 2, 23)	t_{TLTL}	(Note 13)	-	t_{CYC}
Interrupt Pulse Width Low (Edge-Triggered) (See Figure 16B)	t_{ILIH}	63	-	ns
Interrupt Pulse Period (See Figure 16B)	t_{ILIH}	(Note 11)	-	t_{CYC}
OSC1 Pulse Width	t_{OH}, t_{OL}	45	-	ns

DC Electrical Specifications HSC Product Type, V_{DD} = 2.6V - 3.6V

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CDP68HSC05P4B V_{DD} = 2.4V - 3.6V, V_{SS} = 0V, T_A = -40°C to 85°C (Note 2)						
Output Voltage	V_{OL}	$I_{LOAD} \leq 10\mu A$	-	-	0.1	V
	V_{OH}		V_{DD} - 0.1	-	-	V
Output High Voltage						
PA0-7. PB5-7, PC2-7, PD5	V_{OH}	I_{LOAD} = -0.2mA	V_{DD} - 0.8	-	-	V
PC0-1	V_{OH}	I_{LOAD} = -5.0mA	V_{DD} - 0.8	-	-	V
Output Low Voltage						
PA0-7. PB5-7, PC2-7, PD5	V_{OL}	I_{LOAD} = 0.4mA	-	-	0.3	V
PC0-1	V_{OL}	I_{LOAD} = 6.0mA	-	-	0.3	V
Input High Voltage PA0-7, PB5-7, PC0-7, PD5, PD7/TCAP, $\overline{RESET}$, $\overline{IRQ}$, OSC1	V_{IH}		0.7•V_{DD}	-	V_{DD}	V
Input Low Voltage PA0-7, PC0-7, $\overline{RESET}$, $\overline{IRQ}$, OSC1	V_{IH}		V_{SS}	-	0.2•V_{DD}	V
Data Retention Mode	V_{RM}	T_A = 0°C to 70°C	1.2	-	-	V
Supply Current						
RUN (Note 6)	I_{DD}	f_{OSC} = 4.2MHz External Square Wave	-	1.8	3.5	mA
WAIT (Notes 7, 9)	I_{DD}		-	0.8	2.5	mA
STOP (Note 8)	I_{DD}	T_A = 25°C	-	0.6	15	µA
STOP (Note 8)	I_{DD}	T_A = -40°C to 85°C	-	2.0	20	µA
STOP with Wake Up Timer Enabled	I_{DD}	T_A = 25°C	-	10	-	µA
Wake Up Timer RC Oscillator Frequency	f_{RCO}	T_A = 25°C	-	13	-	kHz
I/O Ports Hi-Z Leakage Current: PA0-7, PC0-7	I_{IL}		-10	-	+10	µA
Input Hysteresis Voltage: PA0-7	V_{HYS}		-	0.5	-	V
Input Pullup Current (Note 10)	I_{IN}		5		100	µA

CDP68HSC05P4B Electrical Specifications

DC Electrical Specifications HSC Product Type, V_{DD} = 2.6V - 3.6V

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Hysteresis Voltage: $\overline{RESET}$, $\overline{IRQ}$, OSC1, TCAP	V_{HYS}		0.1•V_{DD}	1.0	0.5•V_{DD}	V
Input Current: $\overline{RESET}$, $\overline{IRQ}$, OSC1, TCAP	I_{IN}		-1	-	+1	µA
Capacitance Ports (As Input or Output) $\overline{RESET}$, $\overline{IRQ}$, TCAP, OSC1	C_{OUT}		-	-	12	pF
	C_{IN}		-	-	8	pF

Control Timing HSC Product Type, V_{DD} = 2.4V - 3.6V

PARAMETER	SYMBOL	MIN	MAX	UNITS
CDP68HSC05P4B V_{DD} = 2.4V - 3.6V, V_{SS} = 0V, T_A = -40°C to 85°C (Note 2)				
Frequency Of Operation				
Crystal Option	f_{OSC}	-	4.2	MHz
External Clock Option	f_{OSC}	DC	4.2	MHz
Internal Operating Frequency				
Crystal (f_{OSC} ÷ 2)	f_{OP}	-	2.1	MHz
External Clock (f_{OSC} ÷ 2)	f_{OP}	DC	2.1	MHz
Cycle Time (See Figure 15)	t_{CYC}	476	-	ns
Crystal Oscillator Start-up Time for AT-cut Crystal (See Figure 15)	t_{OXOV}	-	100	ms
Stop Recovery Start-up Time (AT-cut Crystal Oscillator) (See Figure 1)	t_{ILCH}	-	100	ms
$\overline{RESET}$ Pulse Width (See Figure 15)	t_{RL}	1.5	-	t_{CYC}
Timer				
Resolution (Note 12)	t_{RES}	4.0	-	t_{CYC}
Input Capture Pulse Width (See Figures 2, 23)	t_{TH}, t_{TL}	125	-	ns
Input Capture Pulse Period (See Figures 2, 23)	t_{TLTL}	(Note 13)	-	t_{CYC}
Interrupt Pulse Width Low (Edge-Triggered) (See Figure 16B)	t_{ILIH}	125	-	ns
Interrupt Pulse Period (See Figure 16B)	t_{ILIH}	(Note 11)	-	t_{CYC}
OSC1 Pulse Width	t_{OH}, t_{OL}	90	-	ns

NOTES:

2. This device contains circuitry to protect the inputs against damage due to high static voltages of electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{IN} and V_{OUT} be constrained to the range $V_{SS} < (V_{IN}$ or $V_{OUT}) < V_{DD}$. Reliability of operation is enhanced if unused inputs except OSC2 are connected to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).
3. Includes ports used as input/output pins; Ports used as input only pins, Ports used as output only pins.
4. All values shown reflect average measurement.
5. Typical values at midpoint of voltage range, 25°C only.
6. Run (Operating) I_{DD}, Wait I_{DD}: Measured using external square-wave clock source, all inputs 0.2V from rail, no DC loads, less than 50pF on all outputs, C_L = 20pF on OSC2.
7. Wait, Stop I_{DD}: All ports configured as inputs, V_{IL} = 0.2V, V_{IH} = V_{DD} - 0.2V.
8. Stop I_{DD} measured with OSC1 = V_{SS}.
9. Wait I_{DD} is affected linearly by the OSC2 capacitance.
10. Input pullup current measured with V_{IL} = 0.2V.
11. The minimum period t_{ILIH} should not be less than the number of cycle times it takes to execute the interrupt service routine plus 21 t_{CYC}.
12. Since a 2-bit prescaler in the timer must count four internal cycles (t_{CYC}), this is the limiting minimum factor in determining the timer resolution.
13. The minimum period t_{TLTL} should not be less than the number of cycle times it takes to execute the capture interrupt service routine plus 24 t_{CYC}.

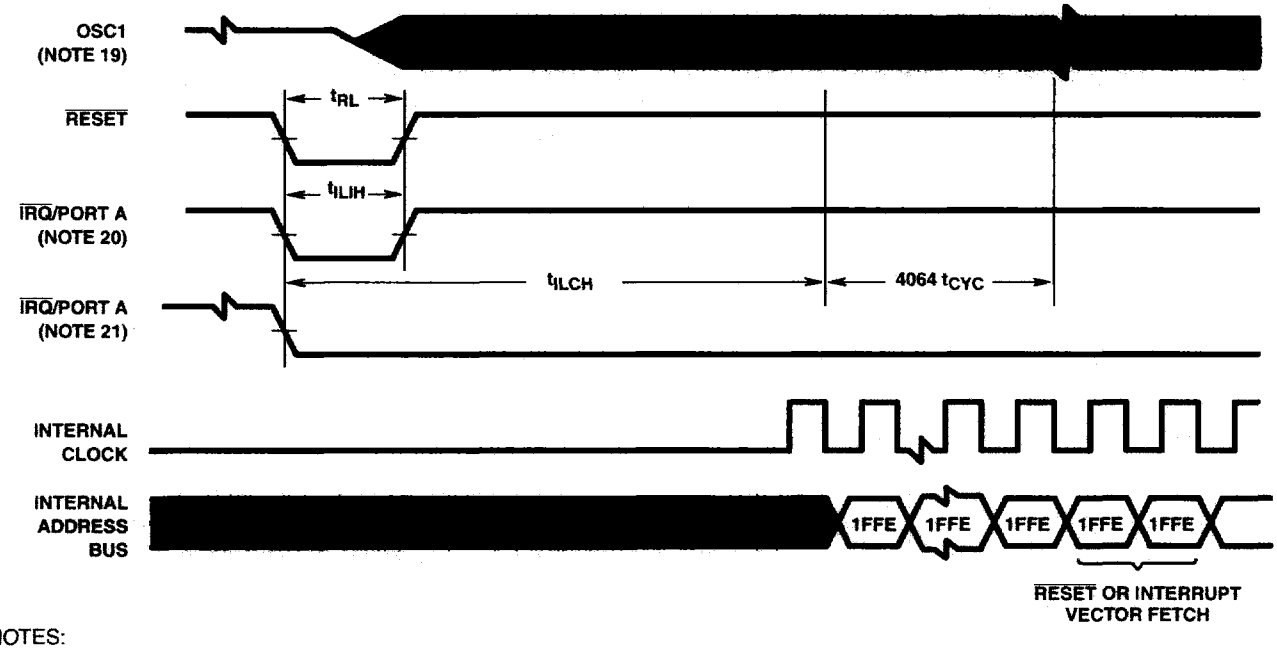
SIOP Timing

PARAMETER	SYMBOL	MIN	MAX	UNITS
CDP68HC05P4B, CDP68HCL05P4B V_{DD} = 5V ±10%, V_{SS} = 0V, T_A = 0°C to 85°C, Unless Otherwise Specified				
Frequency Of Operation				
Master	$f_{SIOP(M)}$	0.25	0.25	f_{OP}
Slave	$f_{SIOP(S)}$	DC	0.25	f_{OP}
Cycle Time				
Master	$t_{SCK(M)}$	4.0	4.0	t_{CYC}
Slave	$t_{SCK(S)}$	-	4.0	t_{CYC}
Clock (SCK) low time (f_{OP} = 2.1MHz)	t_{SCKL}	932	-	ns
SDO Data Valid Time	t_v	-	200	ns
SDO Hold Time	t_{ho}	0	-	ns
SDI Setup Time	t_s	100	-	ns
SDI Hold Time	t_h	100	-	ns
CDP68HSC05P4B V_{DD} = 5V ±10%, V_{SS} = 0V, T_A = -40°C to 85°C, Unless Otherwise Specified				
Frequency Of Operation				
Master	$f_{SIOP(M)}$	0.25	0.25	f_{OP}
Slave	$f_{SIOP(S)}$	DC	0.25	f_{OP}
Cycle Time				
Master	$t_{SCK(M)}$	4.0	4.0	t_{CYC}
Slave	$t_{SCK(S)}$	-	4.0	t_{CYC}
Clock (SCK) low time (f_{OP} = 2.1MHz)	t_{SCKL}	466	-	ns
SDO Data Valid Time	t_v	-	100	ns
SDO Hold Time	t_{ho}	0	-	ns
SDI Setup Time	t_s	50	-	ns
SDI Hold Time	t_h	50	-	ns

NOTES:

14. The minimum period t_{ILIH} should not be less than the number of cycle times it takes to execute the interrupt service routine plus 21 t_{CYC}.
15. Since a 2-bit prescaler in the timer must count four internal cycles (t_{CYC}), this is the limiting minimum factor in determining the timer resolution.
16. The minimum period t_{TLTL} should not be less than the number of cycle times it takes to execute the capture interrupt service routine plus 24 t_{CYC}.
17. For the SIOP, $f_{OP} = f_{OSC}/2$ = 2.1MHz maximum for HC and HCL parts; 4.2MHz maximum for HSC parts; $t_{CYC} = 1/f_{OP}$.
18. In master mode, SCK is generated by dividing the internal clock (f_{OP}) by 4.

Control Timing Diagrams



NOTES:

19. Represents the internal gating of the OSC1 pin.
20. IRQ/PORT A pin edge-sensitive mask option.
21. IRQ/PORT A pin level and edge-sensitive mask option.

FIGURE 1. STOP RECOVERY TIMING DIAGRAM

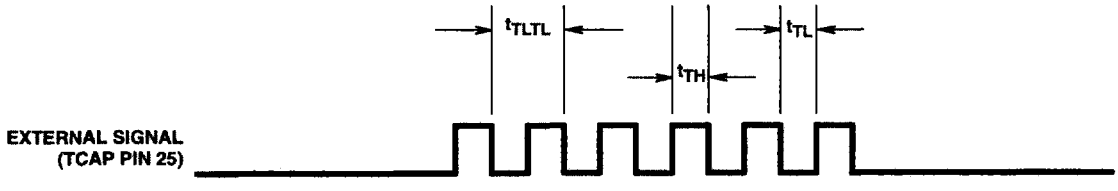
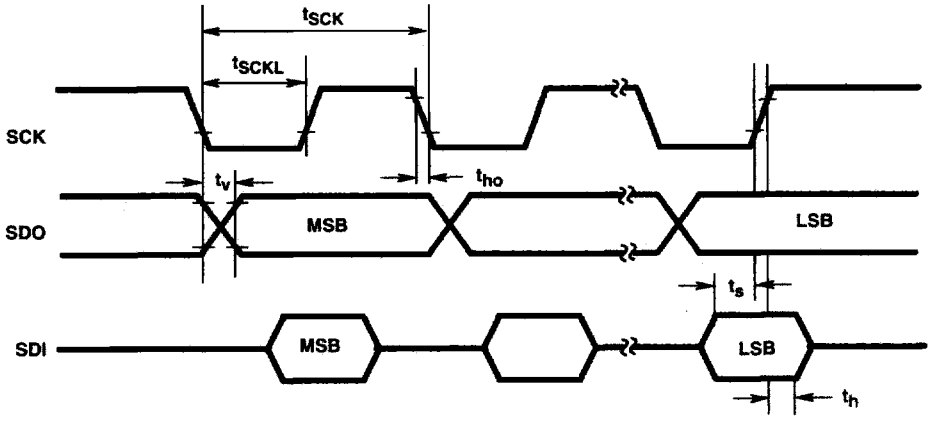


FIGURE 2. TIMER RELATIONSHIPS



This diagram applies to both master and slave SIOP modes.
Bit order shown for MSB first mask option.

FIGURE 3. SIOP TIMING