Preliminary

T-46-13-27

Am28F512

65,536 x 8-Bit CMOS Flash Memory

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **High performance**
  - 90 ns maximum access time
- **Low power consumption**
  - 30 mA maximum active current
  - 100 µA maximum standby current
- **Compatible with JEDEC-standard byte-wide pinouts**
  - 32-pin DIP
  - 32-pin PLCC
- **10,000 erase/program cycles**
- **Program and erase voltage 12.0 V ±5%**
- **Latch-up protected to 100 mA from –1 V to Vcc +1 V**
- **Flasherase™ Electrical Bulk Chip-Erase**
  - One second typical chip-erase
- **Flashrite™ Programming**
  - 10 µs typical byte-program
  - Less than 1 second typical chip program
- **Command register architecture for microprocessor/microcontroller compatible write interface**
- **On-chip address and data latches**
- **Advanced CMOS flash memory technology**
  - Low cost single transistor memory cell

GENERAL DESCRIPTION

The Am28F512 is a 512K "Flash" electrically erasable, electrically programmable read only memory organized as 64K bytes of 8 bits each. The Am28F512 is packaged in 32-pin PDIP and PLCC versions which allow for upgrades to the 2 Megabit density. The device is also offered in ceramic DIP and LCC packages. It is designed to be reprogrammed and erased in-system or in standard EPROM programmers.

The standard Am28F512 offers access times as fast as 90 ns, allowing operation of high-speed microprocessors without wait states. To eliminate bus contention, the Am28F512 has separate chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) controls.

AMD's Flash memories augment EPROM functionality with in-circuit electrical erasure and programming. The Am28F512 uses a command register to manage this functionality, while maintaining a standard 32-pin pinout. The command register allows for 100% TTL level control inputs and fixed power supply levels during erase and programming, while maintaining maximum EPROM compatibility.

AMD's Flash technology reliably stores memory contents even after 10,000 erase and program cycles. The AMD cell is designed to optimize the erase and programming mechanisms. In addition, the combination of advanced tunnel oxide processing and low internal electric fields for erase and programming operations produces reliable cycling. The Am28F512 uses a 12.0 V ±5% V_{PP} supply to perform the Flasherase and Flashrite algorithms.

The highest degree of latch-up protection is achieved with AMD's proprietary non-epi process. Latch-up protection is provided for stresses up to 100 milliamps on address and data pins from –1 V to Vcc+1 V.

The Am28F512 is byte programmable using 10 µs programming pulses in accordance with AMD's Flashrite programming algorithm. The typical room temperature programming time of the Am28F512 is less than one second. The entire chip is bulk erased using 10ms erase pulses according to AMD's Flasherase algorithm. Typical erasure at room temperature is accomplished in less than one second. The windowed package and the 15–20 minutes required for EPROM erasure using ultraviolet light are eliminated.

Commands are written to the command register using standard microprocessor write timings. Register contents serve as inputs to an internal state-machine which controls the erase and programming circuitry. During write cycles, the command register internally latches address and data needed for the programming and erase operations. For system design simplification, the Am28F512 is designed to support either $\overline{WE}$ or $\overline{CE}$ controlled writes. During a system write cycle, addresses are latched on the falling edge of $\overline{WE}$ or $\overline{CE}$ whichever occurs last. Data is latched on the rising edge of $\overline{WE}$ or $\overline{CE}$ whichever occurs first. To simplify the following discussion, the $\overline{WE}$ pin is used as the write cycle control pin throughout the rest of this text. All setup and hold times are with respect to the $\overline{WE}$ signal.

AMD's Flash technology combines years of EPROM and E²PROM experience to produce the highest levels of quality, reliability, and cost effectiveness. The Am28F512 electrically erases all bits simultaneously using Fowler-Nordheim tunneling. The bytes are programmed one byte at a time using the EPROM programming mechanism of hot electron injection.

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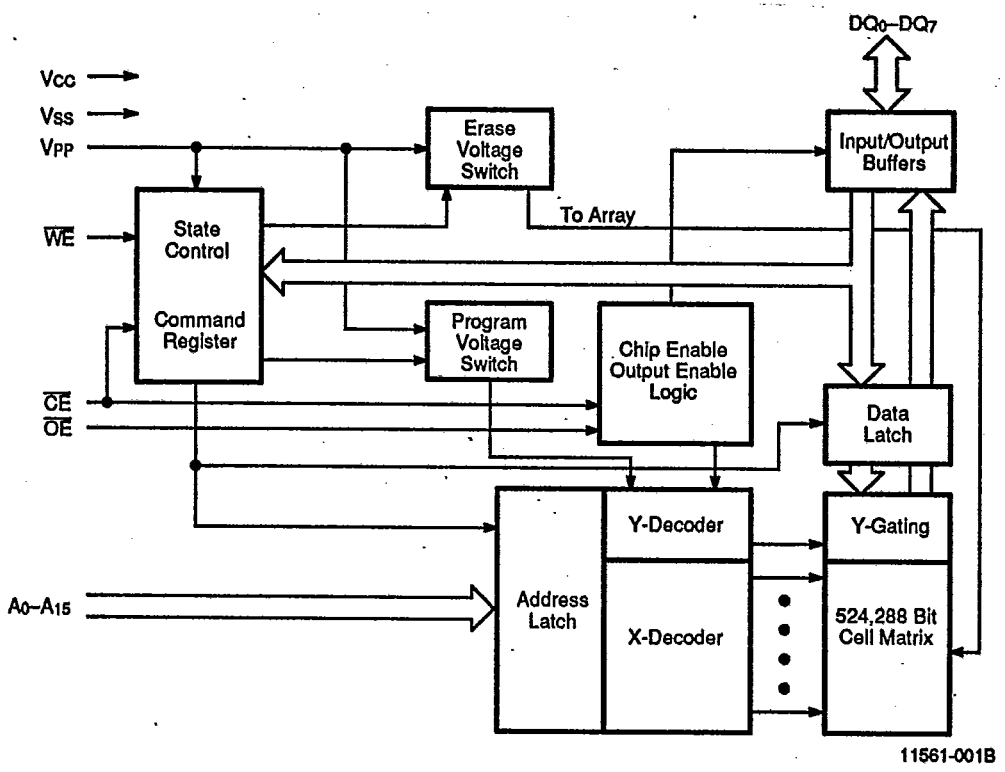
BLOCK DIAGRAM

T-46-13-27



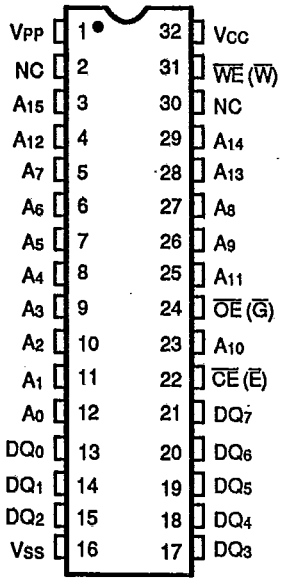
11561-001B

PRODUCT SELECTOR GUIDE

Family Part No.	Am28F512			
Ordering part No:				
±10% Vcc Tolerance	-90	-120	-150	-200
±5% Vcc Tolerance	-95	—	—	—
Max Access Time (ns)	90	120	150	200
$\overline{CE}$ ($\overline{E}$) Access (ns)	90	120	150	200
$\overline{OE}$ ($\overline{G}$) Access (ns)	35	50	75	75

CONNECTION DIAGRAMS

DIP



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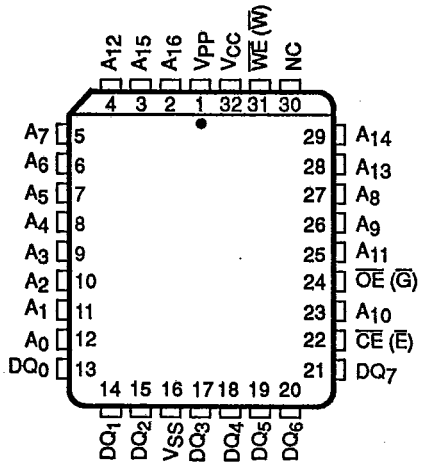
PLCC*

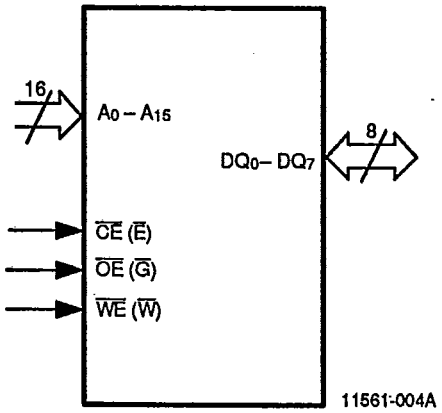


11561-003B

Note: Pin 1 is marked for orientation.

* Also available in LCC.

LOGIC SYMBOL



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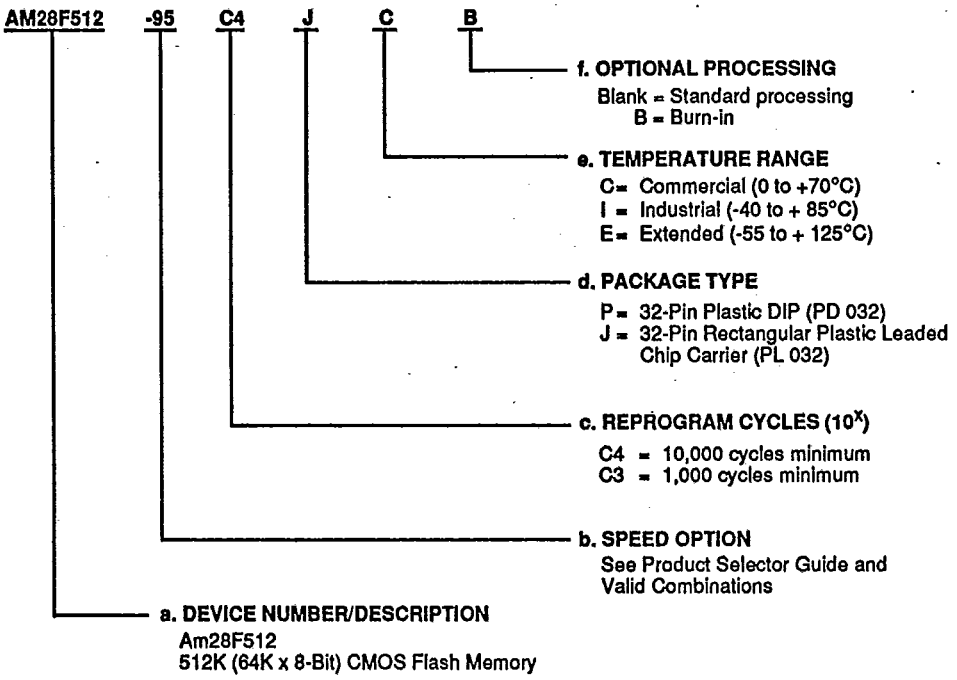
ORDERING INFORMATION
Standard Products

T-46-13-27

AMD standard products are available in several packages and operating ranges. The ordering number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option
c. Reprogram Cycles
d. Package Type
e. Temperature Range
f. Optional Processing



Valid Combinations	
AM28F512-95 AM28F512-90	C4PCB, C4JCB, C4PC, C4JC, C3PC, C3JC, C3PCB, C3JCB
AM28F512-120 AM28F512-150 AM28F512-200	C4PC, C4PI, C4JC, C4PCB, C4PIB, C4JCB, C4JIB, C4PE, C4PEB, C4JE, C4JEB, C4JI, C3PC, C3PI, C3PCB, C3PIB, C3JCB, C3JIB, C3PE, C3PEB, C3JE, C3JEB, C3JC, C3JI

Valid Combinations

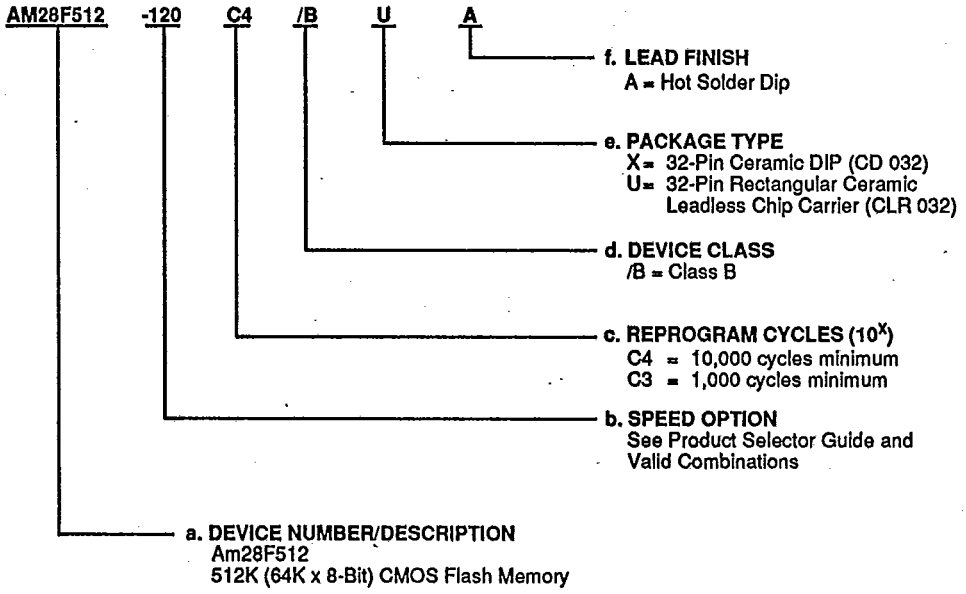
Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

ORDERING INFORMATION
T-46-13-27

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option
c. Reprogram cycles
d. Device Class
e. Package Type
f. Lead Finish



Valid Combinations	
AM28F512-120 AM28F512-150 AM28F512-200	C4/BXA, C4/BUA C3/BXA, C3/BUA

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

PIN DESCRIPTION

$A_0 - A_{15}$

Address Inputs for memory locations. Internal latches hold addresses during write cycles.

$DQ_0 - DQ_7$

Data Inputs during memory write cycles. Internal latches hold data during write cycles. Data Outputs during memory read cycles.

$\overline{CE}$ ($\overline{E}$)

The Chip Enable active low Input activates the chip'scontrol logic and input buffers. Chip Enable high will deselect the device and operates the chip in standby mode.

$\overline{OE}$ ($\overline{G}$)

The Output Enable active low input gates the outputs of the device through the data buffers during memory read cycles.

$\overline{WE}$ ($\overline{W}$)

The Write Enable active low input controls the write function of the command register to the memory array. The target address is latched on the falling edge of the Write Enable pulse and the appropriate data is latched on the rising edge of the pulse.

T-46-13-27

V_{PP}

Power supply for erase and programming. V_{PP} must be at high voltage in order to write to the command register. The command register controls all functions required to alter the memory array contents. Memory contents cannot be altered when $V_{PP} \leq V_{CC} + 2V$.

V_{CC}

Power supply for device operation. (5.0V ± 5% or 10%)

V_{SS}

Ground

NC

No Connect-corresponding pin is not connected internally to the die.

BASIC PRINCIPLES

The Am28F512 uses 100% TTL-level control inputs to manage the command register. Erase and reprogramming operations use a fixed 12.0V ± 5% power supply.

Read Only Memory

Without high V_{PP} voltage, the Am28F512 functions as a read only memory and operates like a standard EPROM. The control inputs still manage traditional read, standby, output disable, and Auto select modes.

Command Register

The command register is enabled only when high voltage is applied to the V_{PP} pin. The erase and reprogramming operations are only accessed via the register. In addition, two-cycle commands are required for erase and reprogramming operations. The traditional read, standby, output disable, and Auto select modes are available via the register.

The Am28F512's command register is written using standard microprocessor write timings. The register controls an internal state machine that manages all device operations. For system design simplification, the Am28F512 is designed to support either $\overline{WE}$ or $\overline{CE}$ controlled writes. During a system write cycle, addresses are latched on the falling edge of $\overline{WE}$ or $\overline{CE}$ whichever occurs last. Data is latched on the rising edge of $\overline{WE}$ or $\overline{CE}$ whichever occur first. To simplify the following discussion, the $\overline{WE}$ pin is used as the write cycle control pin throughout the rest of this text. All setup and hold times are with respect to the $\overline{WE}$ signal.

Overview of Erase/Program Operations

Erase Sequence

A multiple step command sequence is required to erase the Flash device (a two-cycle Erase command and repeated one cycle verify commands).

Note:
The Flash memory array must be completely programmed prior to erasure. Refer to the Flasherase Algorithm.

1. **Set-up Erase:** Write the Set-up Erase command to the command register.
2. **Erase:** Write the Erase command (same as Set-up Erase command) to the command register again. The second command initiates the erase operation. The system software routines must now time-out the erase pulse width (10 ms) prior to issuing the Erase-verify command.
3. **Erase-verify:** Write the Erase-verify command to the command register. This command terminates the erase operation. After the erase operation, each byte of the array must be verified. Address information must be supplied with the Erase-verify command. This command verifies the margin and outputs the addressed byte in order to compare the array data with FFH data (Byte erased). After successful data verification the Erase-verify command is written again with new address information. Each byte of the array is sequentially verified in this manner.

If data of the addressed location is not verified, the Erase sequence is repeated until the entire array is successfully verified or the sequence is repeated 1000 times.

Programming Sequence

A three step command sequence (a two-cycle Program command and one cycle Verify command) is required to program a byte of the Flash array. Refer to the Flashrite Algorithm.

1. **Set-up Program:** Write the Set-up Program command to the command register.
2. **Program:** Write the Program command to the command register with the appropriate Address and Data. The system software routines must now time-out the program pulse width (10 µs) prior to issuing the Program-verify command.
3. **Program-verify:** Write the Program-verify command to the command register. This command terminates the programming operation. In addition, this command verifies the margin and outputs the byte just programmed in order to compare the array data with the original data programmed. After successful data verification, the programming sequence is initiated again for the next byte address to be programmed.

If data is not verified, the Program sequence is repeated until a successful comparison is verified or the sequence is repeated 25 times.

FUNCTIONAL DESCRIPTION

T-46-13-27

Description Of User Modes

Table 1. Am28F512 User Bus Operations

Operation		$\overline{CE}$ ($\overline{E}$)	$\overline{OE}$ ($\overline{G}$)	$\overline{WE}$ ($\overline{W}$)	V_{PP} (Note 1)	A_0	A_9	I/O
Read-Only	Read	V_{IL}	V_{IL}	X	V_{PPL}	A_0	A_9	D_{OUT}
	Standby	V_{IH}	X	X	V_{PPL}	X	X	HIGH Z
	Output Disable	V_{IL}	V_{IH}	V_{IH}	V_{PPL}	X	X	HIGH Z
	Auto-select Manufacturer Code (Note 2)	V_{IL}	V_{IL}	V_{IH}	V_{PPL}	V_{IL}	V_{ID} (Note 3)	CODE (01H)
	Auto-select Device Code (Note 2)	V_{IL}	V_{IL}	V_{IH}	V_{PPL}	V_{IH}	V_{ID} (Note 3)	CODE (25H)
Read/Write	Read	V_{IL}	V_{IL}	V_{IH}	V_{PPH}	A_0	A_9	D_{OUT} (Note 4)
	Standby (Note 5)	V_{IH}	X	X	V_{PPH}	X	X	HIGH Z
	Output Disable	V_{IL}	V_{IH}	V_{IH}	V_{PPH}	X	X	HIGH Z
	Write	V_{IL}	V_{IH}	V_{IL}	V_{PPH}	A_0	A_9	D_{IN} (Note 6)

Legend:
X = Don't care, where Don't Care is either V_{IL} or V_{IH} levels, $V_{PPL} = V_{PP} < V_{CC} + 2V$, See DC Characteristics for voltage levels of V_{PPH}, $0V < An < V_{CC} + 2V$, (normal TTL or CMOS input levels, where n = 0 or 9).

Notes:

1. V_{PPL} may be grounded, connected with a resistor to ground, or $\leq V_{CC} + 2.0V$. V_{PPH} is the programming voltage specified for the device. Refer to the DC characteristics. When $V_{PP} = V_{PPL}$, memory contents can be read but not written or erased.
2. Manufacturer and device codes may also be accessed via a command register write sequence. Refer to Table 2.
3. $11.5 \leq V_{ID} \leq 13.0V$
4. Read operation with $V_{PP} = V_{PPH}$ may access array data or the Auto select codes.
5. With V_{PP} at high voltage, the standby current is $I_{CC} + I_{PP}$ (standby).
6. Refer to Table 3 for valid D_{IN} during a write operation.
7. All inputs are Don't Care unless otherwise stated, where Don't Care is either V_{IL} or V_{IH} levels. In the Auto select mode all addresses except A_9 and A_0 must be held at V_{IL}.

READ ONLY MODE

$V_{PP} < V_{CC} + 2$ V

Command Register Inactive

Read

The Am28F512 functions as a read only memory when $V_{PP} < V_{CC} + 2$ V. The Am28F512 has two control functions. Both must be satisfied in order to output data. $\overline{CE}$ controls power to the device. This pin should be used for specific device selection. $\overline{OE}$ controls the device outputs and should be used to gate data to the output pins if a device is selected.

Address access time t_{ACC} is equal to the delay from stable addresses to valid output data. The chip enable access time t_{CE} is the delay from stable addresses and stable $\overline{CE}$ to valid data at the output pins. The output enable access time is the delay from the falling edge of $\overline{OE}$ to valid data at the output pins (assuming the addresses have been stable at least $t_{ACC} - t_{OE}$).

Standby Mode

The Am28F512 has two standby modes. The CMOS standby mode ($\overline{CE}$ input held at $V_{CC} \pm 0.5$ V), consumes less than 100 µA of current. TTL standby mode ($\overline{CE}$ is held at V_{IH}) reduces the current requirements to less than 1 mA. When in the standby mode the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

If the device is deselected during erasure, programming, or program/erase verification, the device will draw active current until the operation is terminated.

Output Disable

Output from the device is disabled when $\overline{OE}$ is at a logic high level. When disabled, output pins are in a high impedance state.

Auto Select

Flash memories can be programmed in-system or in a standard PROM programmer. The device may be soldered to the circuit board upon receipt of shipment and programmed in-system. Alternatively, the device may initially be programmed in a PROM programmer prior to soldering the device to the board.

The Auto select mode allows the reading out of a binary code from the device that will identify its manufacturer and type. This mode is intended for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional over the entire temperature range of the device.

Programming In A Prom Programmer

To activate this mode, the programming equipment must force V_{ID} (11.5 V to 13.0 V) on address A_9. Two identifier bytes may then be sequenced from the device outputs by toggling address A_0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL}, and V_{PP} must be less than or equal to $V_{CC} + 2.0$ V while using this Auto select mode. Byte 0 ($A_0 = V_{IL}$) represents the manufacturer code and byte 1 ($A_0 = V_{IH}$) the device identifier code. For the Am28F512 these two bytes are given in the table below. All identifiers for manufacturer and device codes will exhibit odd parity with the MSB (DQ_7) defined as the parity bit.

(Refer to the AUTO SELECT paragraph in the ERASE, PROGRAM, and READ MODE section for programming the Flash memory device in-system).

Table 2. Am28F512 Auto Select Code

Type	A_0	Code (HEX)	DQ_7	DQ_6	DQ_5	DQ_4	DQ_3	DQ_2	DQ_1	DQ_0
Manufacturer Code	V_{IL}	01	0	0	0	0	0	0	0	1
Device Code	V_{IH}	25	0	0	1	0	0	1	0	1

ERASE, PROGRAM, AND READ MODE

T-46-13-27

V_{PP} = 12.0 V ± 5%

Command Register Active

Write Operations

High voltage must be applied to the V_{PP} pin in order to activate the command register. Data written to the register serves as input to the internal state machine. The output of the state machine determines the operational function of the device.

The command register does not occupy an addressable memory location. The register is a latch that stores the command, along with the address and data information needed to execute the command. The register is written by bringing $\overline{WE}$ and $\overline{CE}$ to V_{IL}, while $\overline{OE}$ is at V_{IH}. Addresses are latched on the falling edge of $\overline{WE}$, while data is latched on the rising edge of the $\overline{WE}$ pulse. Standard microprocessor write timings are used.

Register bits R_7 – R_0 correspond to the data inputs DQ_7 – DQ_0 (Refer to Table 3). Register bits R_7 – R_5 store the command data. All register bits R_4 to R_0 must be zero. The only exceptions are: the reset command, when FFH is written to the register and Auto select, when 90H or 80H is written to the register.

The device requires the $\overline{OE}$ pin to be V_{IH} for write operations. This condition eliminates the possibility for bus contention during programming operations. In order to write, $\overline{OE}$ must be V_{IH}, and $\overline{CE}$ and $\overline{WE}$ must be V_{IL}. If any pin is not in the correct state a write command will not be executed.

Refer to AC Write Characteristics and the Erase/Programming Waveforms for specific timing parameters.

Command Definitions

The contents of the command register default to 00H (Read Mode) in the absence of high voltage applied to the V_{PP} pin. The device operates as a read only memory. High voltage on the V_{PP} pin enables the command register. Device operations are selected by writing specific data codes into the command register. Table 4 defines these register commands.

Read Command

Memory contents can be accessed via the read command when V_{PP} is high. To read from the device, write 00H into the command register. Wait 6 µs before reading the first accessed address location. All subsequent Read operations take t_{ACC}. Standard microprocessor read cycles access data from the memory. The device will remain in the read mode until the command register contents are altered.

The command register defaults to 00H (read mode) upon V_{PP} power-up. The 00H (Read Mode) register default helps ensure that inadvertent alteration of the memory contents does not occur during the V_{PP} power transition. Refer to the AC Read Characteristics and Waveforms for the specific timing parameters.

Table 3. Command Register

Data Input/Output	DQ_7	DQ_6	DQ_5	DQ_4	DQ_3	DQ_2	DQ_1	DQ_0
Command Register	R_7	R_6	R_5	R_4	R_3	R_2	R_1	R_0
Data/Commands*	X	X	X	X	X	X	X	X

*** Notes:**

1. See Table 4 Am28F512 Command Definitions
2. X = Appropriate Data or Register Commands

Table 4. Am28F512 Command Definitions

Command	First Bus Cycle			Second Bus Cycle		
	Operation (Note 1)	Address (Note 2)	Data (Note 3)	Operation (Note 1)	Address (Note 2)	Data (Note 3)
Read Memory (Notes 6, 7)	Write	X	00H/FFH	Read	RA	RD
Read Auto select	Write	X	80H or 90H	Read	00H/01H	01H/25H
Set-up Erase/Erase (Note 4)	Write	X	20H	Write	X	20H
Erase-Verify (Note 4)	Write	EA	A0H	Read	X	EVD
Set-up Program/Program (Note 5)	Write	X	40H	Write	PA	PD
Program-Verify (Note 5)	Write	X	C0H	Read	X	PVD
Reset (Note 7)	Write	X	FFH	Write	X	FFH

Notes:

1. Bus operations are defined in Table 1.
2. RA = Address of the memory location to be read.
   EA = Address of the memory location to be read during erase-verify.
   PA = Address of the memory location to be programmed.
   Addresses are latched on the falling edge of the $\overline{WE}$ pulse.
3. RD = Data read from location RA during read operation.
   EVD = Data read from location EA during erase-verify.
   PD = Data to be programmed at location PA. Data latched on the rising edge of $\overline{WE}$.
   PVD = Data read from location PA during program-verify. PA is latched on the Program command.
4. Figure 1 illustrates the Flasherase Electrical Erase Algorithm.
5. Figure 2 illustrates the Flashrite Programming Algorithm.
6. Wait 6 µs after first Read command before accessing the data. When the second bus command is a Read command, all subsequent Read operations take t_{ACC}.
7. Please refer to Reset Command section on page 5-47.

Erase Sequence

Set-up Erase/Erase Commands

Set-up Erase

Set-up Erase is the first of a two-cycle erase command. It is a command-only operation that stages the device for bulk chip erase. The array contents are not altered with this command. 20H is written to the command register in order to perform the Set-up Erase operation.

Erase

The second two-cycle erase command initiates the bulk erase operation. You must write the Erase command (20H) again to the register. The erase operation begins with the rising edge of the $\overline{WE}$ pulse. The erase operation must be terminated by writing a new command (Erase-verify) to the register.

This two step sequence of the Set-up and Erase commands helps to ensure that memory contents are not accidentally erased. Also, chip erasure can only occur when high voltage is applied to the V_{PP} pin and all control pins are in their proper state. In absence of this high voltage, memory contents cannot be altered. Refer to AC Erase Characteristics and Waveforms for specific timing parameters.

Note:
The Flash memory device must be fully programmed to 00H data prior to erasure. This equalizes the charge on all memory cells ensuring reliable erasure.

Erase-verify Command

The erase operation erases all bytes of the array in parallel. After the erase operation, all bytes must be sequentially verified. The Erase-verify operation is initiated by writing A0H to the register. The byte address to be verified must be supplied with the command. Addresses are latched on the falling edge of the $\overline{WE}$ pulse. The rising edge of the $\overline{WE}$ pulse terminates the erase operation.

Margin Verify

During the Erase-verify operation, the Am28F512 applies an internally generated margin voltage to the addressed byte. Reading FFH from the addressed byte indicates that all bits in the byte are properly erased.

Verify Next Address

You must write the Erase-verify command with the appropriate address to the register prior to verification of each address. Each new address is latched on the falling edge of $\overline{WE}$. The process continues for each byte in

the memory array until a byte does not return FFH data or all the bytes in the array are accessed and verified.

If an address is not verified to FFH data, the entire chip is erased again (refer to Set-up Erase/Erase). Erase verification then resumes at the address that failed to verify. Erase is complete when all bytes in the array have been verified. The device is now ready to be programmed. At this point, the verification operation is terminated by writing a valid command (e.g. Program set-up) to the command register. Figure 1 and Table 5, the Flasherase electrical erase algorithm, illustrate how commands and bus operations are combined to perform electrical erasure. Refer to AC Erase Characteristics and Waveforms for specific timing parameters.

Note:
The erase-verify command must be written to the register in order to terminate the erase operation. During the erase operations, the local microprocessor must be dedicated to run software timing routines (erase in 10ms) as specified in AMD's Flasherase algorithm.

Should a system interrupt occur during an erase operation, always write the Erase-verify command prior to executing an interrupt sequence.

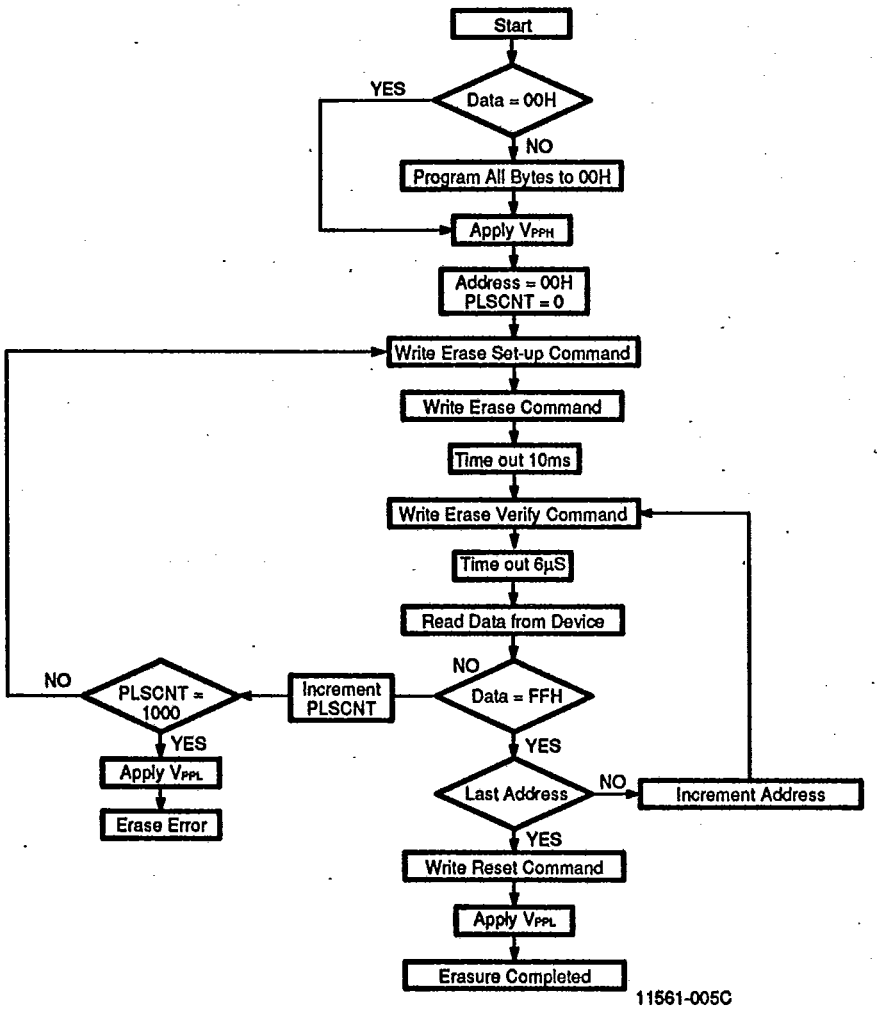


Figure 1. Flasherase Electrical Erase Algorithm

Flasherase Electrical Erase Algorithm

This Flash memory device erases the entire array in parallel. The erase time depends on V_{PP}, temperature, and number of erase/program cycles on the device. In general, reprogramming time increases as the number of erase/program cycles increases.

The Flasherase electrical erase algorithm employs an interactive closed loop flow to simultaneously erase all bits in the array. Erasure begins with a read of the memory contents. The Am28F512 is erased when shipped from the factory. Reading FFH data from the device would immediately be followed by executing the Flashrite programming algorithm with the appropriate data pattern.

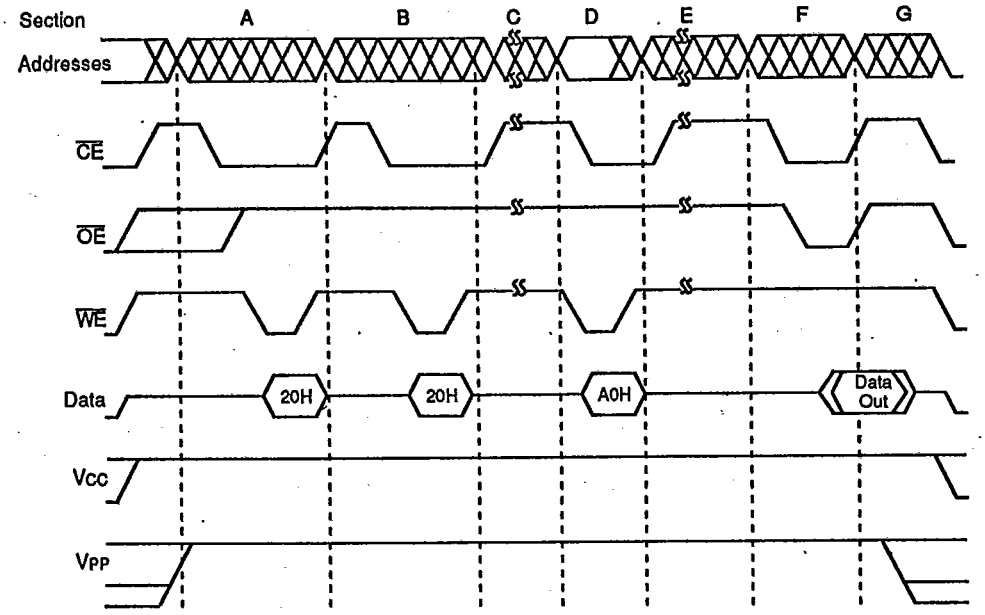
Should the device be currently programmed, data other than FFH will be returned from address locations. Follow the Flasherase algorithm. Uniform and reliable erasure is ensured by first programming all bits in the device to their charged state (Data = 00H). This is accomplished using the Flashrite programming algorithm. Erasure then continues with an initial erase operation. Erase verification (Data = FFH) begins at address 0000H and continues through the array to the last address, or until data other than FFH is encountered. If a byte fails to verify, the device is erased again. With each erase operation, an increasing number of bytes verify to the erased state. Typically, devices are erased in less than 100 pulses (1 second). Erase efficiency may be improved by storing the address of the last byte that fails to verify in a register. Following the next erase operation, verification may start at the stored address location. A total of 1000 erase operations are allowed per reprogram cycle, which corresponds to approximately 10 seconds of cumulative erase time. Erasure typically occurs in one second. The entire sequence of erase and byte verification is performed with high voltage applied to the V_{PP} pin. Figure 1 illustrates the electrical erase algorithm.

Table 5. Flasherase Electrical Erase Algorithm

Bus Operations	Command	Comments
		Entire memory must = 00H before erasure (Note 3) **Note:** Use Flashrite programming algorithm (Figure 2) for programming.
Standby		Wait for V_{PP} ramp to V_{PPH} (Note 1) Initialize: Addresses PLSCNT (Pulse count)
Write	Set-Up Erase	Data = 20H
Write	Erase	Data = 20H
Standby		Duration of Erase Operation (t_{WHWH2})
Write	Erase-verify (Note 2)	Address = Byte to Verify Data = A0H Stops Erase Operation
Standby		Write Recovery Time before Read = 6µs
Read		Read byte to verify erasure
Standby		Compare output to FFH Increment pulse count
Write	Reset	Data = FFH, reset the register for read operations.
Standby		Wait for V_{PP} ramp to V_{PPL} (Note 1)

Notes:

1. See DC Characteristics for value of V_{PPH} or V_{PPL}. The V_{PP} power supply can be hard-wired to the device or switchable. When V_{PP} is switched, V_{PPL} may be ground, no connect with a resistor tied to ground, or less than V_{CC} + 2.0V.
2. Erase Verify is performed only after chip erasure. A final read compare may be performed (optional) after the register is written with the read command.
3. The erase algorithm **Must Be Followed** to ensure proper and reliable operation of the device.



	A	B	C	D	E	F	G
Bus Cycle	Write	Write	Time -out	Write	Time -out	Read	Stand by
Command	20H	20H	N/A	A0H	N/A	Compare Data	N/A
Function	Set-up Erase	Erase	Erase (10ms)	Erase-verify	Transition (6µs)	Erase verification	Stand by & Vcc Power down

Figure 2. A.C. Waveforms For Erase Operations

Analysis Of Erase Timing Waveform

Note:
This analysis does not include the requirement to program the entire array to 00H data prior to erasure. Refer to the Flasherase algorithm.

Set-up Erase/Erase

This analysis illustrates the use of two-cycle erase commands (section A&B). The first erase command (20H) is a set-up command and does not affect the array data (section A). The second erase command (20H) initiates the erase operation (section B) on the rising edge of this $\overline{WE}$ pulse. All bytes of the memory array are erased in parallel. No address information is required.

The erase pulse occurs in section C.

Time-out

A software timing routine (10 ms duration) must be initiated on the rising edge of the $\overline{WE}$ pulse of section B.

Erase-verify

Upon completion of the erase software timing routine, the microprocessor must write the Erase-verify command (A0H). This command terminates the erase operation on the rising edge of the $\overline{WE}$ pulse (section D). The Erase-verify command also stages the device for data verification (section F).

After each erase operation each byte must be verified. The byte address to be verified must be supplied with the Erase-verify command (section D). Addresses are latched on the falling edge of the $\overline{WE}$ pulse.

Another software timing routine (6 µs duration) must be executed to allow for generation of internal voltages for margin checking and read operation (section E).

During Erase-verification (section F) each address that returns FFH data is successfully erased. Each address of the array is sequentially verified in this manner by repeating sections D thru F until the entire array is verified or an address fails to verify. Should an address location fail to verify to FFH data, erase the device again. Repeat sections A thru F. Resume verification (section D) with the failed address.

Each data change sequence allows the device to use up to 1,000 erase pulses to completely erase. Typically 100 erase pulses are required.

Notes:

1. All address locations must be programmed to 00H prior to erase. This equalizes the charge on all memory cells and ensures reliable erasure.

2. The erase verify command must be written to terminate the erase operation. Should a system interrupt occur during an erase operation, always write the erase-verify command prior to executing an interrupt sequence.

Programming Sequence

Set-up Program/Program Command

Set-up Program

The Am28F512 is programmed byte by byte. Bytes may be programmed sequentially or at random. Set-up Program is the first of a two-cycle program command. It stages the device for byte programming. The Set-up Program operation is performed by writing 40H to the command register.

Program

Only after the program set-up operation is completed will the next $\overline{WE}$ pulse initiate the active programming operation. The appropriate address and data for programming must be available on the second $\overline{WE}$ pulse. Addresses and data are internally latched on the falling and rising edge of the $\overline{WE}$ pulse respectively. The rising edge of $\overline{WE}$ also begins the programming operation. You must write the Program-verify command to terminate the programming operation. This two step sequence of the Set-up and Program commands helps to ensure that memory contents are not accidentally written. Also, programming can only occur when high voltage is applied to the V_{PP} pin and all control pins are in their proper state. In absence of this high voltage, memory contents cannot be programmed.

Refer to AC Characteristics and Waveforms for specific timing parameters.

Program Verify Command

Following each programming operation, the byte just programmed must be verified.

Write C0H into the command register in order to initiate the Program-verify operation. The rising edge of this $\overline{WE}$ pulse terminates the programming operation. The Program-verify operation stages the device for verification of the last byte programmed. Addresses were previously latched. No new information is required.

Margin Verify

During the Program-verify operation, the Am28F512 applies an internally generated margin voltage to the addressed byte. A normal microprocessor read cycle outputs the data. A successful comparison between the programmed byte and the true data indicates that the byte was successfully programmed. The original programmed data should be stored for comparison. Programming then proceeds to the next desired byte location. Should the byte fail to verify, reprogram (refer to Set-up Program/Program). Figure 3 and Table 6 indicate how instructions are combined with the bus operations to perform byte programming. Refer to AC Programming Characteristics and Waveforms for specific timing parameters.

Flashrite Programming Algorithm

The Am28F512 Flashrite programming algorithm employs an interactive closed loop flow to program data byte by byte. Bytes may be programmed sequentially or at random. The Flashrite programming algorithm uses 10 microsecond programming pulses. Each operation is followed by a byte verification to determine when the addressed byte has been successfully programmed. The program algorithm allows for up to 25 programming operations per byte per reprogramming cycle. Most bytes verify after the first or second pulse. The entire sequence of programming and byte verification is performed with high voltage applied to the V_{PP} pin. Figure 3 and Table 6 illustrate the programming algorithm.

T-46-13-27

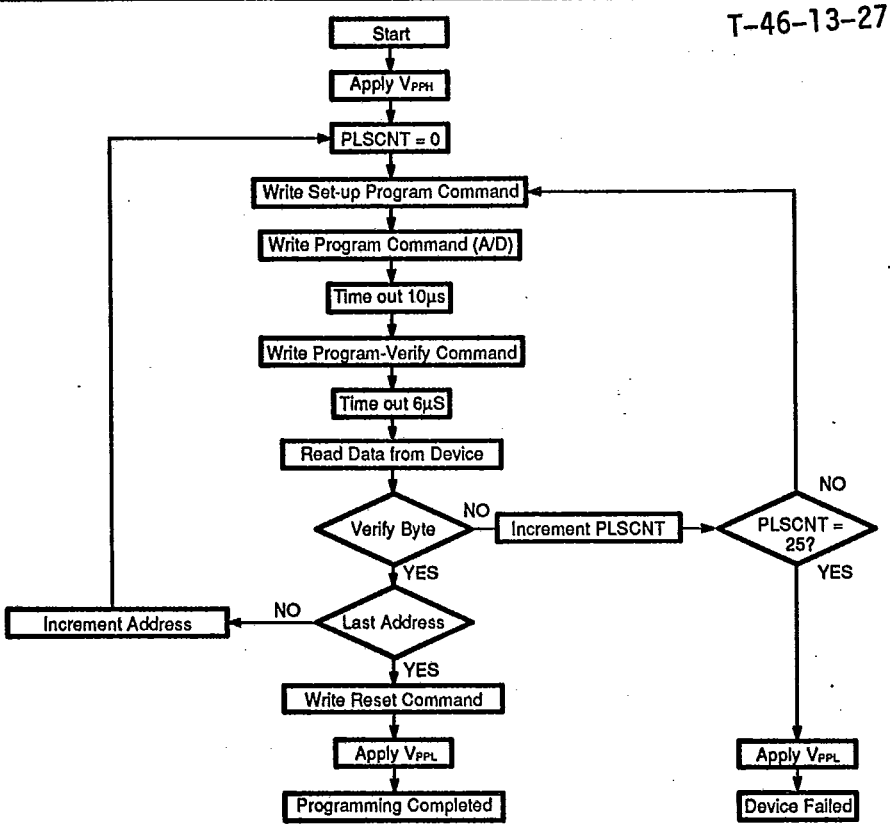


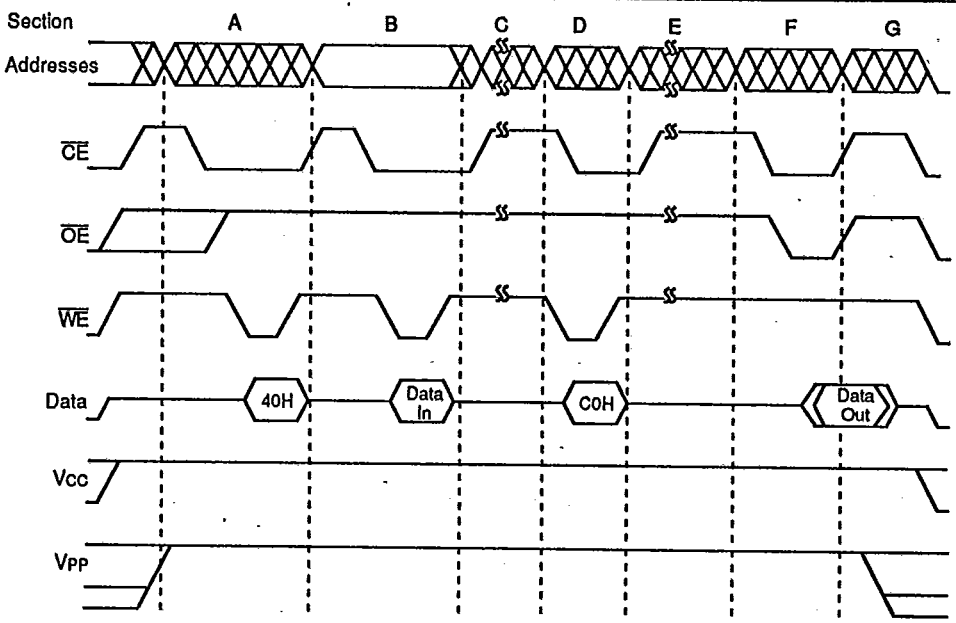
Figure 3. Flashrite Programming Algorithm

Table 6. Flashrite Programming Algorithm

Bus Operations	Command	Comments
Standby		Wait for V_{PP} ramp to V_{PPH} (Note 1) Initialize pulse counter
Write	Set-Up Program	Data = 40H
Write	Program	Valid Address/Data
Standby		Duration of Programming Operation (t_{WHWH1})
Write	Program-Verify (2)	Data = C0H Stops Program Operation
Standby		Write Recovery Time before Read = 6µs
Read		Read byte to verify programming
Standby		Compare data output to data expected
Write	Reset	Data = FFH, resets the register for read operations.
Standby		Wait for V_{PP} ramp to V_{PPL} (Note 1)

Notes:

1. See DC Characteristics for value of V_{PPH}. The V_{PP} power supply can be hard-wired to the device or switchable. When V_{PP} is switched, V_{PPL} may be ground, no connect with a resistor tied to ground, or less than V_{CC} + 2.0V.
2. Program Verify is performed only after byte programming. A final read/compare may be performed (optional) after the register is written with the read command.



	A	B	C	D	E	F	G
Bus Cycle	Write	Write	Time -out	Write	Time -out	Read	Stand by
Command	40H	Program Address, Program Data	N/A	C0H (Stops Program)	N/A	Compare Data	N/A
Function	Set-up Program	Program Command Latch Address & Data	Program (10 µs)	Program verify	Transition (6 µs)	Program verification	Stand by & Vcc Power down

Figure 4. A.C. Waveforms for Programming Operations

Analysis Of Program Timing Waveforms

Set-up Program/Program

Two-cycle write commands are required for program operations (section A&B). The first program command (40H) is a set-up command and does not affect the array data (section A). The second program command latches address and data required for programming on the falling and rising edge of $\overline{WE}$ respectively (section B). The rising edge of this $\overline{WE}$ pulse (section B) also initiates the programming pulse. The device is programmed on a byte by byte basis either sequentially or randomly.

The program pulse occurs in section C.

Time-out

A software timing routine (10 µs duration) must be initiated on the rising edge of the $\overline{WE}$ pulse of section B.

Program-verify

Upon completion of the program timing routine, the microprocessor must write the program-verify command (C0H). This command terminates the programming operation on the rising edge of the $\overline{WE}$ pulse (section D). The program-verify command also stages the device for data verification (section F). Another software timing routine (6 µs duration) must be executed to allow for generation of internal voltages for margin checking and read operations (section E).

During program-verification (section F) each byte just programmed is read to compare array data with original program data. When successfully verified, the next desired address is programmed. Should a byte fail to verify, reprogram the byte (repeat section A thru F). Each data change sequence allows the device to use up to 25 program pulses per byte. Typically, bytes are verified within one or two pulses.

Note:
The program-verify operation must be written to terminate the programming operation. Should a system interrupt occur during a programming operation, always write the program-verify command prior to executing an interrupt sequence.

Algorithm Timing Delays

There are four different timing delays associated with the Flasherase and Flashrite algorithms:

1. The first delay is associated with the V_{PP} rise-time when V_{PP} first turns on. The capacitors on the V_{PP} bus cause an RC ramp. After switching on the V_{PP}, the delay required is proportional to the number of devices being erased and the 0.1 µF/device. V_{PP} must reach its final value 100ns before commands are executed.
2. The second delay time is the erase time pulse width (10 ms). A software timing routine should be run by the local microprocessor to time out the delay. The erase operation must be terminated at the conclusion of the timing routine or prior to executing any system interrupts that may occur during the erase operation. To ensure proper device operation, write the Erase-verify operation after each pulse, or the device may continue to erase until the memory cells are driven into depletion (over-erasure). Should this happen the internal circuitry will no longer select unique addresses. A symptom of over-erasure is an error attempting to program the next time. Occasionally it is possible to recover over-erased devices by programming all of the locations with 00H data.
3. A third delay time is required for each programming pulse width (10 µs). The programming algorithm is interactive and verifies each byte after a program pulse. The program operation must be terminated at the conclusion of the timing routine or prior to executing any system interrupts that may occur during the programming operation.
4. A fourth timing delay associated with both the Flasherase and Flashrite algorithms is the write recovery time (6 µs). During this time internal circuitry is changing voltage levels from the erase/ program level to those used for margin verify and read operations. An attempt to read the device during this period will result in possible false data (it may appear the device is not properly erased or programmed).

Note:
Software timing routines should be written in machine language for each of the delays. Code written in machine language requires knowledge of the appropriate microprocessor clock speed in order to accurately time each delay.

Parallel Device Erasure

Many applications will use more than one Flash memory device. Total erase time may be minimized by implementing a parallel erase algorithm. Flash memories may erase at different rates. Therefore each device must be verified seperately. When a device is completely erased and verified use a masking code to prevent further erasure. The other devices will continue to erase until verified. The masking code applied could be the read command (00H).

Power-up Sequence

V_{CC} Prior to V_{PP}

The Am28F512 powers-up in the Read only mode. In addition, memory contents may only be altered after successful completion of a two step command sequence.

V_{PP} Prior to V_{CC}

When V_{CC} = 0 V, the V_{PP} voltage is internally disabled from the device. Memory contents cannot be altered. With V_{PP} = 12 V, the Flash device resets to the Read mode when V_{CC} rises above 2 V.

Power supply sequencing is not required.

Reset Command

The Reset command initializes the Flash memory device to the Read mode. In addition, it also provides the user with a safe method to abort any device operation (including program or erase).

The Reset command must be written two consecutive times after the set-up Program command (40H). This will reset the device to the Read mode.

Following any other Flash command, write the Reset command once to the device. This will safely abort any previous operation and initialize the device to the Read mode.

The set-up Program command (40H) is the only command that requires a two sequence reset cycle. The first Reset command is interpreted as program data. However, FFH data is considered null data during programming operations (memory cells are only programmed from a logical "1" to "0"). The second Reset command safely aborts the programming operation and resets the device the Read mode.

Memory contents are not altered in any case.

This detailed information is for your reference. It may prove easier to always issue the Reset command two consecutive times. This eliminates the need to determine if you are in the set-up Program state or not.

Auto Select Command

Flash memories can be programmed in-system or in a standard PROM programmer. The device may be soldered to the circuit board upon receipt of shipment and programmed in-system. Alternatively, the device may initially be programmed in a PROM programmer prior to soldering the device to the board.

Programming In-system

AMD's Flash memories are designed for use in applications where the local CPU alters memory contents. Accordingly, manufacturer and device codes must be accessible while the device resides in the target system. PROM programmers typically access the signature codes by raising A_9 to a high voltage. However, multiplexing high voltage onto address lines is not a generally desired system design practice.

The Am28F512 contains an Auto Select operation to supplement traditional PROM programming methodology. The operation is initiated by writing 80H or 90H into the command register. Following this command, a read cycle address 0000H retrieves the manufacturer code of 01H. A read cycle from address 0001H returns the device code 25H (See Table 2). To terminate the operation, it is necessary to write another valid command into the register (See Table 3).

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	
Ceramic Packages	−65°C to +150°C
Plastic Packages	−65°C to +125°C
Ambient Temperature with Power Applied	−55°C to + 125°C
Voltage with Respect To Ground All pins except A_9 and V_{PP} (Note 1)	−2.0 V to 7.0 V
V_{CC} (Note 1)	−2.0 V to 7.0 V
A_9 (Note 2)	−2.0 V to 14.0 V
V_{PP} (Note 2)	−2.0 V to 14.0 V
Output Short Circuit Current (Note 3)	200 mA

Notes:

1. *Minimum DC voltage on input or I/O pins is −0.5 V. During voltage transitions, inputs may overshoot V_{SS} to −2.0 V for periods of up to 20 ns. Maximum DC voltage on output and I/O pins is V_{CC} + 0.5 V. During voltage transitions, outputs may overshoot to V_{CC} + 2.0 V for periods up to 20 ns.*
2. *Minimum DC input voltage on A_9 and V_{PP} pins is −0.5V. During voltage transitions, A_9 and V_{PP} may overshoot V_{SS} to −2.0 V for periods of up to 20 ns. Maximum DC input voltage on A_9 and V_{PP} is +13.5 V which may overshoot to 14.0 V for periods up to 20 ns.*
3. *No more than one output shorted at a time. Duration of the short circuit should not be greater than one second.*

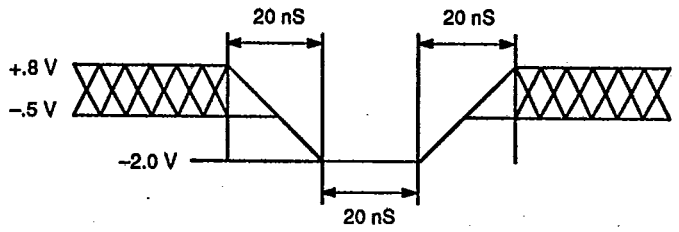
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices	
Case Temperature (Tc)	0°C to +70°C
Industrial (I) Devices	
Case Temperature (Tc)	−40°C to +85°C
Extended (E) Devices	
Case Temperature (Tc)	−55°C to +125°C
Military (M) Devices	
Case Temperature (Tc)	−55°C to +125°C
V_{CC} Supply Voltages	
V_{CC} for Am28F512–X5	+4.75 V to +5.25 V
V_{CC} for Am28F512–XX0	+4.50 V to +5.50 V
V_{PP} Supply Voltages	
Read	−0.5 V to +12.6 V
Program, Erase, and Verify	+11.4 V to +12.6 V

MAXIMUM OVERSHOOT

Maximum Negative Input Overshoot



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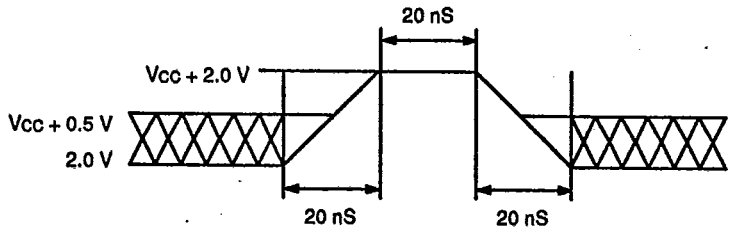
Maximum Negative Overshoot Waveform

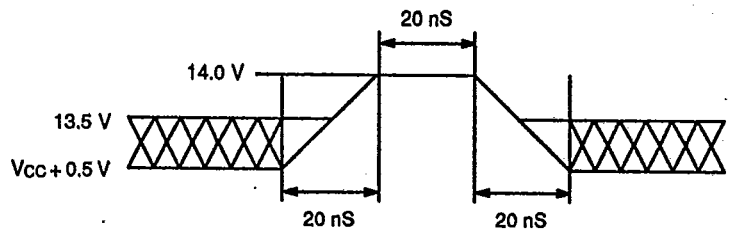
Maximum Positive Input Overshoot



11561-010A

Maximum Positive Overshoot Waveform

Maximum V_{PP} Overshoot



11561-011A

Maximum V_{PP} Overshoot Waveform

DC CHARACTERISTICS over operating range unless otherwise specified (for APL Products, Group A, Subgroups 1, 2, 3, 7 and 8 are tested unless otherwise noted). (Notes 1–3)

T-46-13-27

DC CHARACTERISTICS-TTL/NMOS COMPATIBLE

PRELIMINARY

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
I_{LI}	Input Leakage Current	V_{CC} = V_{CC} Max., V_{IN} = V_{CC} or V_{SS}		±1.0	µA
I_{LO}	Output Leakage Current	V_{CC} = V_{CC} Max., V_{OUT} = V_{CC} or V_{SS}		±1.0	µA
I_{CCS}	V_{CC} Standby Current	V_{CC} = V_{CC} Max. $\overline{CE}$ = V_{IH}		1.0	mA
I_{CC1}	V_{CC} Active Read Current	V_{CC} = V_{CC} Max., $\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH} I_{OUT} = 0 mA, at 6 MHz		30	mA
I_{CC2}	V_{CC} Programming Current	$\overline{CE}$ = V_{IL} Programming in Progress		30	mA
I_{CC3}	V_{CC} Erase Current	$\overline{CE}$ = V_{IL} Erasure in Progress		30	mA
I_{PPS}	V_{PP} Standby Current	V_{PP} = V_{PPL}		±1.0	µA
I_{PP1}	V_{PP} Read Current	V_{PP} = V_{PPH}		200	µA
		V_{PP} = V_{PPL}		±1.0	
I_{PP2}	V_{PP} Programming Current	V_{PP} = V_{PPH} Programming in Progress		30	mA
I_{PP3}	V_{PP} Erase Current	V_{PP} = V_{PPH} Erasure in Progress		30	mA
V_{IL}	Input Low Voltage		–0.5	0.8	V
V_{IH}	Input High Voltage		2.0	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 5.8 mA V_{CC} = V_{CC} Min.		0.45	V
V_{OH1}	Output High Voltage	I_{OH} = –2.5 mA V_{CC} = V_{CC} Min.	2.4		V
V_{ID}	A_9 Auto Select Voltage	A_9 = V_{ID}	11.5	13.0	V
I_{ID}	A_9 Auto Select Current	A_9 = V_{ID} Max. V_{CC} = V_{CC} Max.		50	µA
V_{PPL}	V_{PP} during Read-Only Operations	**Note:** Erase/Program are inhibited when V_{PP} = V_{PPL}	0.0	V_{CC} + 2.0	V
V_{PPH}	V_{PP} during Read/Write Operations		11.4	12.6	V

DC CHARACTERISTICS-CMOS COMPATIBLE

PRELIMINARY

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
I_{LI}	Input Leakage Current	V_{CC} = V_{CC} Max., V_{IN} = V_{CC} or V_{SS}		±1.0	µA
I_{LO}	Output Leakage Current	V_{CC} = V_{CC} Max., V_{OUT} = V_{CC} or V_{SS}		±1.0	µA
I_{CCS}	V_{CC} Standby Current	V_{CC} = V_{CC} Max. $\overline{CE}$ = V_{CC} ± 0.5 V		100	µA
I_{CC1}	V_{CC} Active Read Current	V_{CC} = V_{CC} Max., $\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH} I_{OUT} = 0 mA, at 6 MHz		30	mA
I_{CC2}	V_{CC} Programming Current	$\overline{CE}$ = V_{IL} Programming in Progress		30	mA
I_{CC3}	V_{CC} Erase Current	$\overline{CE}$ = V_{IL} Erasure in Progress		30	mA
I_{PPS}	V_{PP} Standby Current	V_{PP} = V_{PPL}		±1.0	µA
I_{PP1}	V_{PP} Read Current	V_{PP} = V_{PPH}		200	µA
I_{PP2}	V_{PP} Programming Current	V_{PP} = V_{PPH} Programming in Progress		30	mA
I_{PP3}	V_{PP} Erase Current	V_{PP} = V_{PPH} Erasure in Progress		30	mA
V_{IL}	Input Low Voltage		–0.5	0.8	V
V_{IH}	Input High Voltage		0.7 V_{CC}	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 5.8 mA V_{CC} = V_{CC} Min.		0.45	V
V_{OH1}	Output High Voltage	I_{OH} = –2.5 mA, V_{CC} = V_{CC} Min.	0.85 V_{CC}		V
V_{OH2}		I_{OH} = –100 µA, V_{CC} = V_{CC} Min.	V_{CC} –0.4		
V_{ID}	A_9 Auto Select Voltage	A_9 = V_{ID}	11.5	13.0	V
I_{ID}	A_9 Auto Select Current	A_9 = V_{ID} Max. V_{CC} = V_{CC} Max.		50	µA
V_{PPL}	V_{PP} during Read-Only Operations	**Note:** Erase/ Program are inhibited when V_{PP} = V_{PPL}	0.0	V_{CC} + 2.0	V
V_{PPH}	V_{PP} during Read/Write Operations		11.4	12.6	V

Notes:

1. **Caution:** the Am28F512 must not be removed from (or inserted into) a socket when V_{CC} or V_{PP} is applied.
2. I_{CC1} is tested with $\overline{OE}$ = V_{IH} to simulate open outputs.
3. Maximum active power usage is the sum of I_{CC} and I_{PP}.

PIN CAPACITANCE

Parameter Symbol	Parameter Description	Test Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	$V_{IN} = 0$	8	10	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0$	8	12	pF
C_{IN2}	V_{PP} Input Capacitance	$V_{PP} = 0$	8	12	pF

Notes:

1. Sampled, not 100% tested.
2. Test conditions $T_A = 25°C$, f = 1.0 MHz

SWITCHING CHARACTERISTICS over operating range unless otherwise specified

AC CHARACTERISTICS-Read Only Operation (Notes 1– 2)

PRELIMINARY

Parameter Symbols		Parameter Description		Am28F512				Unit
JEDEC	Standard			-90 -95	-120 —	-150 —	-200 —	
t_{AVAV}	t_{RC}	Read Cycle Time	Min. Max.	90	120	150	200	ns
t_{ELQV}	t_{CE}	Chip Enable Access Time	Min. Max.	90	120	150	200	ns
t_{AVQV}	t_{ACC}	Address Access Time	Min. Max.	90	120	150	200	ns
t_{GLQV}	t_{OE}	Output Enable Access Time	Min. Max.	35	50	75	75	ns
t_{ELQX}	t_{LZ}	Chip Enable to Output in Low Z	Min. Max.	0	0	0	0	ns
t_{EHQZ}	t_{DF}	Chip Disable to Output in High Z	Min. Max.	25	30	35	35	ns
t_{GLQX}	t_{OLZ}	Output Enable to Output in Low Z	Min. Max.	0	0	0	0	ns
t_{GHQZ}	t_{DF}	Output Disable to Output in High Z	Min. Max.	25	30	35	35	ns
t_{AXQX}	t_{OH}	Output Hold from first of Address, $\overline{CE}$, or $\overline{OE}$ Change	Min. Max.	0	0	0	0	ns
t_{WHGL}		Write Recovery Time before Read	Min. Max.	6	6	6	6	µs
t_{VCS}		Vcc Set-up Time to Valid Read	Min. Max.	50	50	50	50	µs

Notes:

1. Output Load (except Am28F512-95): 1 TTL gate and $C_L = 100$ pF, Input Rise and Fall Times: ≤ 10 ns, Input Pulse levels: 0.45 to 2.4 V, Timing Measurement Reference Level - Inputs: 0.8 V and 2 V
   Outputs: 0.8 V and 2 V
2. The Am28F512-95 Output Load: 1 TTL gate and $C_L = 30$ pF
   Input Rise and Fall Times: ≤ 10 ns
   Input Pulse levels: 0 to 3 V
   Timing Measurement Reference Level: 1.5 V inputs and outputs.
3. t_{VCS} is guaranteed by design not tested.

AC CHARACTERISTICS-Write/Erase/Program Operations (Notes 1– 4)

PRELIMINARY

Parameter Symbols		Parameter Description		Am28F512				Unit
JEDEC	Standard			-90 -95	-120 —	-150 —	-200 —	
t_{AVAV}	t_{WC}	Write Cycle Time	Min. Max.	90	120	150	200	ns
t_{AVWL}	t_{AS}	Address Set-Up Time	Min. Max.	0	0	0	0	ns
t_{WLAX}	t_{AH}	Address Hold Time	Min. Max.	45	50	60	75	ns
t_{DVWH}	t_{DS}	Data Set-Up Time	Min. Max.	45	50	50	50	ns
t_{WHDX}	t_{DH}	Data Hold Time	Min. Max.	10	10	10	10	ns
t_{WHGL}	t_{WR}	Write Recovery Time before Read	Min. Max.	6	6	6	6	µs
t_{GHWL}		Read Recovery Time before Write	Min. Max.	0	0	0	0	µs
t_{ELWL}	t_{CS}	Chip Enable Set-Up Time	Min. Max.	0	0	0	0	ns
t_{WHEH}	t_{CH}	Chip Enable Hold Time	Min. Max.	0	0	0	0	ns
t_{WLWH}	t_{WP}	Write Pulse Width	Min. Max.	45	50	50	50	ns
t_{WHWL}	t_{WPH}	Write Pulse Width HIGH	Min. Max.	20	20	20	20	ns
t_{WHWH1}		Duration of Programming Operation	Min. Max.	10 25	10 25	10 25	10 25	µs
t_{WHWH2}		Duration of Erase Operation	Min. Max.	9.5 10.5	9.5 10.5	9.5 10.5	9.5 10.5	ms
t_{EHVP}		Chip Enable Set-Up Time to V_{PP} Ramp	Min. Max.	100	100	100	100	ns
t_{VPEL}		V_{PP} Set-Up Time to Chip Enable LOW	Min. Max.	100	100	100	100	ns
t_{VCS}		Vcc Set-Up Time to Chip Enable Low	Min. Max.	50	50	50	50	µs
t_{VPPR}		V_{PP} Rise Time 90% V_{PPH}	Min. Max.	500	500	500	500	ns
t_{VPPF}		V_{PP} Fall Time 90% V_{PPL}	Min. Max.	500	500	500	500	ns

Notes:

1. Read timing characteristics during read/write operations are the same as durng read-only operations. Refer to AC Characteristics for Read Only operations.
2. Chip-Enable Controlled Writes: Write operations are driven by the valid combination of Chip-Enable and Write-Enable. In systems where Chip-Enable defines the Write Pulse Width (within a longer Write-Enable timing waveform) all set-up, hold and inactive Write-Enable times should be measured relative to the Chip-Enable waveform.
3. All devices except Am28F512-95. Input Rise and Fall times: ≤ 10 ns; Input Pulse Levels: 0.45 V to 2.4 V Timing Measurement Reference Level: Inputs: 0.8 V and 2.0 V; Outputs: 0.8 V and 2.0 V
4. Am28F512-95. Input Rise and Fall times: ≤ 10 ns; Input Pulse Levels: 0.0 V to 3.0 V Timing Measurement Reference Level: Inputs and Outputs: 1.5 V

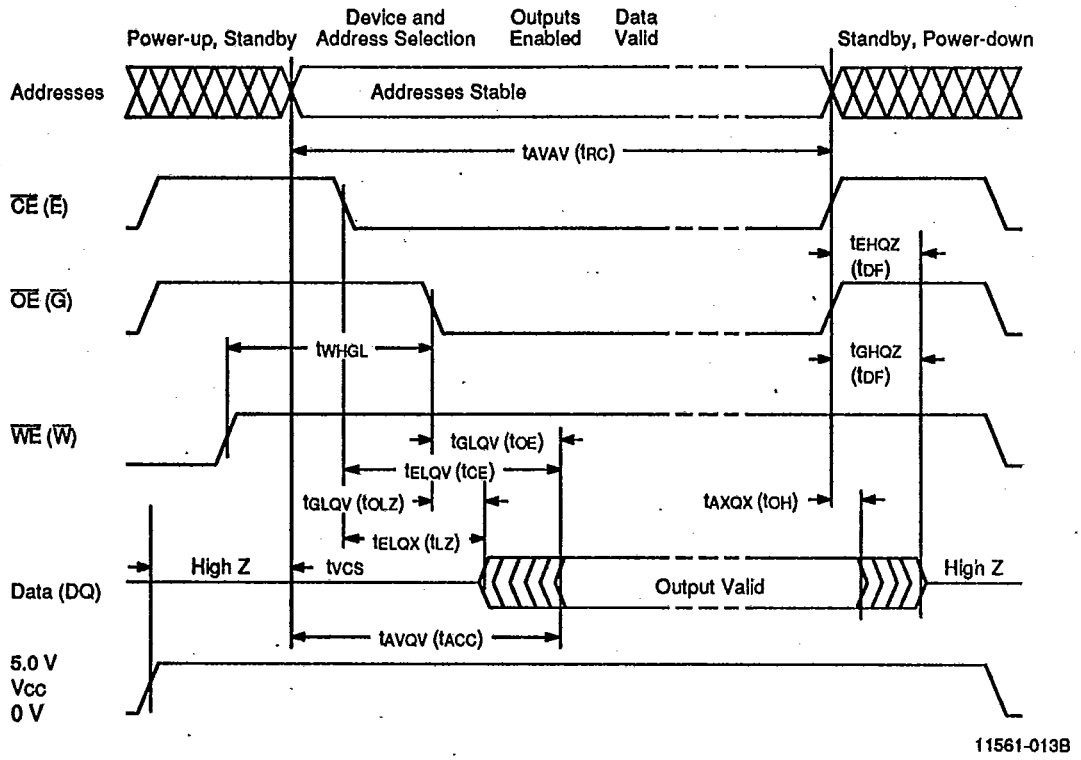


Figure 5. AC Waveforms for Read Operations

T-46-13-27

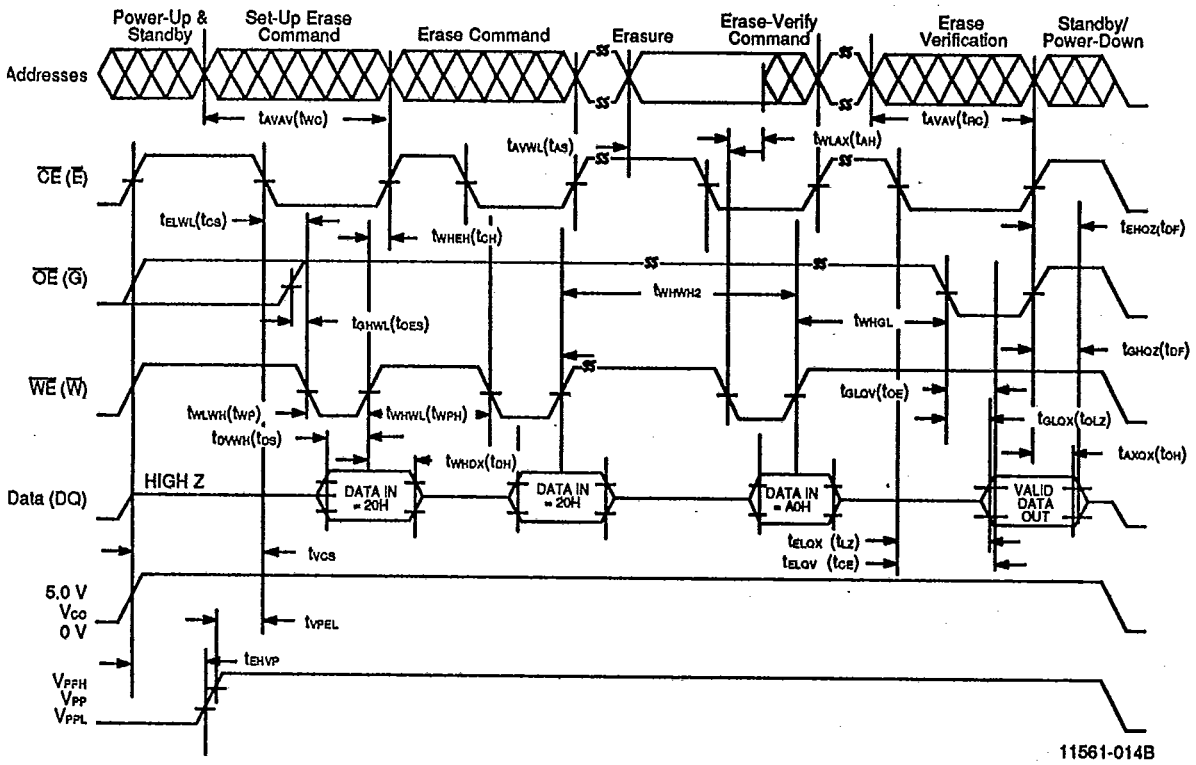


Figure 6. AC Waveforms for Erase Operations

T-46-13-27

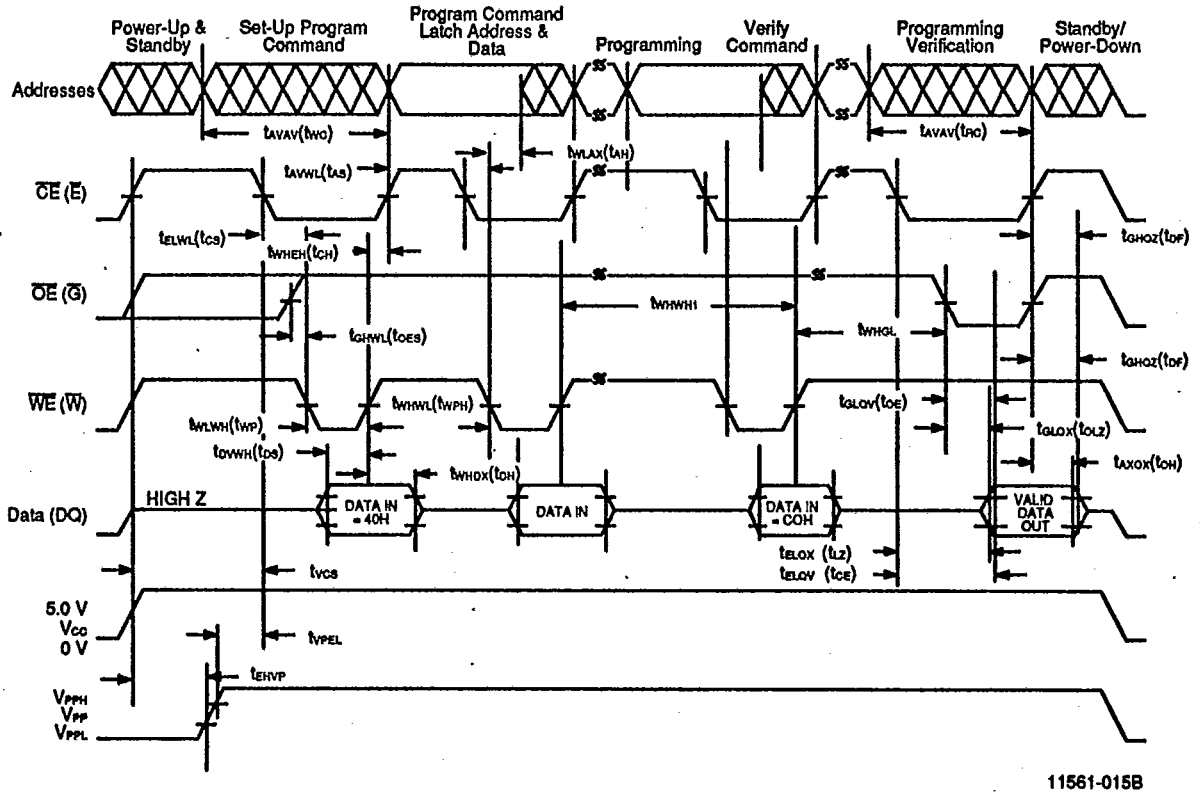
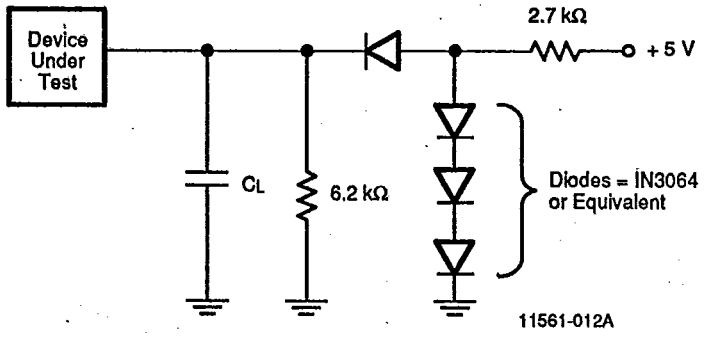


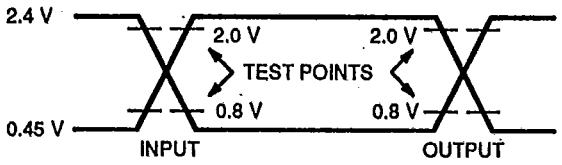
Figure 7. AC Waveforms for Programming Operations

SWITCHING TEST CIRCUIT



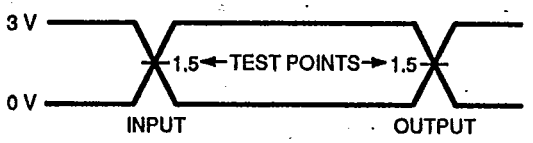
C_L = 100 pF including jig capacitance (30 pF for Am28F512-95)

SWITCHING TEST WAVEFORMS



All Devices Except Am28F512-95

AC Testing: Inputs are driven at 2.4 V for a logic "1" and 0.45 V for a logic "0". Input pulse rise and fall times are ≤ 10 ns.



For Am28F512-95

AC Testing: Inputs are driven at 3.0 V for a logic "1" and 0 V for a logic "0". Input pulse rise and fall times are ≤ 10 ns.

08007-003A

ERASE AND PROGRAMMING PERFORMANCE

Parameter	Limits Min.	Typ.	Max.	Unit	Comments
Chip Erase Time		0.5 (Note 1)	10	S	Excludes 00H programming prior to erasure
Chip Programming Time		1 (Note 1)	12	S	Excludes system-level overhead
Erase/Program Cycles					
Am28F512-95C4JC	10,000			Cycles	
Am28F512-95C3JC	1,000			Cycles	

Note:

1. 25°C, 12 V V_{PP}.

LATCHUP CHARACTERISTICS

	Min.	Max.
Input Voltage with respect to Vss on all pins except I/O pins (Including A_9 and V_{PP})	−1.0 V	13.5 V
Input Voltage with respect to Vss on all pins I/O pins	−1.0 V	Vcc + 1.0 V
Current	−100 mA	+100 mA
Includes all pins except Vcc. Test conditions: Vcc = 5.0 V, one pin at a time.		

Thin Small Outline Package

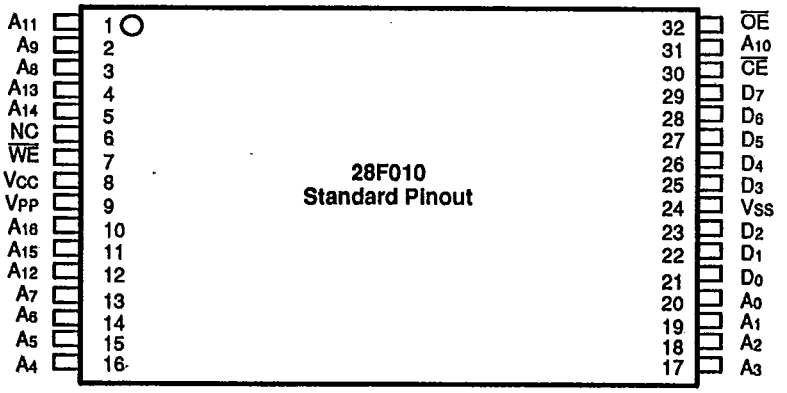
THIN SMALL OUTLINE PACKAGE (TSOP) DESCRIPTION

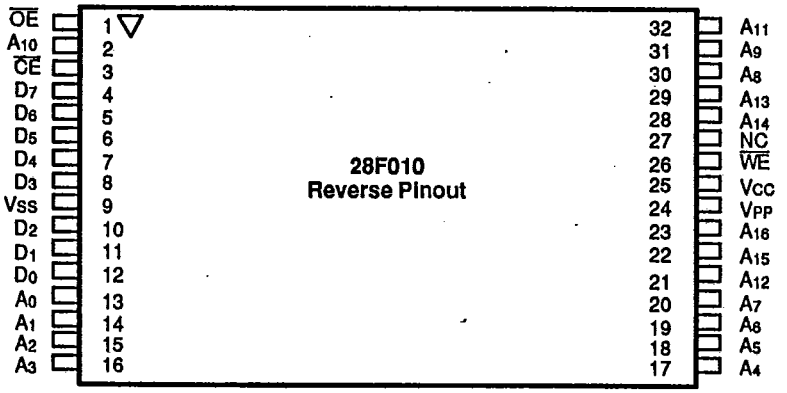
AMD presents the Thin Small Outline Package. The TSOP is the industry's leading edge plastic, surface mountable memory package today. System requirements for higher density and smaller form fit memory arrays are driving this package evolution. TSOP offers a form fit close to that of bare die yet provides the added benefit of being shipped from the factory completely tested, something not available with bare die. This increases system yield because there is no loss due to cleanroom assembly related defects and/or parametric failures. In addition to supporting Flash memory technology, AMD may also support EPROM (OTP/Express ROM™) technology in TSOP.

Primary Characteristics

- JEDEC/EIAJ standard dimensions and 32-pin pinout
- Standard and reverse pinout options
- Maximum package thickness of 1.27mm

This is AMD's initial offering in state of the art small form fit packaging. The 32-pin package is available in the 8 mm x 20 mm x 1.27 mm package outline. As densities increase, package leadcount will also.





28F010 128K x 8 Flash Memory in 32 Lead TSOP

Packaging Evolution

The continuing trend toward smaller systems and/or higher density memory arrays

Computers:	Desktop	Notebook	Palmtop
Disk drives:	3–1/2"	2–1/2"/Flash "Disk"	Flash "Disk"
Instrumentation:	Benchtop	Portable	Handheld

has led to a significant evolution in newer small form fit packaging. This trend is outlined below.

Package Type	Package Volume (cubic inchs)
PDIP (100 mil Pitch)	0.18
Slim DIP (100 mil Pitch)	0.09
ZIP (100 mil Pitch)	0.072
SOIC/SOJ (50 mil Pitch)	0.075
PLCC (50 mil Pitch)	0.045
TSOP (20 mil Pitch)	0.01

The TSOP is not only suited for standard printed circuit board and single in-line Memory Module (SIMM) applications, but is the package of choice in the exploding new growth area of solid state memory cards. These high volume applications will quickly prove the reliability of this new package.

TSOP packaging is well suited to high density, small form fit systems. This latest evolution offers significant packaging volume savings in comparison with the above alternatives. Increasingly, TSOP is being used in disk drive controller boards, notebook and palm top PCs, high density memory subsystems, and PCMCIA 68-pin standard memory cards. This is just the beginning.

An emerging market segment with explosive growth is the PCMCIA 68-pin memory card standard. The TSOP can be used to pack both sides of a memory board in order to increase the memory density available within a given space constraint. In addition, the TSOP packaged devices are tested to AMD's standard test flows. This allows AMD to guarantee the highest level of quality and long term reliability.

Minimal Space Requirements

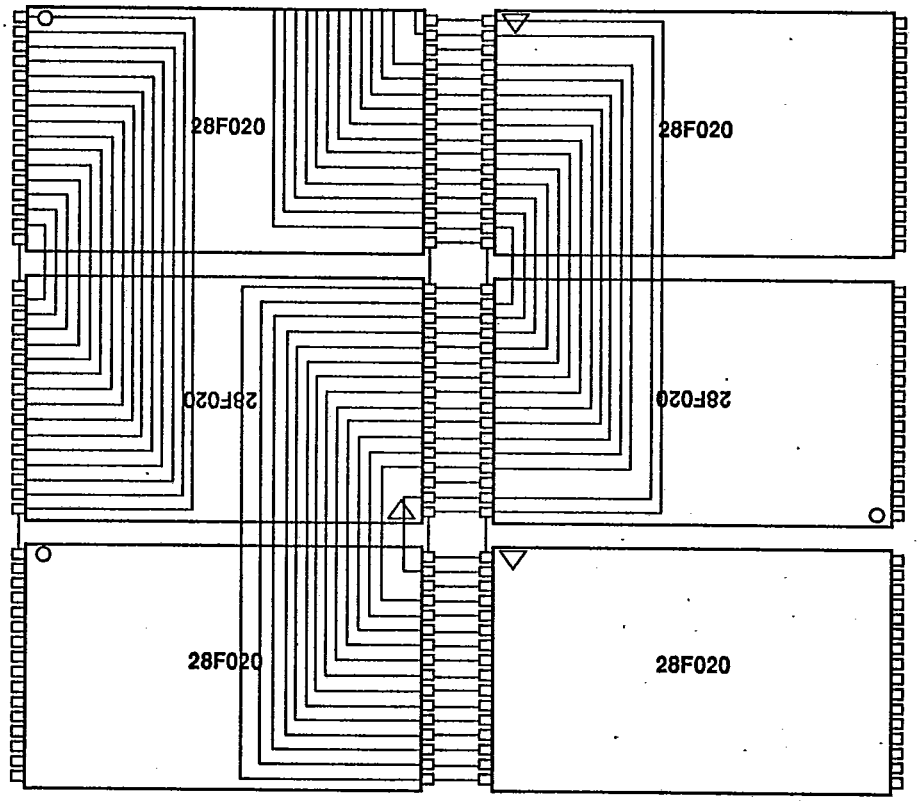
In addition to the TSOP's low height profile, maximum board space saving is achieved with the dual-in-line and standard/reverse pinouts. Board layers can be reduced because traces are routed under the two sides of the package that do not have leads. This allows packages to be mounted side by side and end to end. Packages can be mounted end to end because AMD offers both standard and mirror image reverse pinout packages (see figures below). All pins except chip enable pins can be connected in parallel. This is accomplished by using standard and reverse pinout packages in an alternating sequence as shown below.

HANDLING AND SHIPPING

Shipping Trays

TSOP devices will be shipped in JEDEC Standard dimension trays. JEDEC trays all have the same outside dimensions for easy stacking for use in manufacturing and storage. Trays are designed to prevent TSOP leads from touching any part of the holding tub.

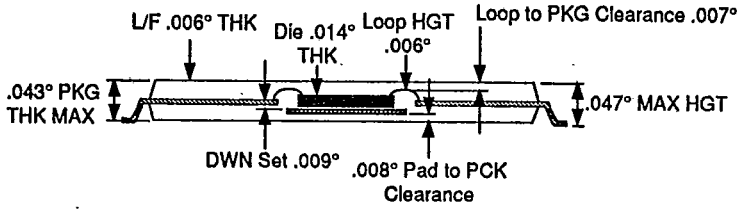
OPTIMAL BOARD LAYOUT WITH TSOP



○ = Pin 1 indicator for standard bend pinout

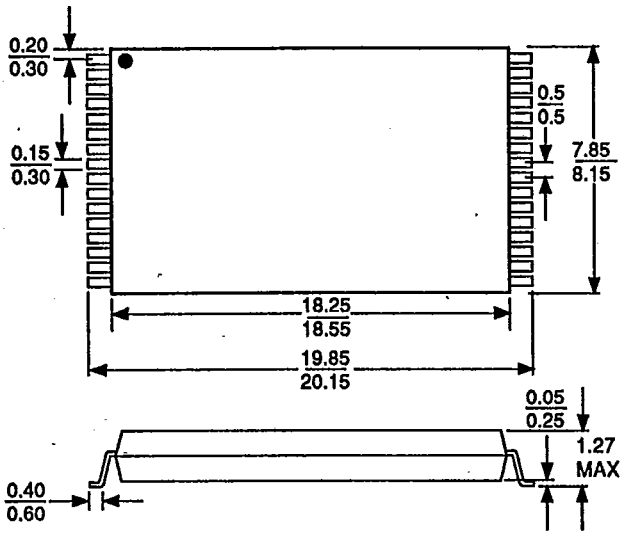
△ = Pin 1 indicator for reverse bend pinout

TSOP Cross-Section



PACKAGE DRAWING*

T-90-10



* For reference only. All measurments measured in millimeters. BSC is an ANSI standard for Basic Space Centering. Package in development.