SOT-1 Device
SONET STS-1 Overhead Terminator
TXC-03001B

DATA SHEET

FEATURES

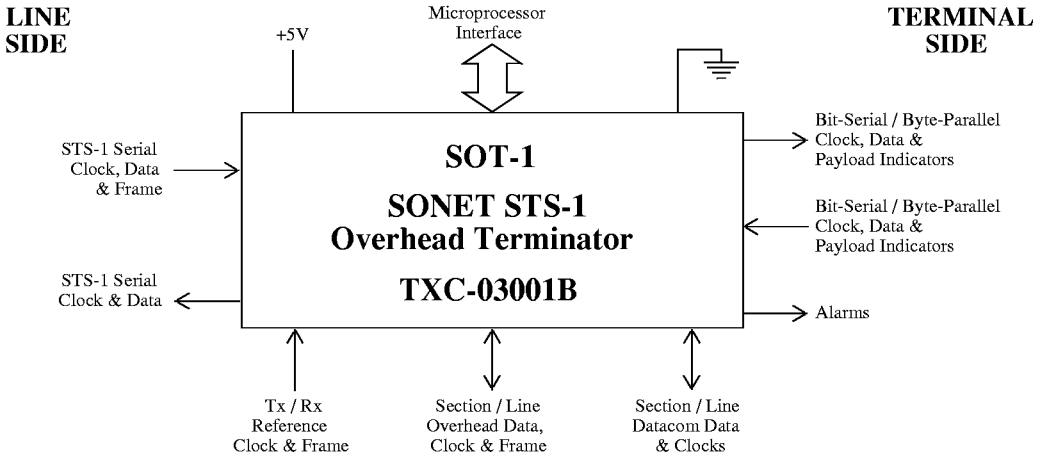
- Two operating modes: Enhanced features ("B") or backwards compatible with TXC-03001 version of the SOT-1 device ("A")
- Provides SONET interface to any type of payload
- Programmable STS-1 or STS-N modes
- Receive bit-serial STS-1 signal input to the Line Side using external reference frame pulse input for STS-N applications
- Transmit bit-serial STS-1 signal output from the Line Side using external reference frame pulse for outgoing phase synchronization
- Programmable: full STS-1 or SPE-only I/O on the Terminal Side
- Bit-serial, or 6.48 MB/s byte-parallel, I/O on the Terminal Side
- Optional AIS communication with peer SOT-1 (TXC-03001 or TXC-03001B), SOT-1E or SOT-3
- Interfaces to microprocessors with hierarchical scan and optional hardware interrupt on alarms
- SONET alarm processing and performance monitoring
- Meets 1995 ANSI and Bellcore Standards in Enhanced ("B") Mode:
  - T1.105
  - GR-253-CORE
- Single +5 volt, ± 5 % power supply
- 84-pin plastic leaded chip carrier package

DESCRIPTION

The SOT-1 SONET/STS-1 Overhead Terminator performs Section, Line and Path Overhead processing for STS-1 SONET signals. This versatile device can be used anywhere in a SONET network where STS-1 signals are in use, e.g., repeaters, and Line or Path termination points. Interfaces are provided for both Section and Line Orderwire and Datacom channels. Further, control bits in the Memory Map enable the SOT-1 to perform loopback and serial or parallel I/O. Line Side and Terminal Side clock rates can differ. The Receive and Transmit Pointers are recalculated as necessary to compensate for clock differences. All overhead bytes are stored in on-chip RAM. New overhead bytes can be substituted from RAM to either the Terminal or Line Side, depending on the application. The SOT-1 also provides alarm detection and AIS generation, as well as software and hardware interrupts in the event of errors.

APPLICATIONS

- Replacement for "A" version of SOT-1 (TXC-03001)
- SONET W-DCS/B-DCS
- High speed data communication
- Payload extraction, introduction into STS-1
- STS-N Multiplexer
- SONET test sets



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* Please note that TranSwitch provides documentation for all of its products. Most product documentation is available from the TranSwitch Internet Web site at www.transwitch.com. Customers who are using a TranSwitch Product, or planning to do so, should register with the TranSwitch Marketing Department to receive relevant updated and supplemental documentation as it is issued. They should also contact the Applications Engineering Department to ensure that they are provided with the latest available information about the product, especially before undertaking development of new designs incorporating the product.

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SONET TUTORIAL

A primary goal in developing the SONET (Synchronous Optical NETwork) format was to define a synchronous, optical hierarchy with sufficient flexibility to carry many different payloads. This has been accomplished by defining a basic signal of 51.84 Mb/s and a byte interleaved multiplex scheme that results in a family of standard rates and formats defined at a rate of N times 51.84 Mb/s, where N is an integer. Since some signals that must be transported are greater than the basic rate, a technique of linking several basic rate signals together to form a transport signal of varying capacity has also been defined. There are three major differences between the SONET Hierarchy and the North American Digital Hierarchy (NADH)[1].

1. SONET is synchronous. All SONET tributaries in a SONET network must be traceable to one or more Stratum 1 synchronization sources.
   NADH is asynchronous. The tributaries need not be synchronized.
2. SONET is a harmonic multiplexing structure. All higher rate SONET signals are integer multiples of a base rate. Lower order SONET tributaries are byte interleaved to form the higher order SONET signal.
   NADH is hierarchical. Higher order multiplexing is accomplished with bit stuffing to accommodate speed differences in lower order tributaries.
3. SONET overhead (Framing, Performance Monitoring, Alarms, etc.) and payload are distinct entities. In a SONET signal the payload bits do not occupy a fixed position in relation to the transport overhead bits. A pointer mechanism is used to identify the start of the payload.
   NADH overhead bits and payload bits have a fixed, unvarying relationship to each other.

The Basic modular signal (at 51.84 Mb/s) is called the Synchronous Transport Signal level One (STS-1). The optical counterpart is the Optical Carrier level One (OC-1), which is the result of direct optical conversion of the STS-1 signal. Higher level signals are denoted by STS-N and OC-N, where N is an Integer. At present the standardized values of N are: 1, 3, 12, 24, 48 and 192. These values provide standardized multiplexing rates for SONET systems at 51.84 Mb/s, 155.52 Mb/s, 622.08 Mb/s, 1.24416 Gb/s, 2.48832 Gb/s and 9.95328 Gb/s, respectively.

FORMATS

There are four basic formats upon which the SONET Hierarchy is built.

STS-1 Structure

The basic SONET format is the 51.84 Mb/s signal designated STS-1. It consists of 810 eight bit bytes arranged in a matrix of nine rows each of which has 90 columns as shown in Figure 1. This nine by 90 arrangement is referred to as a SONET Frame. It repeats every 125 µs. The first three columns consist of the Transport Overhead (TOH). The remaining 87 columns are referred to as the Synchronous Payload Envelope (SPE). It is this portion of a SONET signal that is allowed to "float." Within the TOH is a pointer that identifies the starting position of the SPE with respect to the TOH Bytes in the Frame. The first column of the SPE is the Path Overhead (POH). The remaining 86 columns contain the actual payload information whose capacity is approximately 50 Mb/s.

1. The North American Digital Hierarchy is described in ANSI T1.107. The ITU term "PDH" (Plesiochronous Digital Hierarchy) is sometimes used to generically refer to an asynchronous multiplexing structure.

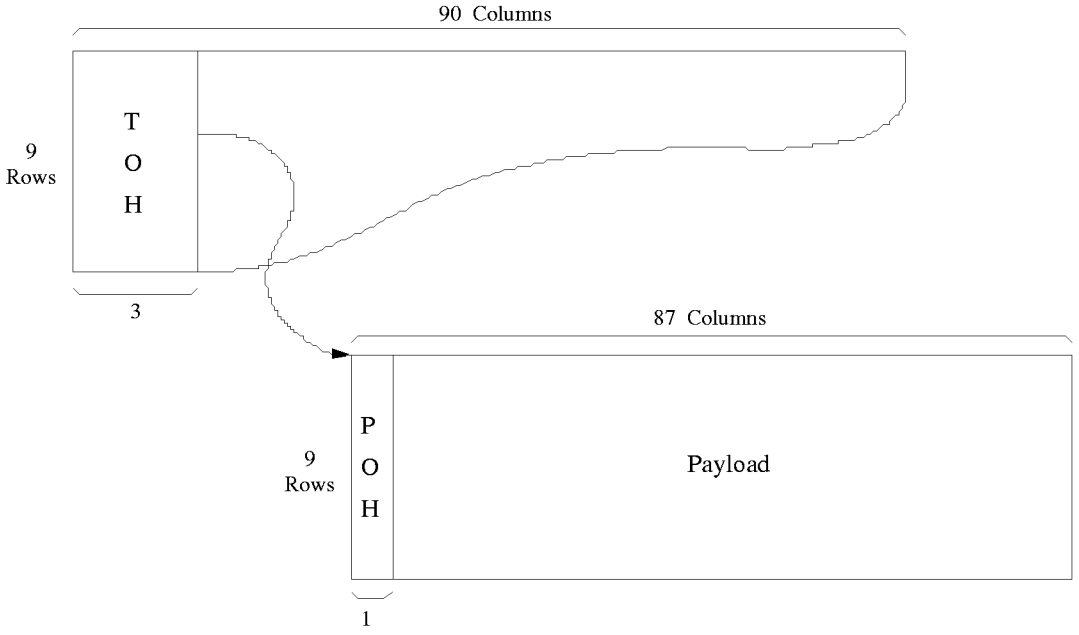


Figure 1. STS-1 Format

STS-N Structure

STS-N formats are higher order multiplex structures which allow the transportation of N number of ≈50 Mb/s payloads (e.g., STS-3 transports three ≈50 Mb/s payloads). As shown in Figure 2, the Frame consists of nine rows and N x 90 columns. The TOH is N x 3 columns wide. There are N number of nine by 87 SPEs each of which contains one column of POH. The TOH contains N number of pointers: one for each of the SPEs.

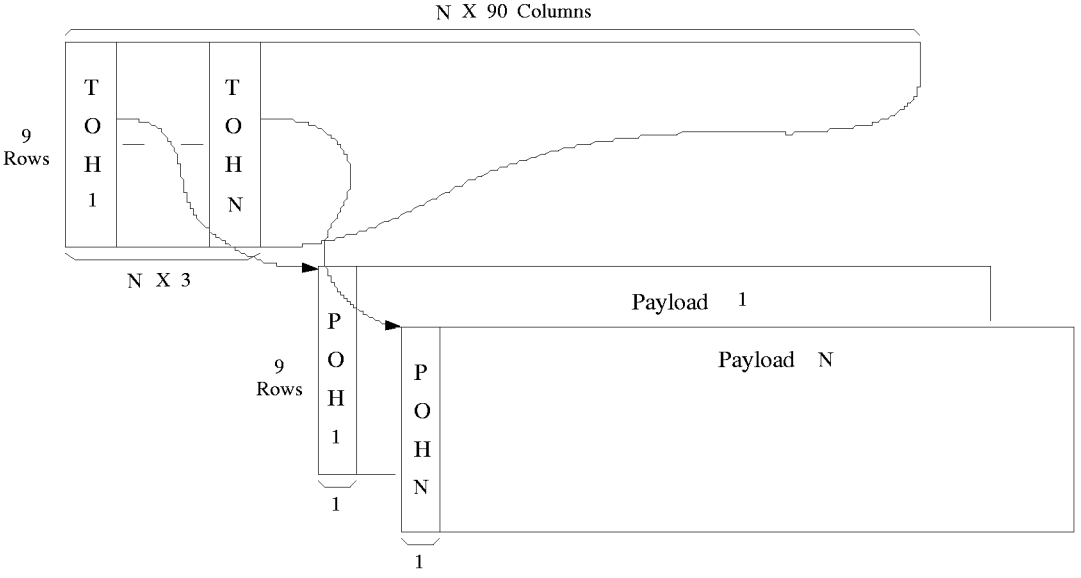


Figure 2. STS-N Format

STS-Nc Structure

As mentioned earlier, SONET contains a mechanism by which payloads that are larger than ≈50 Mb/s can be carried. This mechanism is called Concatenation and is indicated by the designation Nc. STS-Nc formats are higher order structures which allow the transportation of a single payload whose bandwidth is approximately N x 50 Mb/s (e.g., STS-3c transports one 149.76 Mb/s payload). The STS-Nc format is shown in Figure 3. As with the STS-N format, the Frame consists of nine rows and N x 90 columns. The TOH is N x 3 columns wide. There is a single SPE which is nine rows by N x 87 columns. The first SPE column is used for POH. The TOH contains one pointer which identifies the start of the SPE in the Frame.

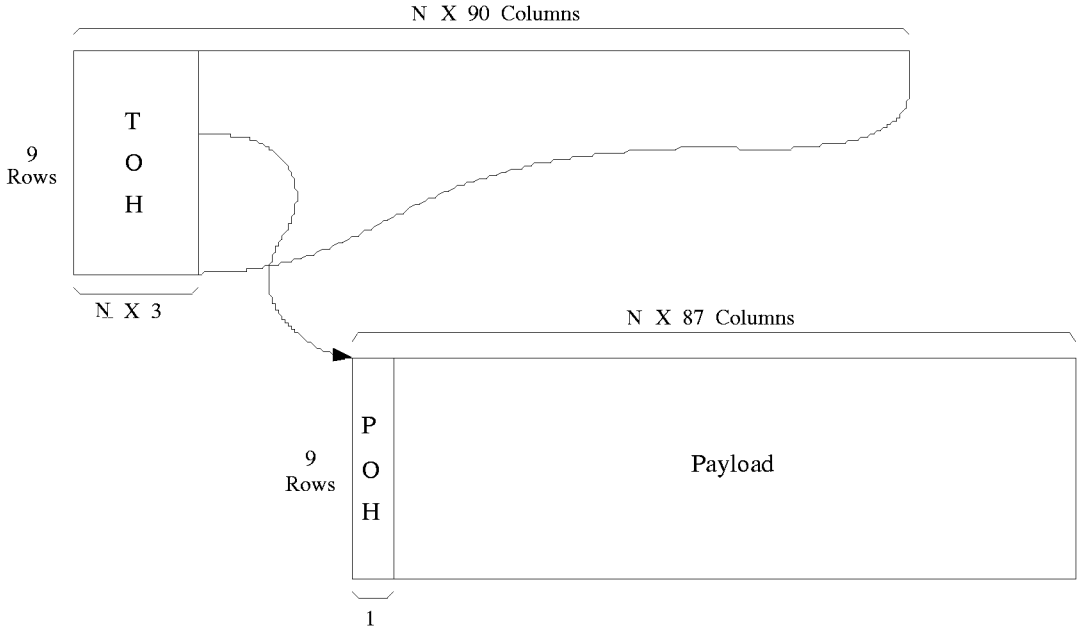


Figure 3. STS-Nc Format

Virtual Tributary Structures

The Virtual Tributary (VT) is a structure designed for transport and switching of sub-STS-1 payloads (payloads less than DS3). As shown in Figure 4, it consists of a VT Pointer, which indicates the start of the VT SPE. The VT SPE is composed of VT POH and Payload. The VT Pointer provides for flexible and dynamic alignment of the VT SPE within the VT, independent of other VTs in the STS-1 SPE.

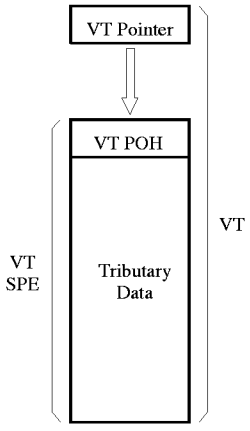


Figure 4. VTn Format

There are four sizes of VT: the VT1.5 (≈1.7 Mb/s), the VT2 (≈2.3 Mb/s), the VT3 (≈3.5 Mb/s) and the VT6 (≈6.9 Mb/s). These are shown in Figure 5. In the nine row format of the STS-1 SPE they occupy three columns, four columns, six columns and twelve columns, respectively. VTs may only be carried in an STS-1 SPE. STS-Nc SPEs cannot be subrated into VTs. For example, to carry 84 DS1s in SONET an STS-3 format must be used with each STS-1 SPE organized as 28 VT1.5s.

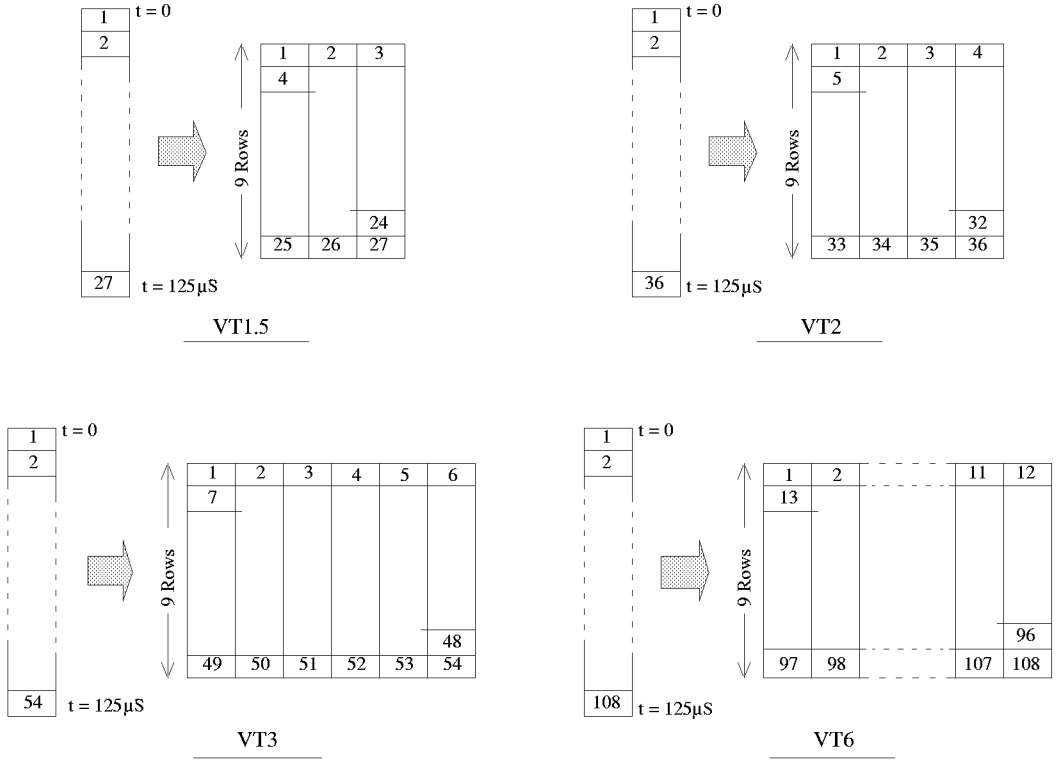


Figure 5. VT Sizes

Four consecutive 125 µs frames of the STS-1 SPE are organized into a 500 µs Superframe, the phase of which is indicated by a Multiframe Indicator Byte (H4) in the STS-1 POH. This defines a 500 µs structure for each of the VTs, called the VT Superframe, which is shown in Figure 6. The VT Superframe contains the VT Pointer and the VT SPE. The VT Pointer occupies four bytes designated V1, V2, V3 and V4 and the remaining bytes define the VT SPE, the capacity of which is different for each VT type. The placement of the V1 through V4 Bytes is such that they will appear in Byte 1 (shown in Figure 5) of the VT regardless of the VT size. Since the SOT-1 does not process VTs there will be no further discussion of VT characteristics.

OVERHEAD

The overhead and transport functions in SONET have been broken into layers to promote understanding and structure. In order of increasing complexity the layers are: Physical Medium, Section, Line and Path. When viewed with a bottom-up approach, each layer builds upon the services provided by the lower layer. The Physical Medium Layer provides transmission at a standard bit rate. The Section layer provides framing, scrambling and Section maintenance for the bits being transmitted. The Line layer provides Line maintenance and protection as well as multiplexing of the STS SPEs. The Path layer provides the payload mapping function and Path maintenance. Note than all layers can be implemented in a single piece of equipment or they can be broken into multiple pieces of equipment.

Physical Medium Layer

The Physical Medium Layer deals with transport of the bits across the transmission medium. No overhead is associated with this layer. Its main function is the conversion between signals internal to a Network Element (NE) and signals suitable for transmission. Issues dealt with at this layer include pulse shape, power levels, and (for optical equipment) wavelength. Electro-optical units communicate at this level.

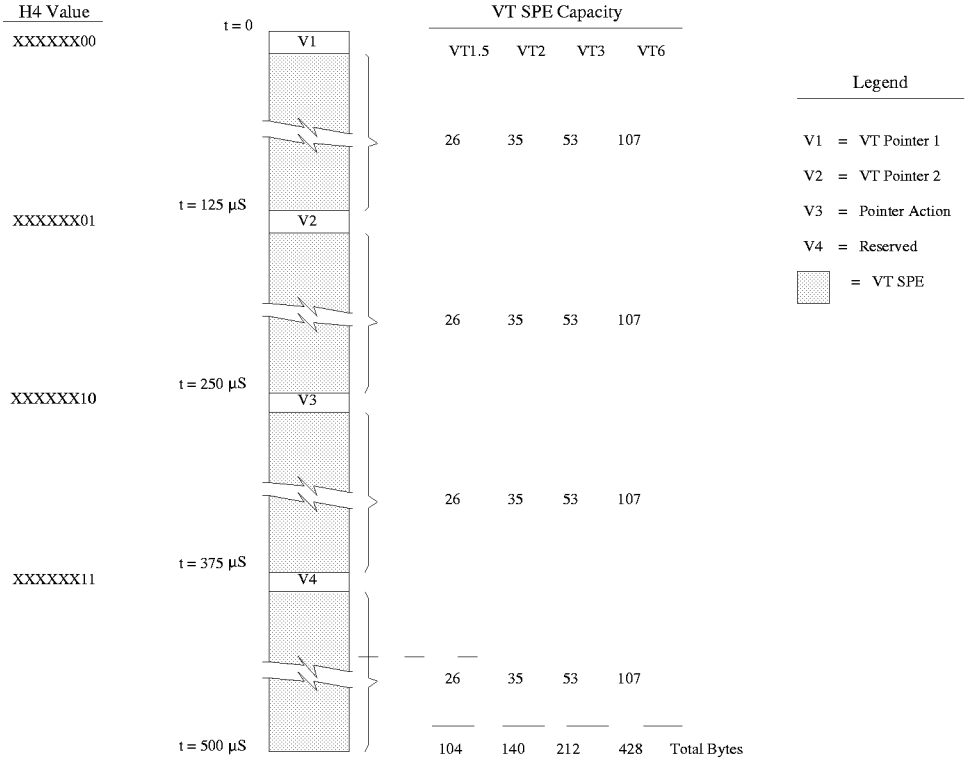


Figure 6. VT Superframe

Section Layer

The Section Layer deals with the reliable transport of an STS-N frame across the physical medium. Functions within this layer include framing, scrambling, error monitoring, data communications, and a local orderwire. Section and Physical Medium Layers can be utilized in some equipment without any higher order layers. A regenerator would operate in this manner.

Line Layer

The Line Layer deals with the reliable transport of Path Layer payload and its overhead across the Section and Physical Medium Layers. Overhead added here is accessed at points where SPEs are multiplexed together. The functions of this layer are to provide synchronization and multiplexing for the Path Layer, as well as error monitoring, data communications, orderwire, and protection signaling for Line protection switching. An example of equipment that communicates at this level is an OC-M to OC-N multiplexer *where*: M < N.

Path Layer

The Path Layer deals with the reliable transport of services over the Line, Section and Physical Medium Layers. Example of such services are DS1s, DS3s and ATM signals. The main function of this layer is to map the services into the format required by the Line Layer. In addition, this layer provides error monitoring and connectivity checks. The overhead defined for this layer is read, interpreted, and modified by equipment that creates or disassembles the SONET payload for a given service. POH may be monitored but not modified by Line processing equipment. There is an exception to this last statement. Line processing elements that have implemented Tandem Connection Maintenance (see ANSI T1.105.05) may modify certain Path Layer bytes. However, the original Path Layer information must be restored at the termination point of the Tandem Connection function. An example of equipment that communicates at the Path level is a DS3 to STS-1 mapping circuit.

Overhead Termination

Any NE that originates or terminates an overhead layer is considered to be a terminating entity for that layer. This defines three types of NEs:

1. Section Terminating Equipment (STE)
2. Line Terminating Equipment (LTE)
3. Path Terminating Equipment (PTE)

Peer communications occur between pieces of equipment that terminate a particular layer. Examples of STE, LTE, and PTE Equipment and the layers processed by each entity are shown in Figure 7. There are four multiplexers and two regenerator (repeaters) in this example. The two multiplexers on the left and the one on the right are multiplexing and de-multiplexing DS3s into and out of a SONET signal. The multiplexer in the middle represents a higher order unit which is multiplexing and de-multiplexing lower order SONET signals to and from a higher order signal. Since the Physical Medium Layer does not have any overhead associated with it, it will not be discussed. By definition, all SONET NEs are Section Terminating and a regenerator is only STE. There are five Section Layer peer communication links. There are three Line Layer peer communication links: one from each of the left most multiplexers to the middle multiplexer, and one between the middle multiplexer and the multiplexer on the right. Finally, there are two Path Layer peer communication links. These exist between the multiplexers on the left and the multiplexer on the right.

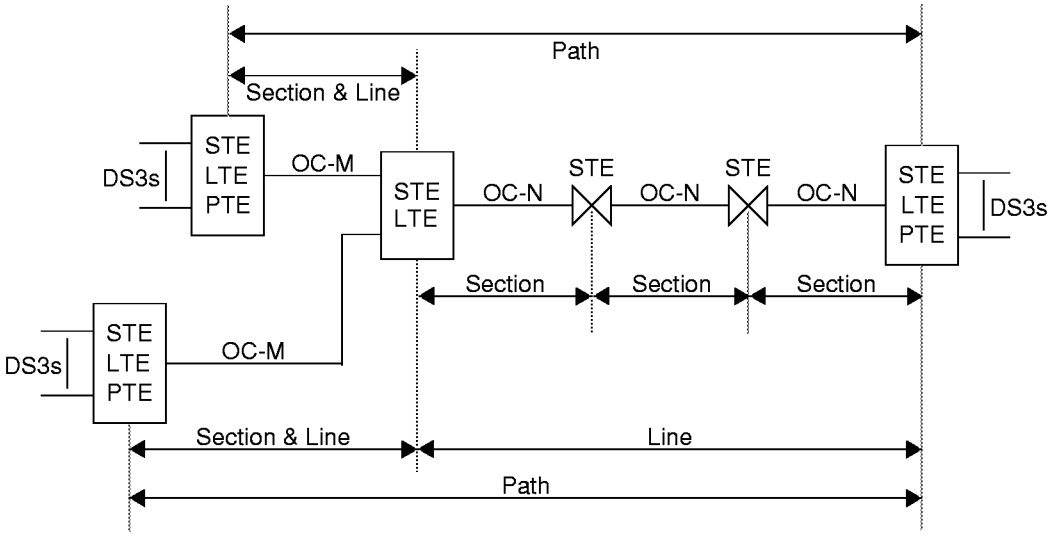


Figure 7. Overhead Utilization

Overhead Locations

The functions of the Section and Line Layers have been combined into a structure of 27 bytes called Transport Overhead (TOH), which occupies the first three columns of an STS-1 Frame. The first three rows are Section Overhead (SOH). The last six rows are Line Overhead (LOH). This is shown in Figure 8. In STS-N and Nc frames there are 3 x N TOH columns. Figures 9 and 10 represent STS-N and Nc formats using STS-3 and 3c as an example. The byte-interleaved characteristic of SONET can be seen in these figures. Some of the transport overhead fields in STS-1 numbers two through N are the same as for STS-1 number one and some are not. In the STS-3 Format there are three H1 and H2 Bytes. Each H1, H2 combination is a pointer for one of the three payloads that is being transported. The STS-3c format is carrying one ≈150 Mb/s payload. There is only one pointer. The H1 and H2 bytes in the STS-1 number one position are the pointer. The two remaining H1 and H2 byte pairs in STS-1 positions two and three are Concatenation Indicators.

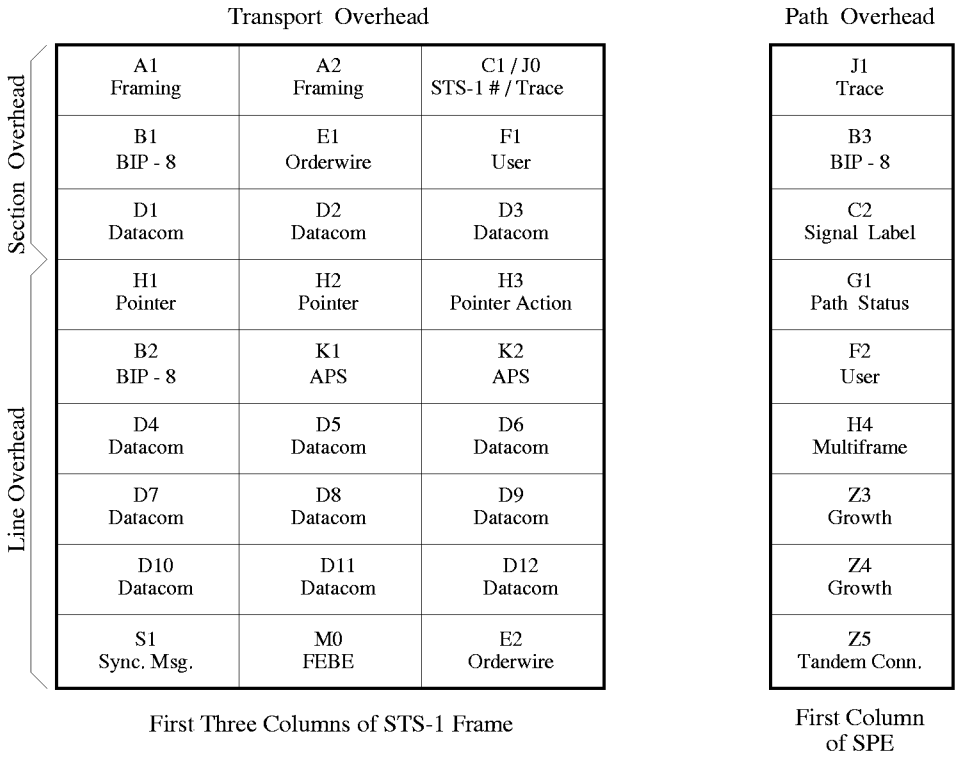


Figure 8. STS-1 Overhead

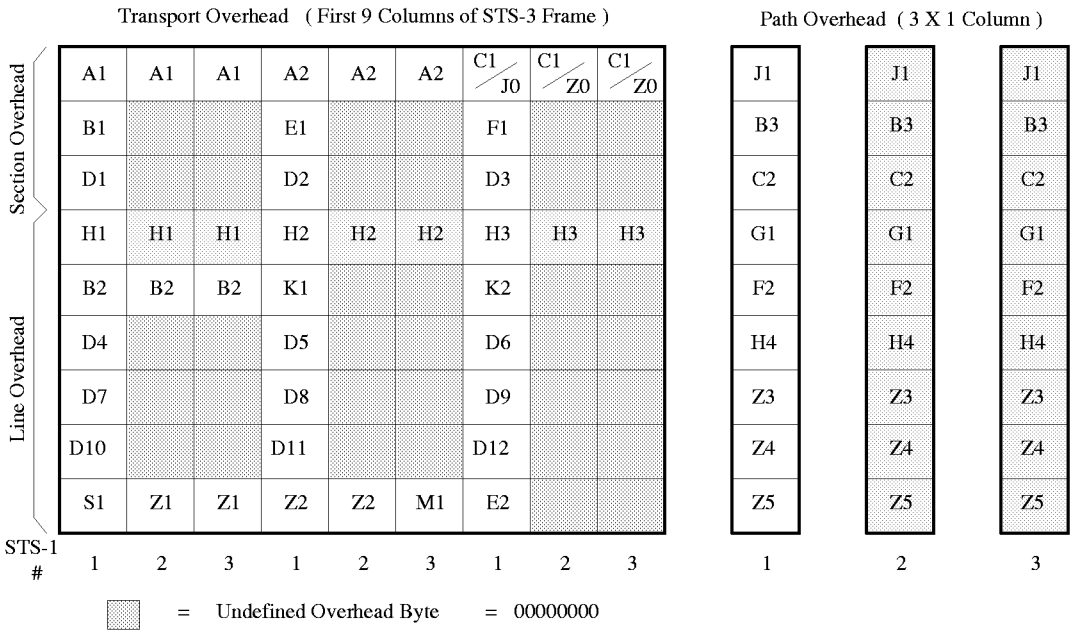


Figure 9. STS-3 Overhead

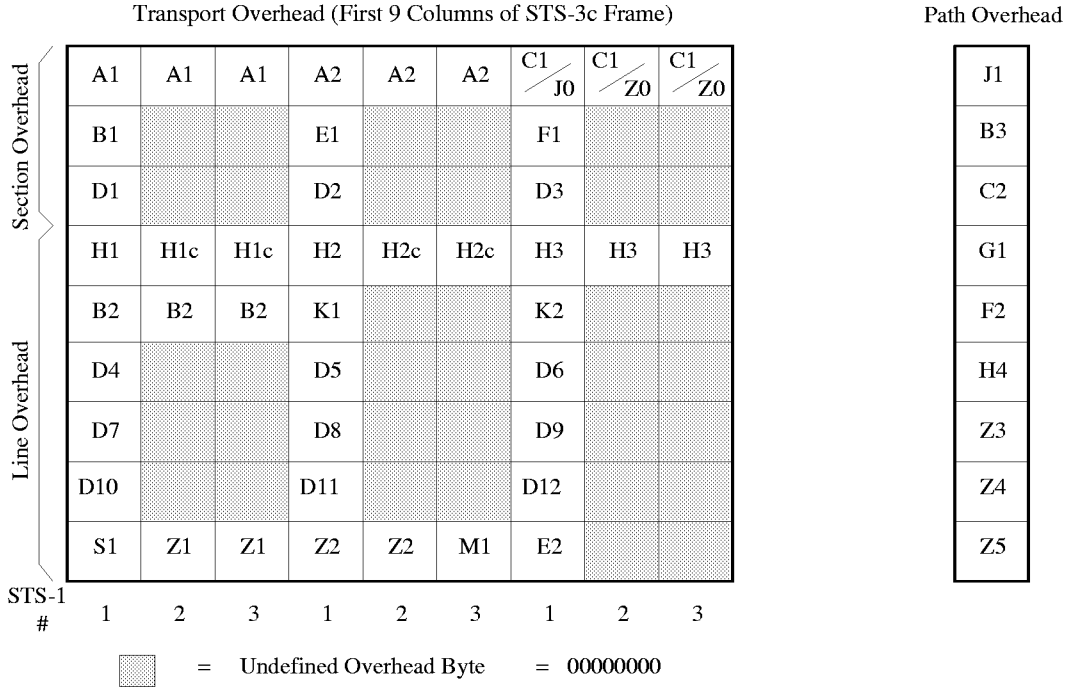


Figure 10. STS-3c Overhead

The Path Layer functions are assigned to the nine bytes occupying the first column of the STS SPE. The distinction between TOH and POH is made so that transmission equipment can be specified without regard to the information structure that is being transported. The STS-1 and STS-3c formats have only one POH field. In the STS-3 format there are three POH fields, one for each payload. The lightly shaded cells in Figure 9 represent Pointer and POH bytes associated with STS-1 numbers two and three.

Section Overhead Definitions - SOH

The definitions for the Section Overhead Bytes are given below.

A1, A2: Framing - Two bytes are allocated in each STS-1 for Framing. The Pattern is A1 = F6[H] and A2 = 28[H]. these bytes are provided in all STS-1 portions of an STS-N/Nc signal.

C1: STS-1 I.D. - In earlier editions of the SONET standard, one byte labeled C1 in each STS-1 was allocated for an STS-1 identification function. These bytes are no longer used for this purpose. Instead, this overhead is currently allocated for Section Trace and Section Growth (defined below). However, to ensure interworking with older equipment, these bytes must be capable of transmitting and receiving the STS-1 Identification Codes. When used in this manner the following definition will apply. The C1 byte in Each STS-1 shall be set to a binary number corresponding to its order of appearance in the byte interleaved STS-N frame where 01[H] is the number for the first STS-1 appearing in the frame. The C1 Byte is defined for all STS-1s in an STS-N/Nc signal.

J0: Section Trace - One byte is allocated to be used for a Section Trace function. This byte is defined only for STS-1 number one in an STS-N/Nc signal. J0 (formerly C1 of STS-1 number one) is used to repetitively transmit a one-byte fixed length string so that a receiving terminal can verify its continued connection to the intended transmitter. Any value in the range of 00[H] through FF[H] may be placed in this byte. When the Section Trace function is not supported or if no value has been assigned then 01[H] shall be transmitted.

Z0: Section Growth - One byte is defined in each STS-1 for future growth except for STS-1 number one (defined as J0). For interworking with older equipment, the Z0 bytes shall be capable of being set consistent with the C1 definition described above.

B1: Section BIP-8 - One byte is allocated for a Section Error Monitoring function. This function is a bit interleaved parity 8 code using even parity. The Section BIP-8 is calculated over all bits of the previous STS-N/Nc frame after scrambling. The computed BIP-8 is placed in the B1 Byte before scrambling. This byte is defined only for STS-1 number one of an STS-N/Nc signal.

E1: Orderwire - One byte is allocated to be used as a Section Orderwire. This is a local orderwire channel reserved for voice communications between STEs, hubs and remote NEs. It is only defined for STS-1 number one.

F1: Section User Channel - One byte is set aside for the users purpose. This byte is passed from Section to Section within a transmission system and is readable, writable or both at each STE in that system. The use of this function is optional. The F1 byte is defined only for STS-1 number one in an STS-N/Nc signal.

D1-D3: Section Datacom Channel - Three bytes are allocated for a Section Data Communications Channel and are considered as a single 192 kb/s message-based channel between STEs. The messaging protocols used are defined in ANSI T1.105.04. These bytes are defined only for STS-1 number one in an STS-N/Nc signal.

Line Overhead Definitions - LOH

The definitions for the Line Overhead Bytes are given below.

H1, H2: Pointer - Two bytes are allocated to a pointer that indicates the offset in bytes between the pointer and the first byte of the STS SPE. It allows alignment of the STS-1 TOHs in an STS-N/Nc signal and to perform frequency justification. In an STS-Nc signal the actual pointer is in the first set of H1 and H2 bytes. H1 and H2 bytes occupying STS-1 positions two through N carry a Concatenation Indicator, *where*: H1c = 93[H] and H2c = FF[H]. These bytes are required in all STS-1 portions of an STS-N/Nc signal.

H3: Pointer Action - The Pointer Action Byte is allocated for frequency justification purposes. Depending on the pointer value, this byte is used to adjust the fill of input buffers. In the event of a negative justification, it carries valid information. This byte is required in each STS-1 portion of an STS-N/Nc signal.

B2: Line BIP-8 - One byte is allocated in each STS-1 for a Line Error Monitoring function. This function is a bit-interleaved parity 8 code using even parity. The Line BIP-8 is calculated over all bits of the Line Overhead and STS SPE of the previous frame before scrambling. The computed BIP-8 is placed in the B2 Byte before scrambling. This byte is defined for all STS-1s of an STS-N/Nc signal. The N B2 Bytes in an STS-N/Nc are intended to form a single error monitoring function capable of measuring error rate up to 10^{-3} independent of the value of N. It can be thought of as either: (1) N BIP-8 functions each processing 1/N of the signal or (2) a single BIP-(Nx8) processing all of the information. The errors accumulated are to be accumulated into a single error count.

K1, K2: APS Channel - Two bytes are allocated for Automatic Protection Switching (APS) signaling between LTEs. The signaling protocols used are defined in ANSI T1.105.01. These bytes are defined only for STS-1 number one in an STS-N/Nc signal.

D4-D12: Line Datacom Channel - Nine bytes are allocated for a Line Data Communications Channel and are considered as a single 576 kb/s message based channel between LTEs. The messaging protocols used are defined in ANSI T1.105.04. These bytes are defined only for STS-1 number one in an STS-N/Nc signal.

S1: Synchronization Messaging - One byte is allocated for transporting synchronization status messages. Currently, only Bits 5 through 8 are defined. Bits 1 through 4 are reserved for future use. This byte is defined only in STS-1 number one in an STS-N/Nc signal.

M0: STS-1 Line FEBE - In a STS-1 signal one byte is allocated for a Line Far End Block Error (FEBE) function. Currently only Bits 5 through 8 are used. These bits are used to convey the count of errors detected by the B2 Byte. This count has nine legal values, i.e., zero through eight. The remaining seven values are interpreted as zero errors. Bits 1 through 4 are reserved for future use.

M1: STS-N/Nc Line FEBE - In a signal at or above the STS-3/3c level, one byte is allocated for a Line Far End Block Error (FEBE) function. The M1 Byte is located in the third STS-1 in an STS-N/Nc signal. The entire byte is used to convey a count of errors detected in B2 Bytes. This count has (8 x N) + 1 legal values, i.e., zero through (8 x N) errors. For rates below STS-48/48c, the remaining possible 255-(8 x N) values are interpreted as zero errors. At rates at and above STS-48/48c, if greater than 255 errors are detected the Line FEBE shall relay a value of 255 errors.

Z1: Growth - In a signal at or above the STS-3/3c level, and less than the STS-192/192c rate, one byte is reserved in STS-1 numbers two through N of the STS-N/Nc signal for future growth. At rates greater than or equal to STS-192/192c, Z1 is only defined for STS-1 numbers two through 48.

Z2: Growth - In a signal at or above the STS-3/3c level, and at or less than the STS-192/192c rate, one byte is reserved in all STS-1s except for STS-1 number three of the STS-N/Nc signal for future growth. At rates greater than or equal to STS-192/192c, Z2 is only defined for STS-1 numbers one, two, and four through 48.

E2: Order wire - One byte is allocated to be used as a Line Orderwire. This is an express orderwire channel reserved for voice communications between LTEs. It is only defined for STS-1 number one.

Path Overhead Definitions - POH

Path Overhead is assigned to a payload by a source device (DS3 mapping circuit, DS1 to STS-1 mux, etc.) and remains with the payload until demultiplexed by the sink device. Intermediate LTEs may be required to monitor these bytes. POH functions are divided into four classifications:

Class A Payload Independent Functions - These functions have a standard format and coding and are required for all PTEs.

Class B Mapping Dependent Functions - These functions have a standard format and coding that are specific to the type of payload. They are needed for more than one type of payload but not necessarily all payloads. These functions are processed by the appropriate PTEs.

Class C Application Specific Functions - The format and coding for these functions may not be defined in the SONET Standards. These functions are processed by the appropriate PTEs.

Class D Undefined Overhead Functions - These overhead bytes are reserved for future use.

The definitions for the Path Overhead Bytes are given below:

J1: Path Trace: Class A - One byte is used to repetitively transmit a 64-byte fixed length string so that a sink device can verify its continued connection to the intended source device. The content of the message is not constrained by the SONET Standards. However, it is suggested that a message consisting of eight-bit ASCII characters, padded with NULL Characters, and terminated with CR and LF (total length 64 bytes) would be appropriate. If no message is designated then 00[H] is to be transmitted.

B3: Path BIP-8, Class A - One byte is allocated for a Path Error Monitoring function. This function is a bit interleaved parity 8 code using even parity. The Path BIP-8 is calculated over all bits of the previous STS SPE before scrambling. The computed BIP-8 is placed in the B3 Byte before scrambling.

C2: Path Signal Label: Class A/B - One byte is allocated to identify the construction and content of the SPE and for a Path Payload Defect Indicator (PDI-P). The Signal Label portion is a class A function. PDI-P is class B.

G1: Path Status: Class A - One byte is allocated to convey back to the Source PTE the Sink PTE status and performance. Bits 1 through 4 are a Path FEBE. These bits are used to convey the count of errors detected by the B3 Byte. This count has nine legal values i.e., zero through eight. The remaining seven values are interpreted as zero errors. Bits 5, 6 and 7 used for a Path Remote Defect Indication (RDI-P). Bit 8 is reserved for future use.

F2: Path User Channel: Class C - One byte is allocated for user communications purposes between PTEs.

H4: Multiframe Indicator: Class B - This byte provides a generalized multiframe indicator for payloads. Currently, it is only used with VT structured payloads.

Z3, Z4: Growth: Class D - Two bytes are reserved for future use.

Z5: Tandem Connection Maintenance / Path Data Channel: Class C - One byte is allocated to support Tandem Connection Maintenance (TCM) and a Path Data Channel. Bits 1 through 4 are reserved for TCM functions. Bits 5 through 8 form a 32 kb/s data channel that uses the LAPD protocol. The Path Data channel is used in TCM applications and is also available for communications between PTEs. However, TCM messages have priority. Since TCM terminating entities are not required to perform store and forward or Layer 2 termination for non TCM messages, some or all of the preempted PTE to PTE messages may be lost and require re-transmission.

POINTERS

Pointers are defined in SONET at the STS-N and VT Levels. The STS-1 Payload Pointer provides a mechanism to allow the flexible and dynamic alignment of the STS-1 SPE within the SONET Transport Frame. Dynamic alignment means that the STS-1 SPE is allowed to float within the Transport frame. Thus the pointer is able to accommodate differences not only in the phases of the STS-1 SPE and the TOH, but in the frame rates as well. As is shown in Figure 11, the STS-1 SPE will usually start in one frame and end in the following frame.

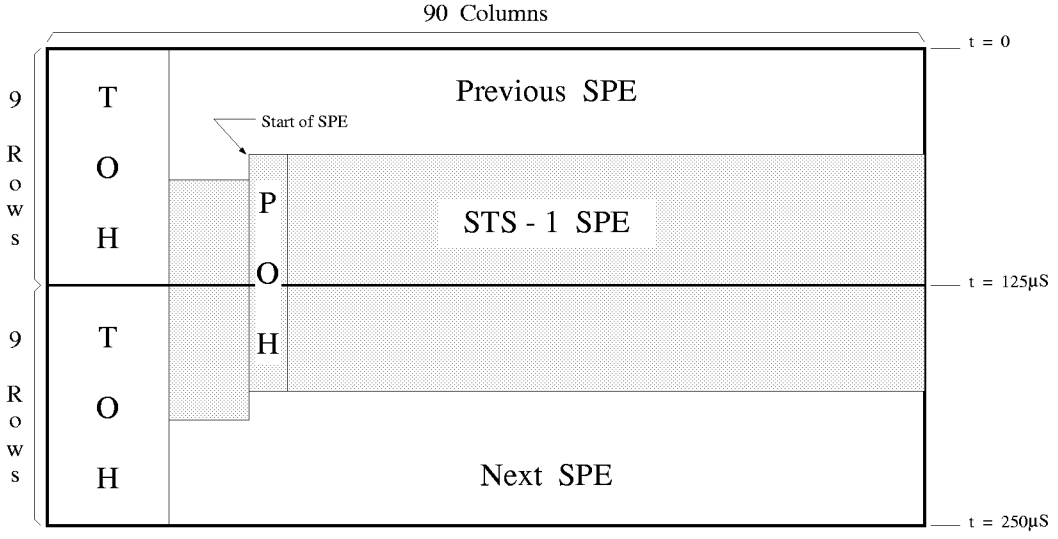
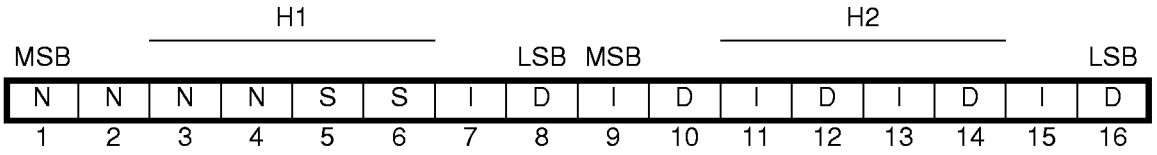


Figure 11. STS-1 Frame

The Pointer Bytes (H1 and H2) can be viewed as one 16 bit word as shown below. The last ten bits (7-16) of the Pointer Word carry the pointer value. This value is a binary number with a range of 0 to 782 that indicates the offset between the Pointer Bytes and the first byte of the SPE (J1). The TOH Bytes are not counted in the offset. For example, a value of "0" indicates that the SPE starts in the byte position immediately following the H3 Byte. The last column of this row is indicated by a pointer value of "86". A value of "87" specifies that the SPE starts at the byte position immediately following the K2 byte. A value of "522" would position the start of the SPE in the byte position immediately following the C1/J0 Byte. The two S bits are not used in STS-1 Pointers and are set to "00".



Frequency Justification

If there is a frequency offset between the frame rate of the TOH and that of the STS-1 SPE, then the pointer value will be incremented or decremented, as needed, accompanied by a corresponding positive or negative stuff byte. Consecutive pointer operations must be separated by at least three frames in which the pointer value remains constant.

If the frame rate of the SPE is too slow with respect to the TOH, then the alignment of the envelope is periodically slipped back in time and the pointer is incremented by one. This is shown in Figure 12. The operation is indicated by inverting Bits 7, 9, 11, 13 and 15 (I Bits) of the Pointer Word. A positive stuff byte appears immediately after the H3 Byte in the frame containing the inverted I Bits. Subsequent pointers contain the new offset.

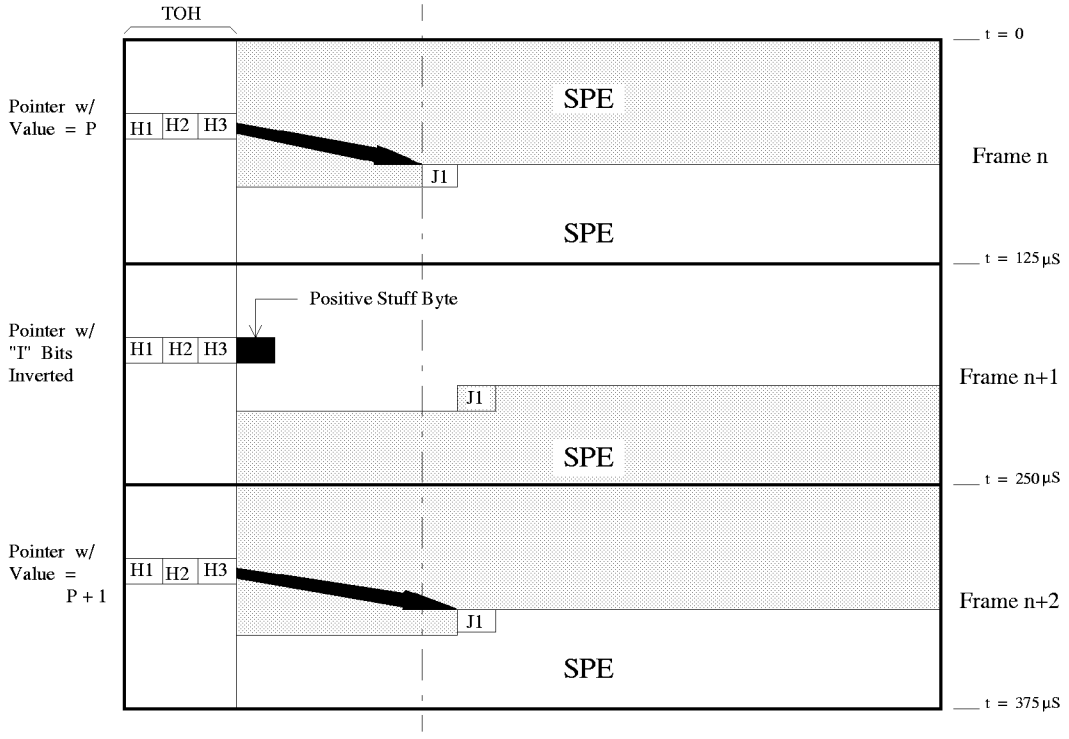


Figure 12. Positive Pointer Justifications

If the frame rate of the SPE is too fast with respect to the TOH, then the alignment of the envelope is periodically advanced in time and the pointer is decremented by one. This operation is indicated by inverting Bits 8, 10, 12, 14 and 16 (D Bits) of the Pointer Word. A negative stuff byte appears in the H3 Byte Position in the frame containing the inverted D Bits. Subsequent pointers contain the new offset. This is shown in Figure 13.

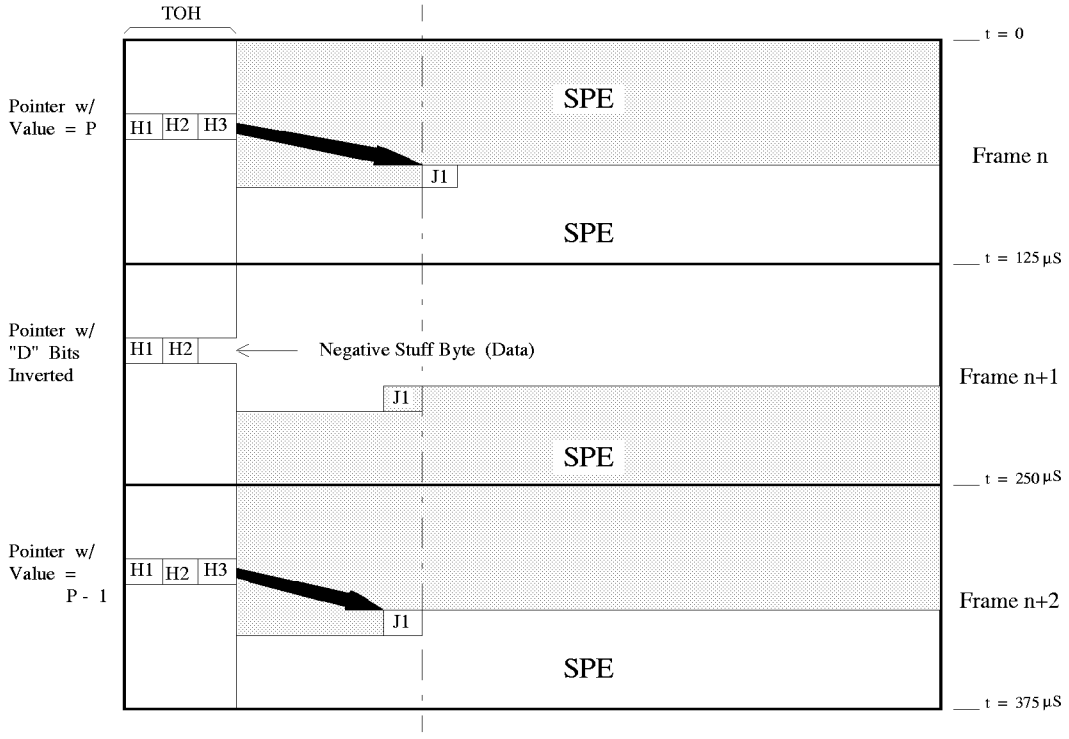


Figure 13. Negative Pointer Justifications

New Data Flag

Bits 1 through 4 (N Bits) of the Pointer Word carry a new Data Flag (NDF). This is a mechanism that allows an arbitrary change of the value of the pointer if that change is due to a change in payload. Normal operation is indicated by a "0110" code in the N Bits. NDF is indicated by inversion of the N Bits to "1001". The new alignment is indicated by the pointer value accompanying the NDF and takes effect at the offset indicated.

Concatenation

A concatenation indication contained in the Pointer Word is used to show that the STS-1 is part of an STS-Nc. The operations indicated in the pointer word of the first STS-1 within the STS-Nc apply to all STS-1s within the group. The pointer value must be multiplied by N to obtain the byte offset into the STS-Nc envelope capacity. Positive and negative justifications are performed as N byte multiples. In the remaining pointer words in the group the I and D Bits are set to all "1"s. The N Bits are set to "1001" and the S Bits are set to "00". The SOT-1 does not support concatenation but does provide a status bit indicating that a concatenation indication has been received in the H1 and H2 Bytes.

BLOCK DIAGRAM

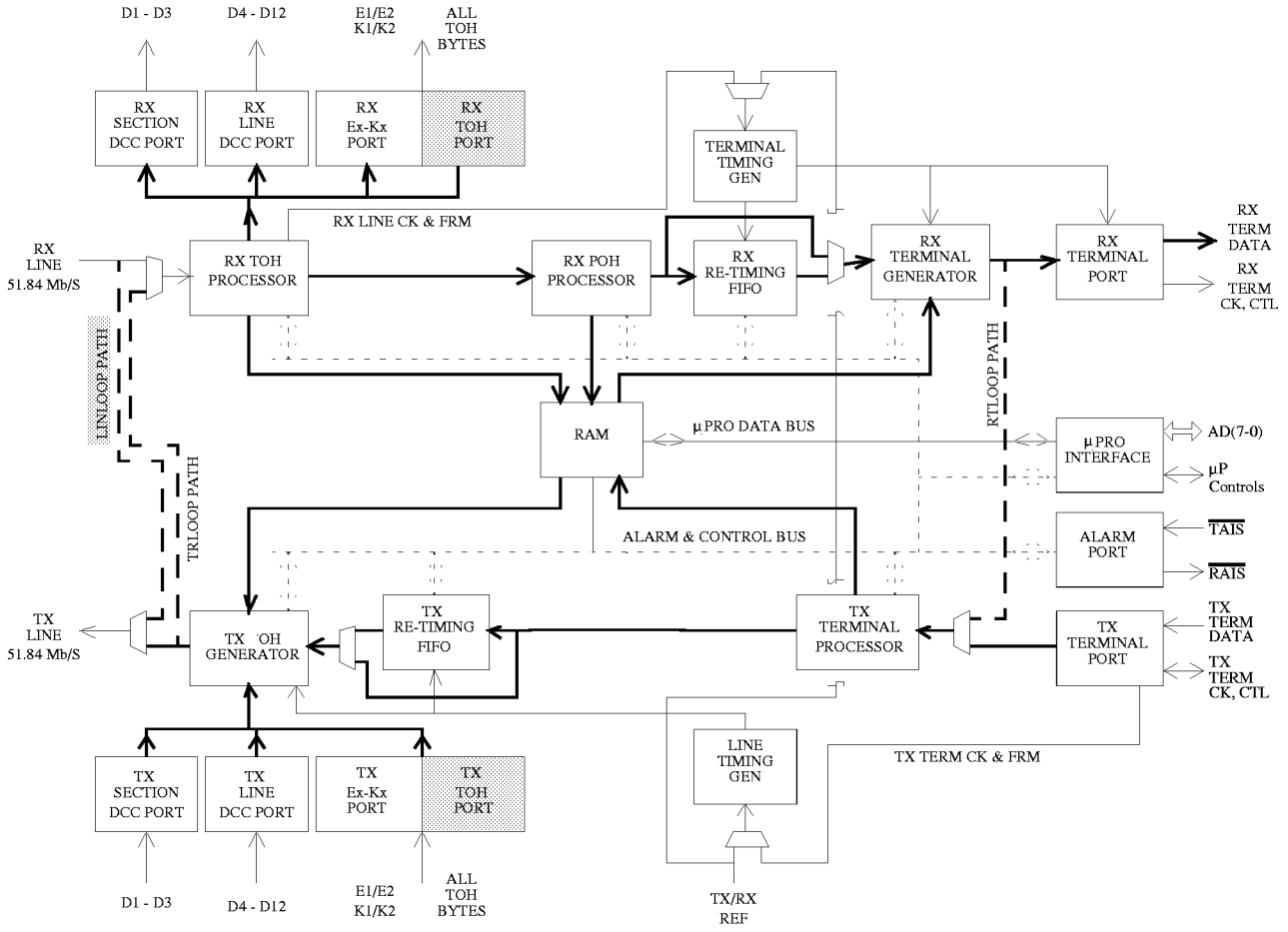


Figure 14. SOT-1 TXC-03001B Block Diagram

The Block Diagram for the SOT-1 TXC-03001B device is shown in Figure 14. There are two operating mode configurations. The first ("A") provides hardware and software backwards compatibility with the "A" version of the SOT-1 device, TXC-03001. The second ("B") provides enhanced features. Configuration selection is determined by the setting of the control bit NWFTREN in Control Register 10. TXC-03001 backwards compatible mode ("A") is enabled when NWFTREN is set to "0". The enhanced features mode ("B") is invoked if NWFTREN is set to "1". The shaded functions shown in the block diagram are only available in the enhanced features mode ("B").

This Data Sheet will only discuss enhanced mode ("B") features. Operation of the TXC-03001B SOT-1 device in the mode ("A") that is backwards compatible with the TXC-03001 device is explained in TranSwitch Technical Bulletin TB-516, entitled "Differences Between the "A" and "B" Versions of the SOT-1 VLSI Device", document number TXC-03001B-TB1.

RECEIVE SIDE

The Multiplexer at the Receive Line Input selects either the Line Side Input or the looped signal from the Transmit Line Output. The selected signal is applied to the Rx TOH Processor. The Rx TOH Processing BLock is responsible for Framing, De-scrambling, Overhead Distribution, and Overhead Processing. All Section and Line Overhead Bytes are stored in RAM and may be read through the µPro Interface. The Section and Line DCC Bytes are output at the Rx Section and Line DCC ports as serial Bit streams suitable for interfacing to HDLC Controllers. The Ex-Kx / TOH Port has two modes of operation. In the First Mode, it outputs the E1, E2, K1 and K2 Bytes in a manner that allows the E1 and E2 Bytes to be directly interfaced to CODECS. The other mode of operation allows external access to all of the Received TOH Bytes. Overhead Processing consists of J0 Processing, Error Accumulation (B1, B2, FEBE-L), De-bouncing of selected TOH Bytes, Pointer Tracking, and Alarm Detection. Section and Line Level Alarms are reported to the µPro Interface. AIS-L and Signal Fail conditions are output at the Alarm Port.

The Rx POH Processor Distributes and Processes the POH Bytes. All bytes are stored in RAM. Selected POH Bytes are de-bounced. B3 and FEBE-P error counts are accumulated. Path Level Alarms are reported to the µPro Interface. AIS-P conditions are output at the Alarm Port.

The Terminal Timing Generator and Rx Re-timing FIFO are used to justify the STS-1 SPE to a Rx Reference Frequency. In certain modes of operation the Re-timing Function can be bypassed. The Reference Frequency may be derived from the Rx Line or from the Tx/Rx Reference input. The Rx Re-timing FIFO Block performs Frequency Justification and Pointer Re-calculation.

The Rx Terminal Generator and Rx Terminal Port create and format the received Signal appearing at the Rx Terminal Port Outputs. The SOH and LOH Bytes (not applicable in SPE-only Mode) appearing at the output may be taken from RAM or generated internally. The POH bytes are taken from RAM or internally generated. The Rx Terminal Generator generates the required bytes and performs Alarm Insertion.

TRANSMIT SIDE

The data to be transmitted enters the SOT-1 at the Tx Terminal Port, with the Tx Terminal Clock and Control input signals.

The Multiplexer at the input to the Tx Terminal Processor selects either the Tx Terminal Port Data or the looped signal from the Rx Terminal Generator. The Tx Terminal Processor performs Frame Delineation, Pointer Tracking, stores all TOH (if present) and POH Bytes in RAM, accumulates B1, B2 and B3 errors, and detects Terminal Side Alarms. The payload portion of the STS-1 SPE is forwarded to the Tx Re-timing FIFO.

The Line Timing Generator and Tx Re-timing FIFO are used to justify the STS-1 SPE to a Tx Reference Frequency. In certain modes of operation the Re-timing Function can be bypassed. The Reference Frequency may be derived from the Tx Terminal or from the Tx/Rx Reference input. The Tx Re-timing FIFO Block performs Frequency Justification and Pointer Re-calculation.

The Tx OH Generator is responsible for Section, Line and Path Overhead Byte Assembly, TOH and POH Level Alarm Insertion, and scrambling. The POH Bytes are taken from RAM. The TOH Bytes are either internally generated, taken from RAM, or input externally. The external sources for the TOH Bytes are the Tx Ex-Kx / TOH Port, the Tx Line DCC Port, or the Tx Section DCC Port. Alarms are generated as a result of Rx Side anomalies, Terminal Side conditions, Alarm Port Input, or upon command from the µPro Interface. The Tx Line Output consists of either the Tx OH Generator Output or the looped Received Line Signal.

PIN DIAGRAMS

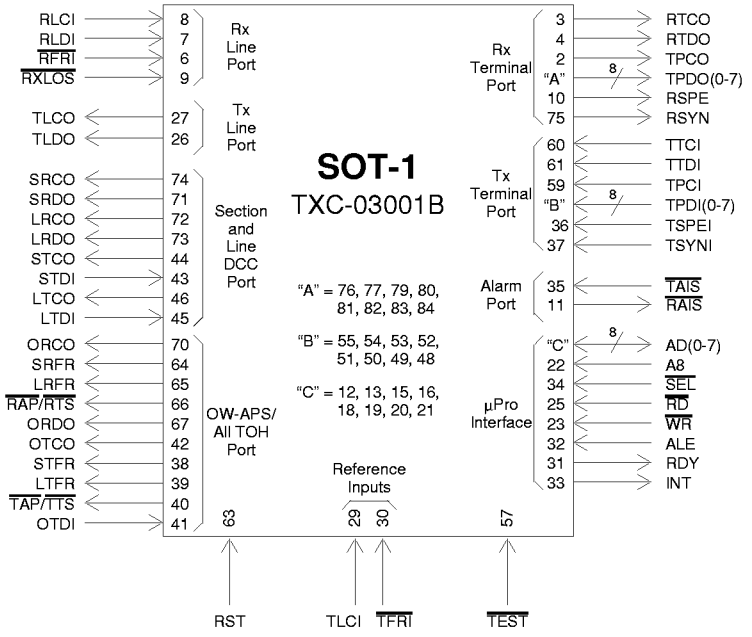


Figure 15. SOT-1 TXC-03001B Functional Pin Diagram

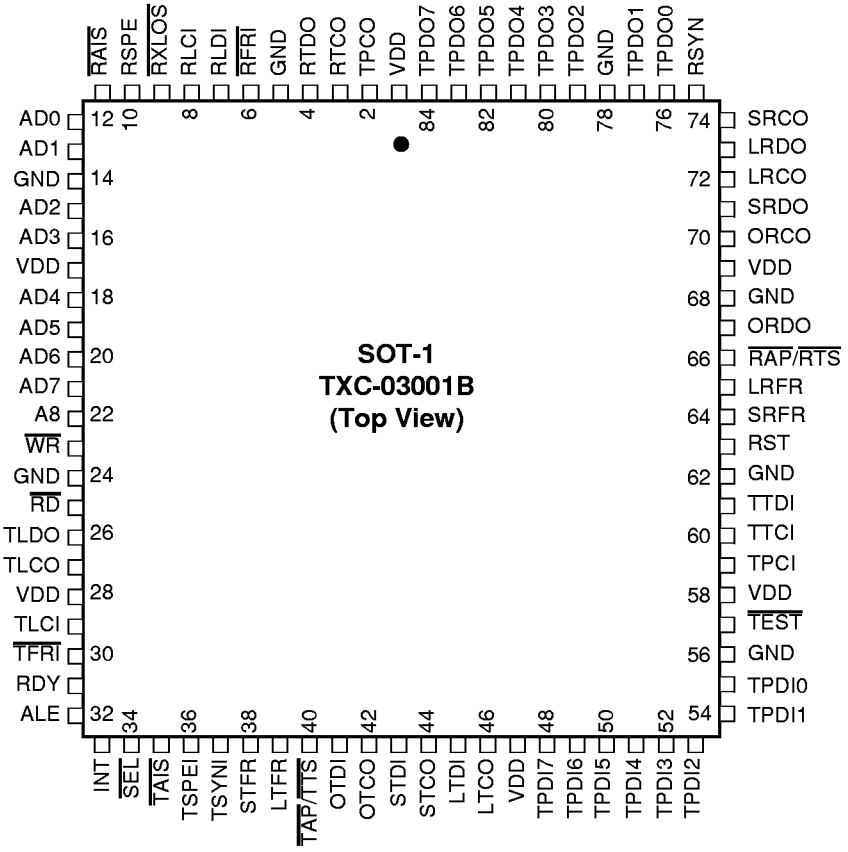


Figure 16. SOT-1 TXC-03001B Physical Pin Diagram

PIN DESCRIPTIONS

POWER SUPPLY AND GROUND PINS

Symbol	Pin No.	I/O/P*	Type**	Name/Function
VDD	1, 17, 28, 47, 58, 69	P		**V_{DD}:** +5 volt ±5 % Power Supply
GND	5, 14, 24, 56, 62, 68, 78	P		**V_{SS}:** Ground, 0 volt reference

* I = Input; O = Output; P = Power

** See Input, Output and I/O Parameters section below for Type Definitions.

REFERENCE INPUTS

Symbol	Pin No.	I/O/P	Type	Name/Function
TLCI	29	I	CMOS	**Transmit Line Clock Input:** 51.84 Mb/s clock. Depending on the operating modes it may be used for Transmit and/or Receive Side re-timing.
$\overline{\text{TFRI}}$	30	I	CMOSp	**Transmit Frame Reference In:** Optional, active Low frame pulse. Depending on the operating modes it may be used to define the Transmit Line and/or Receive Terminal start of frame.

RECEIVE LINE SIDE INTERFACE

Symbol	Pin No.	I/O/P	Type	Name/Function
$\overline{\text{RFRI}}$	6	I	CMOSp	**Receive Line Frame In:** Optional, active Low frame pulse that occurs during the C1 Byte, Bit 7 time. When used, it reduces the SEF/OOF exit time from two frames to one frame. This input is only enabled if STS1 = "0". It is clocked in on the rising edge of RLCI.
RLDI	7	I	CMOS	**Receive Line Data Input:** Incoming, serial STS-1 data which is clocked in on the rising edge of RLCI.
RLCI	8	I	CMOS	**Receive Line Clock Input:** Incoming 51.84 Mb/s Clock.
$\overline{\text{RXLOS}}$	9	I	TTLp	**Receive Loss Of Signal:** Active Low, external, LOS indicator. This input is combined with the internal LOS detectors to produce the RLOS status indicator.

TRANSMIT LINE SIDE INTERFACE

Symbol	Pin No.	I/O/P	Type	Name/Function
TLDO	26	O	CT4	**Transmit Line Data Output:** Outgoing, serial STS-1 Data which is clocked out on the falling edge of TLCO.
TLCO	27	O	CT4	**Transmit Line Clock Output:** Outgoing 51.84 Mb/s Clock. When TCLK = "0", it is derived from TTCI or TLCI, depending on the operating mode. If TCLK = "1", it is derived from TLCI.

TERMINAL SIDE INTERFACE

Symbol	Pin No.	I/O/P	Type	Name/Function
RTCO	3	O	CT4	**Receive Terminal Clock Output:** Serial, 51.84 Mb/s terminal clock. Depending on the operating modes RTCO may be derived from either RLCI or TLCI.
RTDO	4	O	CT4	**Receive Terminal Data Output:** Serial, 51.84 Mb/s data. Data is clocked out on the Falling Edge of RTCO.
TPCO	2	O	CT4	**Terminal Parallel Clock Output:** Parallel, 6.48 Mb/s, Rx Terminal clock. Depending on the operating modes TPCO may be derived from either RLCI or TLCI. When INVPCK = "1", RSYN and RSPE are clocked out on the Rising Edge of TPCO. RTDSEL controls the position of RSYN, RSPE and TPDO(0-7) with respect to TPCO.
TPDO(0,1)	76, 77	O	CT4	**Terminal Parallel Data Output:** Parallel, 6.48 Mb/s, Rx Terminal data. TPDO0 is the LSB of the SONET Byte. When INVPCK = "0", information is clocked out on the Falling Edge of TPCO. When INVPCK = "1", information is clocked out on the Rising Edge. RTDSEL controls the position of RSYN, RSPE and TPDO(0-7) with respect to TPCO.
TPDO(2-7)	79-84			
RSPE	10	O	CT4	**Receive Terminal SPE Indication:** In SPE-only Mode, this is the active Low gapping signal. In SONET mode, it is Low during the TOH Byte times and High during the SPE Byte times. RSPE is clocked out on the Falling Edge of RTCO. When INVPCK = "0", RSPE is clocked out on the Falling Edge of TPCO. When INVPCK = "1", RSPE is clocked out on the Rising Edge of TPCO. See Note 1.
RSYN	75	O	CT4	**Receive Terminal Sync Pulse:** In SONET mode, this is High during the C1, J1, and optionally V1,1 Byte times. In SPE-only Mode, this is High during the J1 Byte time and optionally V1 Byte time. RSYN is clocked out on the Falling Edge of RTCO. When INVPCK = "0", RSYN is clocked out on the Falling Edge of TPCO. When INVPCK = "1", RSYN is clocked out on the Rising Edge of TPCO. See Note 1.

Note 1: Further information on how RSPE and RSYN are clocked out in the various operating modes of the device are provided in the Timing Characteristics and Operations sections.

Symbol	Pin No.	I/O/P	Type	Name/Function
TTCI	60	I	CMOS	**Transmit Terminal Clock Input:** Serial, 51.84 Mb/s terminal clock. In SONET and SPE-only Modes, it is an Input. Since it is possible for the device to power up with this pin as an output, a reset should be performed via pin RST. If this pin is unused, it should be tied high or low through a resistor of 1 kΩ or higher resistance.
TTDI	61	I	CMOS	**Transmit Terminal Data Input:** Serial, 51.84 Mb/s data. Data is clocked in on the Rising Edge of TTCI.
TPCI	59	I	TTL	**Terminal Parallel Clock Input:** Parallel 6.48 Mb/s, Tx Terminal clock. Since it is possible for the device to power up with this pin as an output, a reset should be performed via pin RST. If this pin is unused, it should be tied high or low through a resistor of 1 kΩ or higher resistance.
TPDI(0-7)	55-48	I	TTL	**Terminal Parallel Data Input:** Parallel 6.48 Mb/s, Tx Terminal data. In SONET Mode, data is clocked in on the Rising Edge of TPCI.
TSPEI	36	I	CMOS	**Tx Terminal SPE Input:** In SONET Modes, this is an input which is active high during the SPE Byte times. In SPE-only Mode, this is an input which is the active Low gapping signal. In Serial Modes, TSPEI is sampled on the Rising Edge of TTCI. In Parallel Modes, TSPEI is sampled on the Rising Edge of TPCI when INVPCK="0" or on the Falling Edge when INVPCK="1". Since it is possible for the device to power up with this pin as an output, a reset should be performed via pin RST. If this pin is unused, it should be tied high or low through a resistor of 1 kΩ or higher resistance.
TSYNI	37	I	CMOS	**Tx Terminal Sync Pulse Input:** In SONET Mode, this is an input which is high during the C1, J1, and, optionally, V1,1 byte times. In SPE-only Mode, this is an input which is High during the J1 byte time and optionally the V1 Byte time. In Serial Modes, TSYNI is sampled on the Rising Edge of TTCI. In Parallel Modes, TSYNI is sampled on the Rising Edge of TPCI when INVPCK="0" or on the Falling Edge when INVPCK="1". Since it is possible for the device to power up with this pin as an output, a reset should be performed via pin RST. If this pin is unused, it should be tied high or low through a resistor of 1 kΩ or higher resistance.

ORDER WIRE/APS INTERFACE

Symbol	Pin No.	I/O/P	Type	Name/Function
ORCO	70	O	CT4	**Receive TOH Port Clock Output:** Rx TOH Port output clock. If OA = "1", the rate is 576 kb/s. When OA = "0", the rate is 1.728 Mb/s.
ORDO	67	O	CT4	**Receive Order Wire and APS/TOH Byte Output:** Rx TOH Port data. The information is clocked out on the Rising Edge of ORCO.
SRFR	64	O	CT4	**Receive Section Order Wire Framing Pulse:** Receive framing pulse for Section Order Wire CODEC/filter. SRFR is clocked out on the Rising Edge of ORCO.
LRFR	65	O	CT4	**Receive Line Order Wire Framing Pulse:** Receive framing pulse for Line Order Wire CODEC/filter. LRFR is clocked out on the Rising Edge of ORCO.
$\overline{\text{RAP}}$/$\overline{\text{RTS}}$	66	O	CT4	**Receive APS/TOH Framing Pulse:** Active low receive framing Pulse. When OA = "1", this signal occurs one clock cycle after the LSB of the K2 Byte in OTDO. If OA = "0", it occurs one clock cycle before the MSB of the A1 Byte. $\overline{\text{RAP}}$/$\overline{\text{RTS}}$ is clocked out on the Rising Edge of ORCO.
OTCO	42	O	CT4	**Transmit TOH Port Clock Output:** Output Tx TOH Port clock which is used for sourcing data into the SOT-1. If OA = "1" the rate is 576 kb/s. When OA = "0" the rate is 1.728 Mb/s.
OTDI	41	I	TTLp	**Transmit Order Wire and APS/TOH Byte Input:** Tx TOH Port data. The information is clocked in on the Falling Edge of OTCO.
STFR	38	O	CT4	**Transmit Section Order Wire Framing Pulse:** Transmit framing pulse for Section Order Wire CODEC/filter. STFR is clocked out on the Rising Edge of OTCO.
LTFR	39	O	CT4	**Transmit Line Order Wire Framing Pulse:** Transmit framing pulse for Line Order Wire CODEC/filter. LTFR is clocked out on the Rising Edge of OTCO.
$\overline{\text{TAP}}$/$\overline{\text{TTS}}$	40	O	CT4	**Transmit APS/TOH Framing Pulse:** Active low transmit framing Pulse. When OA = "1", this signal occurs one clock cycle before the MSB of the K1 Byte is expected on OTDI. If OA = "0", it occurs one clock cycle before the MSB of the A1 Byte is expected on OTDI. $\overline{\text{TAP}}$/$\overline{\text{TTS}}$ is clocked out on the Falling Edge of OTCO.

SECTION AND LINE DATA COMMUNICATIONS INTERFACE

Symbol	Pin No.	I/O/P	Type	Name/Function
SRCO	74	O	CT4	**Receive Section DCC Clock Output:** 192 kb/s Clock, derived from RLCI, which is used for clocking out Section DCC information.
SRDO	71	O	CT4	**Receive Section DCC Data Output:** Serial 192 kb/s output for D1-D3 Bytes. Data is clocked out on the Falling Edge of SRCO.
LRCO	72	O	CT4	**Receive Line DCC Clock Output:** 576 kb/s Clock, derived from RLCI, which is used for clocking out Line DCC information.
LRDO	73	O	CT4	**Receive Line DCC Data Output:** Serial 576 kb/s output for D4-D12 Bytes. Data is clocked out on the Falling Edge of LRCO.
STCO	44	O	CT4	**Transmit Section DCC Clock Output:** 192 kb/s Clock, derived from TLCO, which is used for sourcing the Section DCC information into the SOT-1.
STDI	43	I	TTLp	**Transmit Section DCC Data Output:** Serial 192 kb/s input for D1-D3 Bytes. Data is clocked in on the Rising Edge of STCO.
LTCO	46	O	CT4	**Transmit Line DCC Clock Output:** 576 kb/s Clock, derived from TLCO, which is used for sourcing Line DCC information into the SOT-1.
LTDI	45	I	TTLp	**Transmit Line DCC Data Input:** Serial 576 kb/s input for D4-D12 Bytes. Data is clocked in on the Rising Edge of LTCO.

MICROPROCESSOR INTERFACE

Symbol	Pin No.	I/O/P	Type	Name/Function
AD(0, 1)	12, 13	I/O	TTL/CT8	**Address/Data Bus:** Multiplexed address input and bidirectional data bus, Bits 0-7.
AD(2, 3)	15, 16			
AD(4-7)	18-21			
A8	22	I	TTL	**Address Bus - Bit 8:** Bit 8 of the address input bus.
$\overline{WR}$	23	I	TTLp	**Write Enable:** Active low signal that enables writing to the SOT-1 memory.
$\overline{RD}$	25	I	TTLp	**Read Enable:** Active low signal that enables reading of the SOT-1 memory.
RDY	31	O	OD 16 mA	**Ready:** Active high acknowledges that the transfer can be completed. A low indicates that wait states are required.
ALE	32	I	TTLp	**Address Latch Enable:** Falling edge latches address information in the SOT-1.
INT	33	O	CT4	**Interrupt:** Active high interrupt request to the µPro. Polarity is inverted when INVINT="1".
$\overline{SEL}$	34	I	TTLp	**Device Select:** Active low signal that allows reading or writing to the SOT-1 memory.

ALARM PORT

Symbol	Pin No.	I/O/P	Type	Name/Function
$\overline{RAIS}$	11	O	CT4	**Receive Alarm Indication Signal:** Active low signal indicating that a received AIS condition has been detected. See Equation 2 (page 123).
$\overline{TAIS}$	35	I	TTLp	**Transmit Alarm Indication Signal:** Active low signal that causes AIS to be introduced into the Tx Line.

MISCELLANEOUS PINS

Symbol	Pin No.	I/O/P	Type	Name/Function
RST	63	I	TTL	**Reset:** Hardware Reset. RST is a positive pulse with a minimum pulse width of 20 ns. It must be used after power is applied and the clocks are stable.
$\overline{TEST}$	57	I	TTLp	**Test Enable:** An active low signal that activates the Test State. If RST = "1" and $\overline{TEST}$ = "0" all output and bidirectional pins assume the Tri-state condition.

ABSOLUTE MAXIMUM RATINGS AND ENVIRONMENTAL LIMITATIONS

Parameter	Symbol	Min	Max	Unit	Conditions
Supply voltage	V_{DD}	-0.3	+7.0	V	Note 1
DC input voltage	V_{IN}	-0.5	V_{DD} + 0.5	V	Note 1
Storage temperature range	T_S	-55	150	°C	Note 1
Ambient operating temperature	T_A	-40	85	°C	0 ft/min linear air-flow
Component Temperature x Time	TI		270 x 5	°C x s	
Moisture Exposure Level	ME	5		Level	per EIA/JEDEC JESD22-A112-A
Relative Humidity, non-condensing	RH		100	%	Note 2
ESD Classification	ESD		±2000	V	per MIL-STD-883D Method 3015.7

Notes:
1. Conditions exceeding the Min or Max values may cause permanent failure. Exposure to conditions near the Min or Max values for extended periods may impair device reliability.
2. Pre-assembly storage in non-drypack conditions is not recommended or warranted.

THERMAL CHARACTERISTICS

Parameter	Min	Typ	Max	Unit	Test Conditions
Thermal resistance - junction to ambient			41.6	°C/W	0 ft/min linear airflow

POWER REQUIREMENTS

Parameter	Min	Typ	Max	Unit	Test Conditions
Supply Voltage, V_{DD}	4.75	5.0	5.25	V	
Supply Current, I_{DD}			150	mA	
Power Dissipation, P_{DD}			790	mW	

INPUT, OUTPUT AND I/O PARAMETERS

DC Characteristics at T_A = -40°C to +85°C; V_{DD} = +5V ±5%; V_{SS} = 0V

Parameter	Min	Typ	Max	Unit	Notes
CMOS Input High Voltage, C-V_{IH}	3.15		V_{DD}+0.5	V	
CMOS Input Low Voltage, C-V_{IL}	-0.5		1.65	V	
TTL Input High Voltage, T-V_{IH}	2.0		V_{DD}+0.5	V	
TTL Input Low Voltage, T-V_{IL}	-0.5		0.8	V	
Input High Current, I_{IH}			10	µA	1
Input Low current, I_{IL}			-10	µA	1
Output High Voltage, V_{OH}	V_{DD}-0.5			V	2
Output Low Voltage, V_{OL}			0.4	V	3
CMOS/TTL 4 mA Output High Current, CT4-I_{OH}	-4.0			mA	4, 6
CMOS/TTL 4 mA Output Low Current, CT4-I_{OL}	4.0			mA	4, 6
CMOS/TTL 8 mA Output High Current, CT8-I_{OH}	-8.0			mA	4, 6
CMOS/TTL 8 mA Output Low Current, CT8-I_{OL}	8.0			mA	4, 6
CMOS/TTL OD Output Low Current, CT16OD-I_{OL}	16			mA	4, 6, 8
Tri-state Output Leakage Current, I_{OLK}			±10	µA	
TTLp Input Leakage Current, TP-I_{ILK}	75	160	270	µA	5, 7
CMOSp Input Leakage Current, CP-I_{ILK}	75	160	270	µA	5, 7
Input Capacitance, C_I			5	pF	
Output Capacitance, C_O			5	pF	

Notes:
1. V_{IH} = 5.25 V
2. V_{DD} = 4.75 V, I_{OH} = Max
3. V_{DD} = 4.75 V, I_{OL} = Max
4. V_{DD} = 4.75 V
5. V_{DD} = 5.25 V, Input = 0 V
6. All outputs are CMOS and TTL compatible
7. Suffix "p" indicates type of input pin that has internal pull-up to high signal level.
8. "OD" indicates open drain output type.

TIMING CHARACTERISTICS

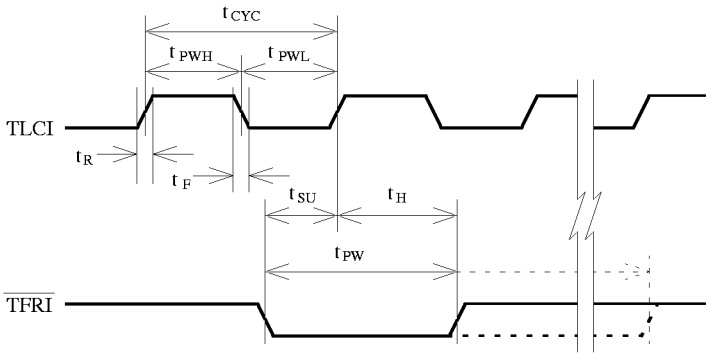
Figures 17 to 33 in this section describe the detailed timing characteristics for the SOT-1. All output times are measured with a load capacitance of 25 pF. Timing parameters are measured at:

1. TTL Inputs - V_{IL} = 0 V, V_{IH} = 3.0 V, and Input Transitions = 1.3 V
2. TTL Outputs - 1.3 V
3. CMOS Inputs - V_{IL} = 0 V, V_{IH} = V_{DD}, and Input Transitions = (V_{DD} ÷ 2) V
4. CMOS Outputs - [(V_{OH} + V_{OL}) ÷ 2] V

REFERENCE INPUTS

Figure 17 shows the timing Reference Input requirements for both the Terminal Timing Generator and the Line Timing Generator. The Timing Generators synchronize to the first Rising Edge of the clock following the active Level of the Frame Reference.

Figure 17. Reference Input Timing



Parameter	Symbol	Min	Typ	Max	Unit	Notes
TLCI	t_{CYC}	19.25	19.29	19.33	ns	
TLCI Fall Time (90% - 10%)	t_F			4.0	ns	
Hold - $\overline{\text{TFRI}}$ after ↑ TLCI	t_H	2.0			ns	
Pulse Width - $\overline{\text{TFRI}}$	t_{PW}	0.9 x	1 x	8.1 x	t_{CYC}	
TLCI High Time	t_{PWH}	45%	50%	55%	t_{CYC}	
TLCI Low Time	t_{PWL}	45%	50%	55%	t_{CYC}	
TLCI Rise Time (10% - 90%)	t_R			4.0	ns	
Set-up - $\overline{\text{TFRI}}$ to ↑ TLCI	t_{SU}	4.0			ns	

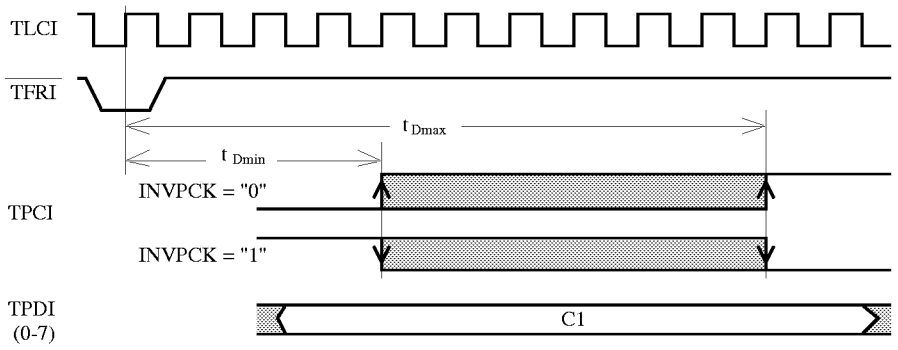
TERMINAL TIMING IN PARALLEL MODES

When the SOT-1 is operating in modes where TCLK="0" and PARA="1", the TLCI, TPCI and $\overline{\text{TFRI}}$ inputs must be as described below:

1. TLCI and TPCI must be derived from the same source
2. The phase relationship shown in Figure 18 must be maintained.

Please refer to the Line Timing Generator subsection of the Operation section for additional information (page 101).

Figure 18. Frame Phase Margin - Tx Re-Timing Disabled

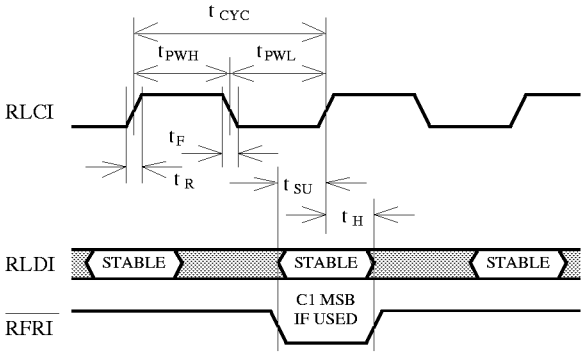


Parameter	Symbol	Value	Notes
Minimum Delay - ↑ TLCI that clocks in $\overline{\text{TFRI}}$ to the active edge of TPCI that clocks in the C1 Byte	t_{Dmin}	4 TLCI Clock Periods	
Maximum Delay - ↑ TLCI that clocks in $\overline{\text{TFRI}}$ to the active edge of TPCI that clocks in the C1 Byte	t_{Dmax}	10 TLCI Clock Periods	

LINE SIDE TIMING

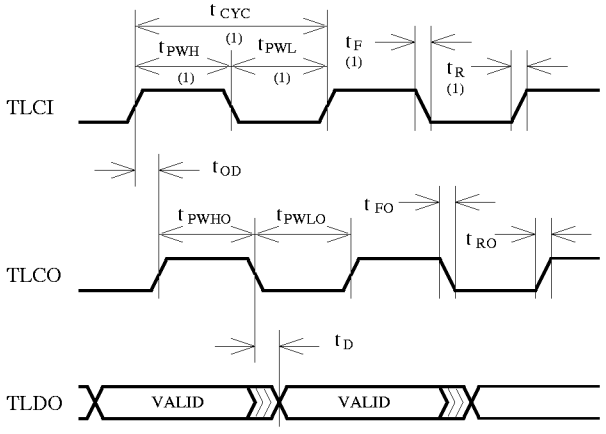
Figures 19 and 20 detail the timing for the Receive and Transmit Line Inputs and Outputs, respectively.

Figure 19. Receive Line Input Timing



Parameter	Symbol	Min	Typ	Max	Unit	Notes
RLCI Period	t_{CYC}	19.25	19.29	19.33	ns	
RLCI Fall Time (90% - 10%)	t_F			4.0	ns	
Hold - RLDI, $\overline{RFRI}$ after ↑ RLCI	t_H	2.0			ns	
RLCI High Time	t_{PWH}	45%	50%	55%	t_{CYC}	
RLCI Low Time	t_{PWL}	45%	50%	55%	t_{CYC}	
RLCI Rise Time (10% - 90%)	t_R			4.0	ns	
Set-up - RLDI, $\overline{RFRI}$ to ↑ RLCI	t_{SU}	4.0			ns	

Figure 20. Transmit Line Output Timing



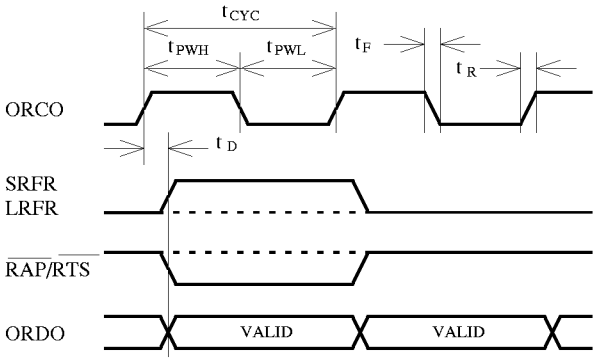
Parameter	Symbol	Min	Typ	Max	Unit	Notes
Delay - ↓ TLCO to TLDO	t_D	-1.0	0	3.0	ns	
TLCO Output Fall Time (90% - 10%)	t_{FO}			1.7	ns	2
Output Delay - ↑ TLCI to ↑ TLCO	t_{OD}	6.0	15	24	ns	
TLCO High Time	t_{PWHO}	40%	50%	60%	t_{CYC}	
TLCO Low Time	t_{PWLO}	40%	50%	60%	t_{CYC}	
TLCO Output Rise Time (10% - 90%)	t_{RO}			1.5	ns	2

Notes:
1. See Reference Input Timing characteristics (Figure 17, page 30).
2. 25 pF load.

ORDER WIRE-APS / TOH PORT TIMING

The output timing characteristics of the Order Wire-APS (OW-APS) / TOH Port are shown in Figures 21 and 22.

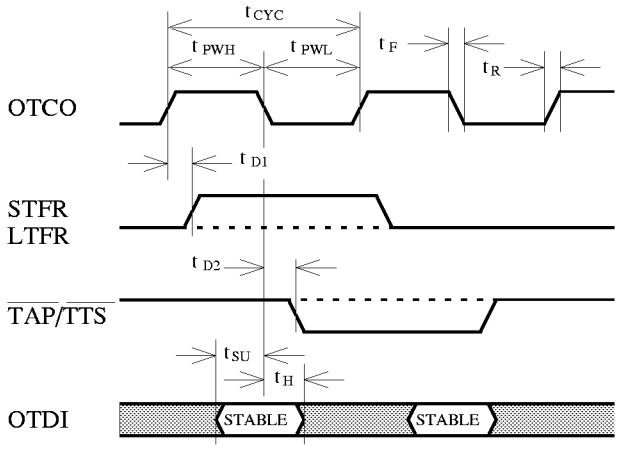
Figure 21. Rx OW-APS / TOH Port Output Timing



Parameter	Symbol	Min	Typ	Max	Unit	Notes
ORCO Period - OW/APS Mode	t_{CYC}	1732	1736	1740	ns	
ORCO Period - All TOH Mode		576	578.7	581.4		
Delay - ↑ ORCO to SRFR, LRFR, $\overline{RAP}/\overline{RTS}$ or ORDO	t_D	-5.0		5.0	ns	
ORCO Fall Time (90% - 10%)	t_F			2.5	ns	1
ORCO High Time	t_{PWH}	40%	50%	60%	t_{CYC}	
ORCO Low Time	t_{PWL}	40%	50%	60%	t_{CYC}	
ORCO Rise Time (10% - 90%)	t_R			2.0	ns	1

Note 1: 25 pF Load.

Figure 22. Tx OW-APS / TOH Port Input Timing



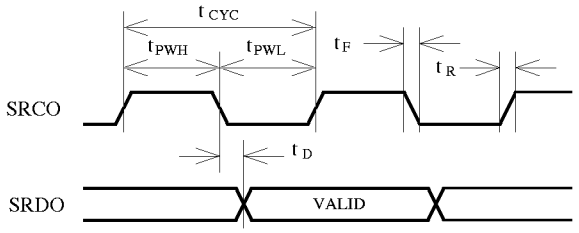
Parameter	Symbol	Min	Typ	Max	Unit	Notes
OTCO Period - OW/APS Mode	t_{CYC}	1732	1736	1740	ns	
OTCO Period - All TOH Mode		576	578.7	581.4		
Delay - ↑ OTCO to STFR, LTFR	t_{D1}	-5.0		5.0	ns	
Delay - ↓ OTCO to $\overline{TAP}/\overline{TTS}$	t_{D2}	-5.0		5.0	ns	
OTCO Fall Time (90% - 10%)	t_F			2.5	ns	1
Hold - OTDI after ↓ OTCO	t_H	0.0			ns	
OTCO High Time	t_{PWH}	40%	50%	60%	t_{CYC}	
OTCO Low Time	t_{PWL}	40%	50%	60%	t_{CYC}	
OTCO Rise Time (10% - 90%)	t_R			2.0	ns	1
Set-up - OTDI to ↓ OTCO	t_{SU}	7.0			ns	

Note 1: 25 pF load.

SECTION AND LINE DCC PORT TIMING

The output timing for the Section and Line DCC Ports is shown in Figures 23 and 24. Figures 25 and 26 depict the input timing.

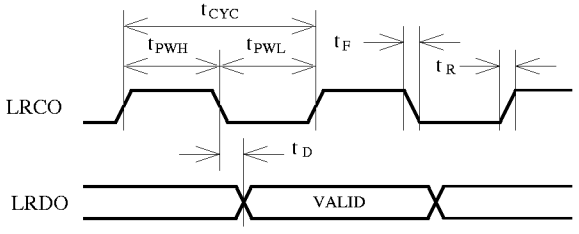
Figure 23. Rx Section DCC Port Output Timing



Parameter	Symbol	Min	Typ	Max	Unit	Notes
SRCO Period	t_{CYC}	5.20	5.21	5.22	µs	
Delay - ↓ SRCO to SRDO	t_D	-5.0	0	5.0	ns	
SRCO Fall Time (90% - 10%)	t_F			2.5	ns	1
SRCO High Time	t_{PWH}	40%	50%	60%	t_{CYC}	
SRCO Low Time	t_{PWL}	40%	50%	60%	t_{CYC}	
SRCO Rise Time (10% - 90%)	t_R			2.0	ns	1

Note 1: 25 pF Load.

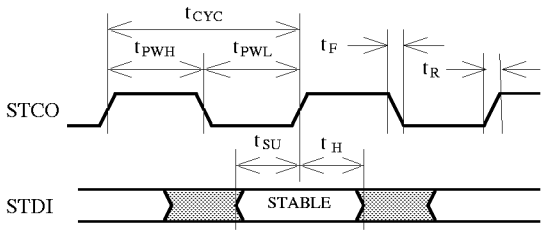
Figure 24. Rx Section DCC Port Output Timing



Parameter	Symbol	Min	Typ	Max	Unit	Notes
LRCO Period	t_{CYC}	1732	1736	1740	ns	
Delay - ↓ LRCO to LRDO	t_D	-5.0	0	5.0	ns	
LRCO Fall Time (90% - 10%)	t_F			2.5	ns	1
LRCO High Time	t_{PWH}	40%	50%	60%	t_{CYC}	
LRCO Low Time	t_{PWL}	40%	50%	60%	t_{CYC}	
LRCO Rise Time (10% - 90%)	t_R			2.0	ns	1

Note 1: 25 pF Load.

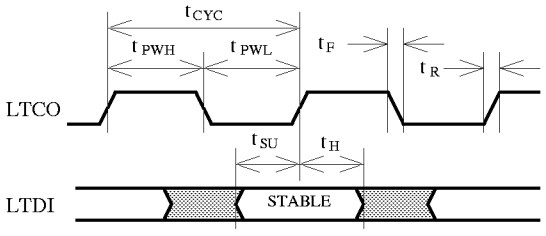
Figure 25. Tx Section DCC Port Input Timing



Parameter	Symbol	Min	Typ	Max	Unit	Notes
STCO Period	t_{CYC}	5.20	5.21	5.22	µs	
STCO Fall Time (90% - 10%)	t_F			2.5	ns	1
Hold - STDI after ↑ STCO	t_H	0.0			ns	
STCO High Time	t_{PWH}	40%	50%	60%	t_{CYC}	
STCO Low Time	t_{PWL}	40%	50%	60%	t_{CYC}	
STCO Rise Time (10% - 90%)	t_R			2.0	ns	1
Set-up - STDI to ↑ STCO	t_{SU}	7.0			ns	

Note 1: 25 pF load.

Figure 26. Tx Line DCC Port Input Timing



Parameter	Symbol	Min	Typ	Max	Unit	Notes
LTCO Period	t_{CYC}	1732	1736	1740	ns	
LTCO Fall Time (90% - 10%)	t_F			2.5	ns	1
Hold - LTDI after ↑ LTCO	t_H	0.0			ns	
LTCO High Time	t_{PWH}	40%	50%	60%	t_{CYC}	
LTCO Low Time	t_{PWL}	40%	50%	60%	t_{CYC}	
LTCO Rise Time (10% - 90%)	t_R			2.0	ns	1
Set-up - LTDI to ↑ LTCO	t_{SU}	7.0			ns	

Note 1: 25 pF load.

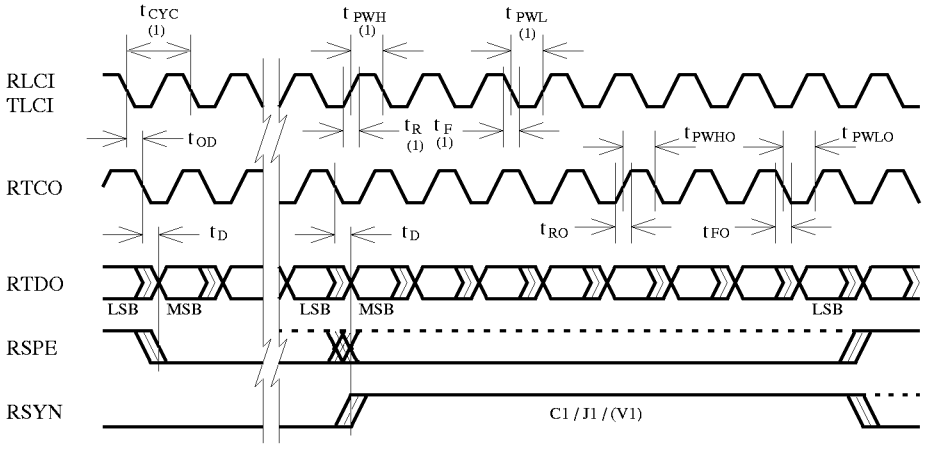
TERMINAL SIDE TIMING

The Tx and Rx Terminal Port Timing is shown in Figures 27 - 31.

Rx Terminal Port Timing

Figures 27 through 29 show the output timing for the Rx Terminal Port.

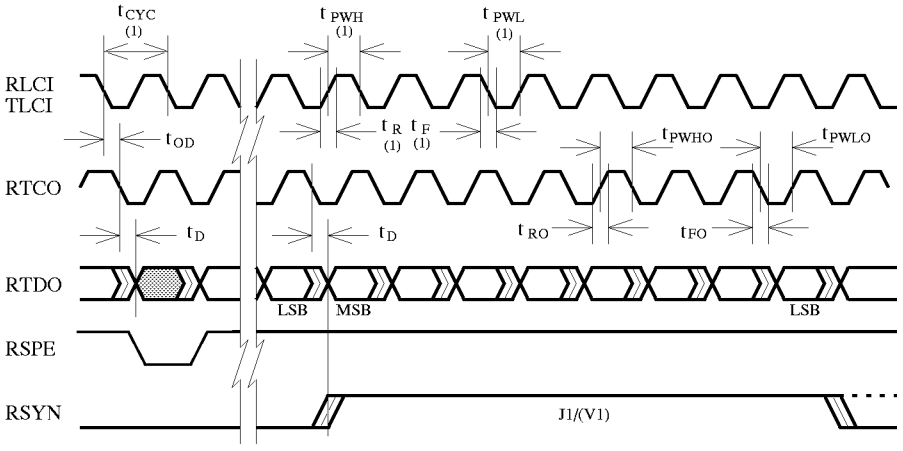
Figure 27. SONET Serial Output Timing



Parameter	Symbol	Min	Typ	Max	Unit	Notes
Delay - ↓ RTCO to RTDO, RSPE or RSYN	t_D	-1.0	0.0	3.0	ns	
RTCO Output Fall Time (90% - 10%)	t_{FO}			1.7	ns	2
Delay - ↓ RLCI/TLCI to ↓ RTCO	t_{OD}	6.0	15	24	ns	
RTCO Output Rise Time (10% - 90%)	t_{RO}			1.5	ns	2
RTCO High Time	t_{PWHO}	40%	50%	60%	t_{CYC}	
RTCO Low Time	t_{PWLO}	40%	50%	60%	t_{CYC}	

Notes:
1. See Reference Input or Rx Line Timing Characteristics (Figure 17, page 30 or Figure 19, page 32).
2. 25 pF Load.

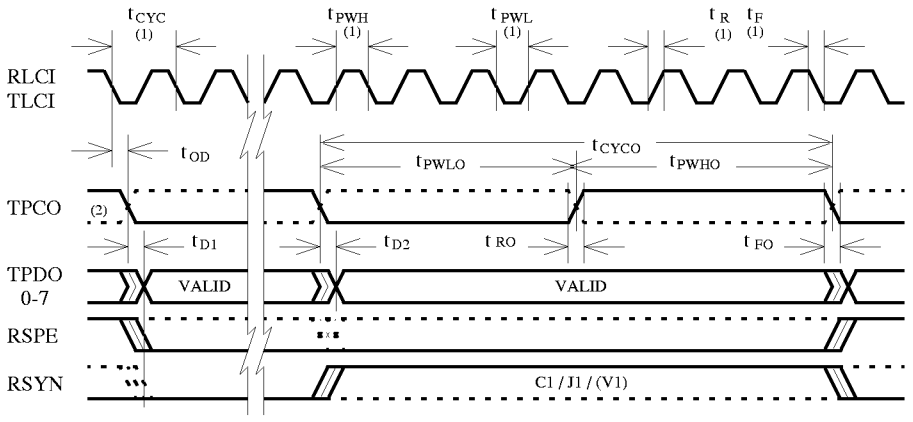
Figure 28. SPE-Only Output Timing



Parameter	Symbol	Min	Typ	Max	Unit	Notes
Delay - ↓ RTCO to RTDO, RSPE or RSYN	t_D	-1.0	0.0	3.0	ns	
RTCO Output Fall Time (90% - 10%)	t_{FO}			1.7	ns	2
Delay - ↓ RLCI/TLCI ↓ RTCO	t_{OD}	6.0	15	24	ns	
RTCO Output Rise Time (10% - 90%)	t_{RO}			1.5	ns	2
RTCO High Time	t_{PWHO}	40%	50%	60%	t_{CYC}	
RTCO Low Time	t_{PWLO}	40%	50%	60%	t_{CYC}	

Notes
1. See Reference Input or Rx Line Timing Characteristics (Figure 17, page 30 or Figure 19, page 32).
2. 25 pF Load.

Figure 29. Parallel Output Timing



Parameter	Symbol	Min	Typ	Max	Unit	Notes
TPCO Period	t_{CYCO}		8 x		t_{CYC}	
Delay - ↓ TPCO to RSPE or RSYN	t_{D1}	-5.0	0.0	5.0	ns	3, 5
Delay - ↓ TPCO to TPDO(0-7)	t_{D2}	-5.0	0.0	5.0	ns	3, 5
TPCO Output Fall Time (90% - 10%)	t_{FO}			2.5	ns	4
Delay - ↓ RLCI/TLCI to ↓ TPCO	t_{OD}	6.0	15	24	ns	3
TPCO Output Rise Time (10% - 90%)	t_{RO}			2.0	ns	4
TPCO High Time	t_{PWHO}	40%	50%	60%	t_{CYCO}	
TPCO Low Time	t_{PWLO}	40%	50%	60%	t_{CYCO}	

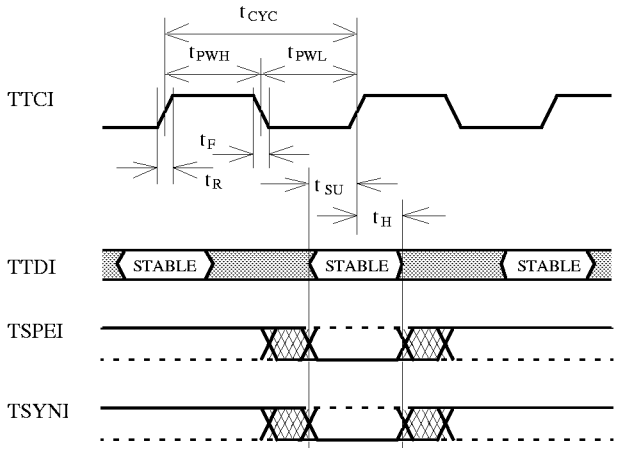
Notes:

1. See Reference Input or Rx Line Characteristics (Figure 17, page 30 or Figure 19, page 32).
2. TPCO inverted (dotted line) when INVPCK = "1".
3. ↑ TPCO when INVPCK ="1".
4. 25 pF Load.
5. The values shown apply when RTDSEL="1". If RTDSEL="0", RSPE and RSYN occur two TPCO periods earlier and TPDO(0-7) occur one TPCO period earlier.

Tx Terminal Port Timing

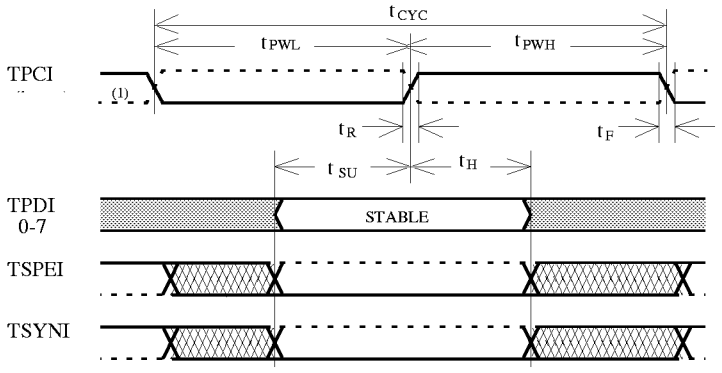
Figures 30 and 31 show the input timing for the Tx Terminal Port.

Figure 30. Serial SONET and SPE-Only Input Timing



Parameter	Symbol	Min	Typ	Max	Unit	Notes
TTCI Period	t_{CYC}	19.25	19.29	19.33	ns	
TTCI Fall Time (90% - 10%)	t_F			4.0	ns	
Hold - TTDI, TSPEI or TSYNI after ↑ TTCI	t_H	2.0			ns	
TTCI High Time	t_{PWH}	45%	50%	55%	t_{CYC}	
TTCI Low Time	t_{PWL}	45%	50%	55%	t_{CYC}	
TTCI Rise Time (10% - 90%)	t_R			4.0	ns	
Set-up - TTDI, TSPEI or TSYNI to ↑ TTCI	t_{SU}	4.0			ns	

Figure 31. Parallel SONET Input Timing



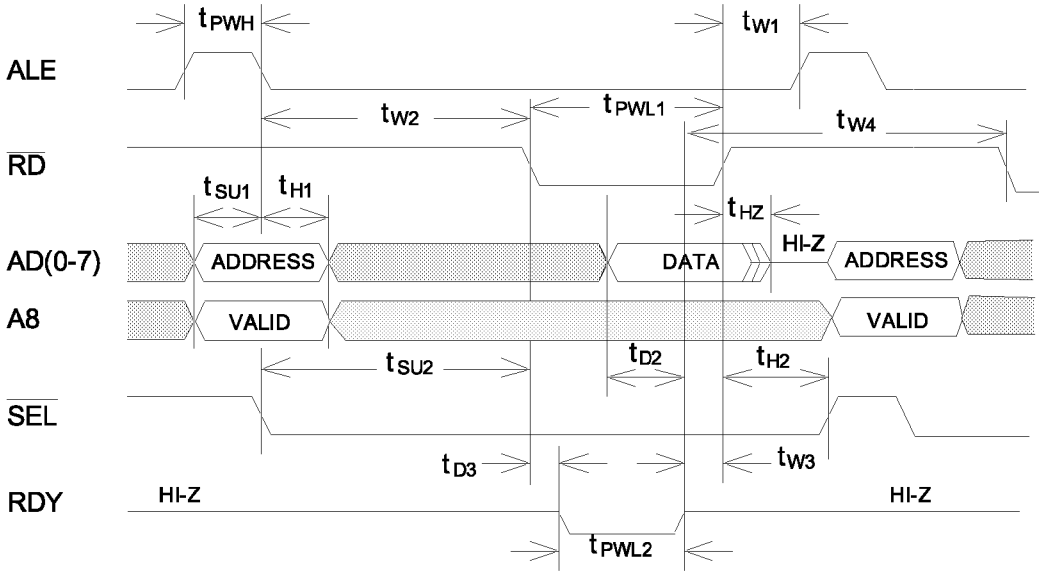
Parameter	Symbol	Min	Typ	Max	Unit	Notes
TPCI Period	t_{CYC}	154.0	154.3	154.6	ns	
TPCI Fall Time (90% - 10%)	t_F			6.0	ns	
Hold - TPDI(0-7), TSPEI or TSYNI after ↑ TPCI	t_H	3.0			ns	1
TPCI High Time	t_{PWH}	45%	50%	55%	t_{CYC}	
TPCI Low Time	t_{PWL}	45%	50%	55%	t_{CYC}	
TPCI Rise Time (10% - 90%)	t_R			6.0	ns	
Set-up - TTDI, TSPEI or TSYNI to ↑ TPCI	t_{SU}	7.0			ns	1

Note 1: Sampling occurs on Falling Edge of TPCI (dotted line) when INVPCK = "1".

MICROPROCESSOR INTERFACE TIMING

Figures 32 and 33 present the μPro Interface timing requirements.

Figure 32. Microprocessor Read Timing



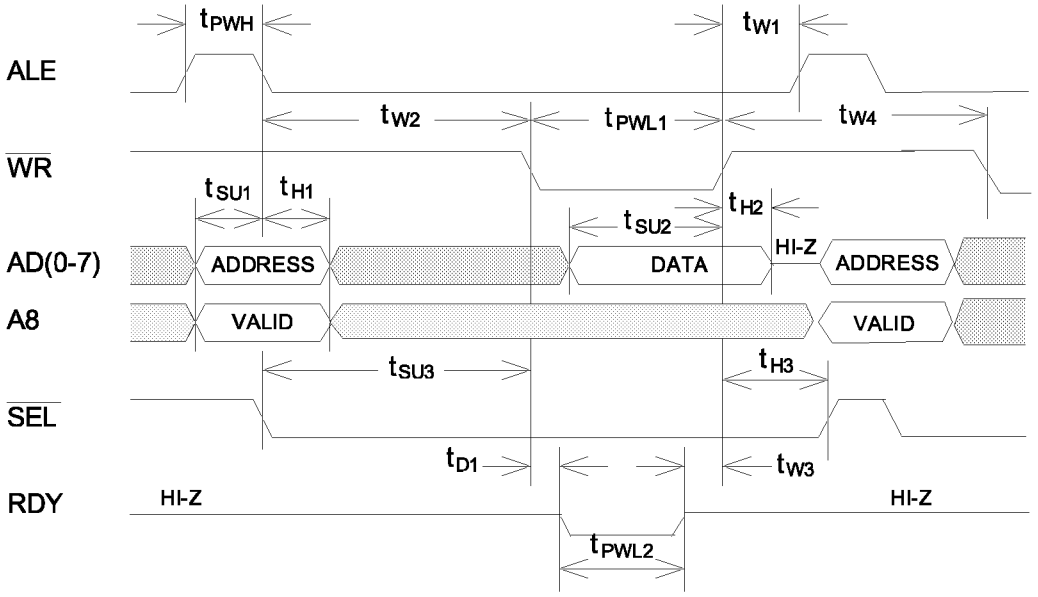
Parameter	Symbol	Min	Typ	Max	Unit	Notes
Delay - Data valid to ↑ RDY	t_{D2}	0.0	20		ns	1
Delay - ↓ RDY after ↓ $\overline{RD}$	t_{D3}	2.0		15	ns	1
Hold - Address after ↓ ALE	t_{H1}	3.0			ns	
Hold - ↑ $\overline{SEL}$ after ↑ $\overline{RD}$	t_{H2}	0.0			ns	
Delay - ↑ $\overline{RD}$ to AD(0-7) = HI-Z	t_{HZ}	2.0		7.0	ns	1
ALE High Time	t_{PWH}	20			ns	
$\overline{RD}$ Low Time	t_{PWL1}	40			ns	2
RDY Low Time	t_{PWL2}	0.0		1220	ns	1, 4, 5, 6
Set-up - Address to ↓ ALE	t_{SU1}	7.0			ns	
Set-up - ↓ $\overline{SEL}$ to ↓ $\overline{RD}$	t_{SU2}	0.0			ns	
Wait - ↑ ALE after ↑ $\overline{RD}$	t_{W1}	0.0			ns	
Wait - ↓ $\overline{RD}$ after ↓ ALE	t_{W2}	0.0			ns	
Wait - ↑ RDY to ↑ $\overline{RD}$	t_{W3}	0.0			ns	
Wait - ↑ RDY to ↓ $\overline{WR}$ or ↓ $\overline{RD}$	t_{W4}	325			ns	3, 5, 6

Notes:

1. With 75 pF Load.
2. Or time RDY is low - whichever is greater.
3. Minimum t_{w4} = 325 ns[5] from ↑ RDY of two-byte read* to ↓ $\overline{RD}$ of next read of a different address, or
   10 ns from ↑ RDY of any other case of read of ↓ $\overline{WR}$ or ↓ $\overline{RD}$.
   The minimum value shown for t_{w4} is the worse case of these two situations.
4. Maximum t_{PWL2} = 600 ns[5] + max of: (0 ns), or
   (65 ns) - (time since ↑ RDY of last two-byte read* to same address), or
   (310 ns) - (time since ↑ $\overline{WR}$ of last one-byte write to same address), or
   (620 ns) - (time since ↑ $\overline{WR}$ of last two-byte write* to same address).
   The maximum value shown for t_{PWL2} is the worst case of these four situations.
5. Increase time by 200 ns for SPE mode with evenly spaced gaps, or by 775 ns if gaps are grouped together in a row.
6. All references to edges of $\overline{RD}$ or $\overline{WR}$ for access times or wait times between accesses are understood to be with $\overline{SEL}$ = "0", which selects this device.

* Two-byte read/write is a read or write of the low byte of a 16-bit counter when CNT16EN = "1".

Figure 33. Microprocessor Write Timing



Parameter	Symbol	Min	Typ	Max	Unit	Notes
Delay - ↓ $\overline{WR}$ to ↓ RDY	t_{D1}	2.0		15	ns	1
Hold - Address after ↓ ALE	t_{H1}	3.0			ns	
Hold - Data after ↑ $\overline{WR}$	t_{H2}	3.0			ns	
Hold - ↑ $\overline{SEL}$ after ↑ $\overline{WR}$	t_{H3}	0.0			ns	
ALE High Time	t_{PWH}	20			ns	
$\overline{WR}$ Low Time	t_{PWL1}	20			ns	2

Parameter	Symbol	Min	Typ	Max	Unit	Notes
RDY Low Time	t_{PWL2}	0.0		900	ns	1, 4, 5, 6
Set-up - Address to ↓ ALE	t_{SU1}	7.0			ns	
Set-up - Data to ↑ $\overline{WR}$	t_{SU2}	10			ns	
Set-up - ↓ $\overline{SEL}$ to ↓ $\overline{WR}$	t_{SU3}	0.0			ns	
Wait - ↑ ALE after ↑ $\overline{WR}$	t_{W1}	0.0			ns	
Wait - ↓ $\overline{WR}$ after ↓ ALE	t_{W2}	0.0			ns	
Wait - ↑ RDY to ↑ $\overline{WR}$	t_{W3}	0.0			ns	
Wait - ↑ $\overline{WR}$ to ↓ $\overline{WR}$ or ↓ $\overline{RD}$	t_{W4}	900			ns	3, 5, 6

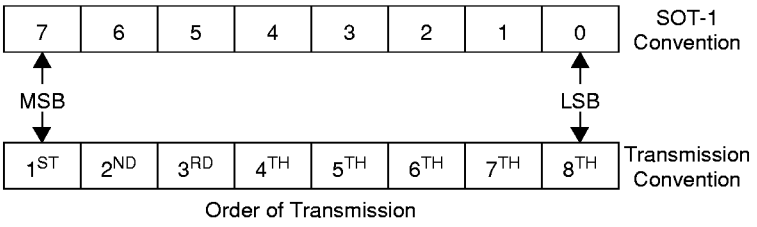
Notes:

1. With 75 pF Load.
2. Or time RDY is low - whichever is greater.
3. Minimum t_{w4} = 600 ns[5] from ↑ $\overline{WR}$ of one-byte write to ↓ $\overline{RD}$ of next read of a different address, or
   900 ns[5] from ↑ $\overline{WR}$ of two-byte write to ↓ $\overline{RD}$ of next read of a different address, or
   10 ns from ↑ $\overline{WR}$ of any other case of write to ↓ $\overline{WR}$ or ↓ $\overline{RD}$.
   The minimum value shown for t_{w4} is the worst case of these three situations.
4. Maximum t_{PWL2} = Max of: (0 ns), or
   (350 ns)[5] - (time since ↑ RDY of last two-byte read* to same address), or
   (900 ns)[5] - (time since ↑ $\overline{WR}$ of last two-byte write* to any address), or
   (600 ns)[5] - (time since ↑ $\overline{WR}$ of last one-byte write to any address).
   The maximum value shown for t_{PWL2} is the worst case of these four situations.
5. Increase time by 200 ns for SPE mode with evenly spaced gaps, or by 775 ns if gaps are grouped together in a row.
6. All references to edges of $\overline{RD}$ or $\overline{WR}$ for access times or wait times between accesses are understood to be with $\overline{SEL}$ = "0", which selects this device.

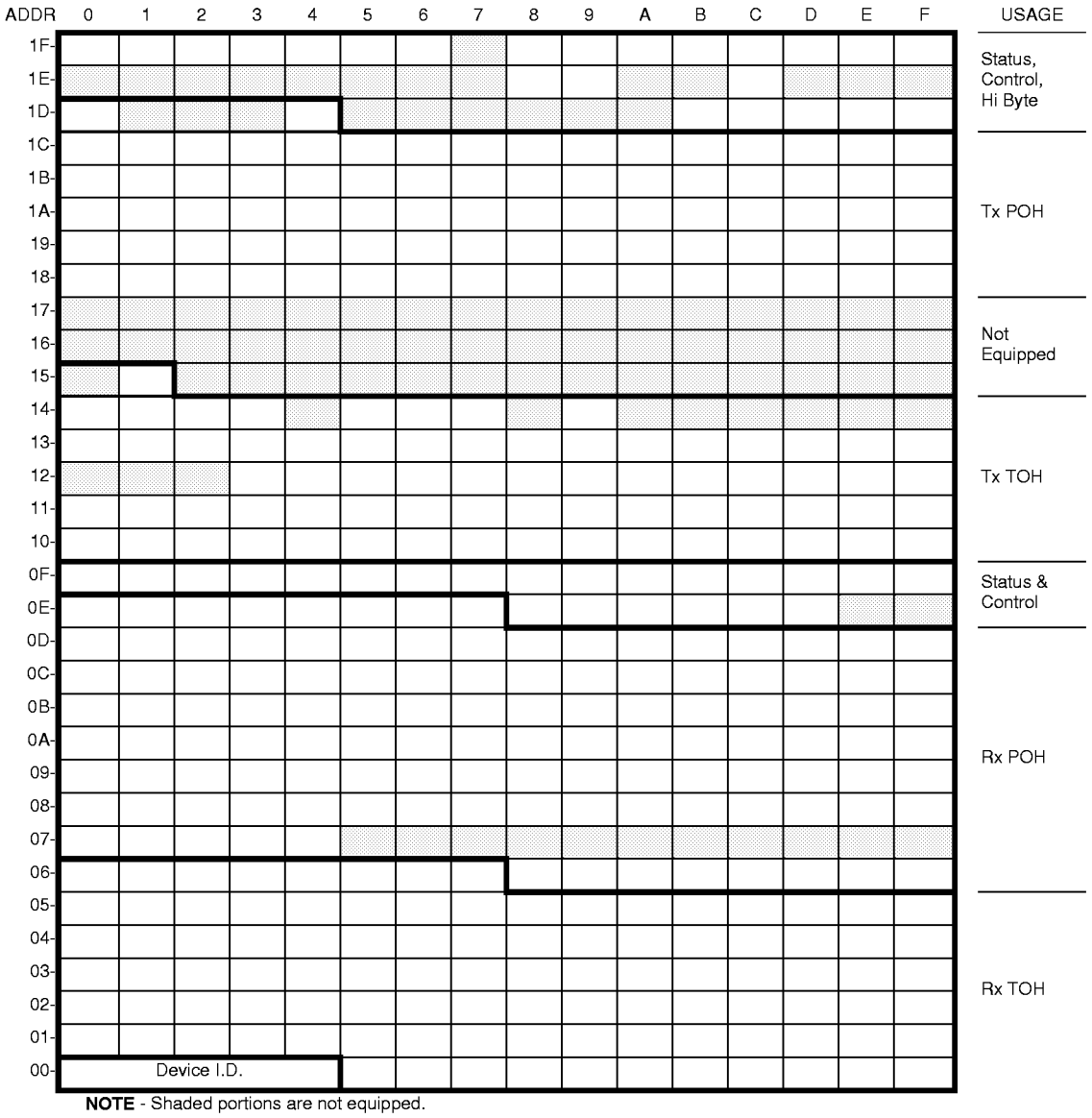
* Two-byte read/write is a read or write of the low byte of a 16-bit counter when CNT16EN = "1".

MEMORY MAP

All Addresses are given in Hex [H]. The bit position relationship between a Transmission Byte (e.g., C1) and the corresponding SOT-1 Memory Location is shown below.



The Memory Map is shown in Figure 34. Address values are row number followed by column number. Detailed explanations for the used byte locations are provided in the sections which follow.



NOTE - Shaded portions are not equipped.

Figure 34. Memory Map

DEVICE I.D. - Read Only

Address (Hex)	Status Bits	Control Bits	Description
000 - 004			**I.D. 0**: all "0" **I.D. 1**: all "0" **I.D. 2**: all "0" **I.D. 3**: all "0" **I.D. 4**: all "0"

Note: Status and Control Bit locations can be found on pages 55 and 61.

RX TOH BYTES - Read/Write

Address (Hex)	Status Bits	Control Bits	Description
005 - 007		OA	**Rx Line D1-D3:** Section DCC Bytes - The D1-D3 Bytes are also output as a single 192 kb/s channel at the Rx Section DCC Port. These bytes are also optionally available at the Rx OA/TOH Port. 005[H] = D1 and 007[H] = D3.
008 - 010		OA	**Rx Line D4-D12:** Line DCC Bytes - The D4-D12 Bytes are also output as a single 576 kb/s channel at the Rx Line DCC Port. These bytes are also optionally available at the Rx OA/TOH Port. 008[H] = D4 and 010[H] = D12.
011 & 012	RNPTR RLOP RAIS-P RCPTR	OA	**Rx Line H1 and H2:** Pointer Bytes - The H1 and H2 bytes are processed internally. These bytes are also optionally available at the Rx OA/TOH Port.
013		OA	**Rx Line H3:** Pointer Action Byte - This byte is also optionally available at the Rx OA/TOH Port.
014		STS1 OA	**Rx Line B1:** Section Parity Byte - If STS1 = "1", this byte contains BIP-8 Parity which is even parity over all bytes in the frame. If STS1 = "0", this byte contains Parity Error Information *where*: any "1"s indicate a BIP-8 Error in that Bit Position. Parity Errors are accumulated by the Rx B1 Error Counter. This byte is also optionally available at the Rx OA/TOH Port.
015		OA	**Rx Line B2:** Line BIP-8 Parity Byte - The Parity Calculation is even parity over all bytes in the frame except the 9 Section Overhead Bytes. Parity Errors are accumulated by the Rx B2 Error Counter. Additional processing is performed to develop an Excess B2 BER Alarm. This byte is also optionally available at the Rx OA/TOH Port.
016 & 017	RFE RSEF RLOF	OA	**Rx Line A1 and A2:** Framing Bytes - The expected pattern is F6[H] and 28[H] in the A1 and A2 Bytes, respectively. This byte is also optionally available at the Rx OA/TOH Port.

Address (Hex)	Status Bits	Control Bits	Description
018	RLE1	RE2A	**Rx Line E1:** Section Order Wire Byte - This byte can be optionally used for AIS communication between SOT-1s and is also available at the Rx OA/TOH Port.
019			**Rx Line E2:** Line Order Wire Byte - This byte is also available at the Rx OA/TOH Port.
01A		OA	**Rx Line Z1:** 1ST Growth Byte - This byte is debounced and stored in Location 05A[H]. This byte is also optionally available at the Rx OA/TOH Port.
01B		OA	**Rx Line Z2:** 2ND Growth Byte - This byte is debounced and stored in Location 05B[H]. Bits 5-8 (line Numbering) are interpreted as FEBE-L Information and Errors are accumulated by the FEBE-L Counter. This byte is also optionally available at the Rx OA/TOH Port.
01C	J0MIS	J0EN0 J0EN1 OA	**Rx Line C1:** STS-1 Number/J0 - This byte is debounced and stored in Location 05C[H]. If J0EN(1,0) = "00", no further Processing is performed. If J0EN(1,0) = "01", the received value is also compared to value in Location 067[H]. If J0EN1 = "1", the J0 message is internally stored and accessible through Locations 080[H] - 0BF[H]. This byte is also optionally available at the Rx OA/TOH Port.
01D		OA	**Rx Line F1:** Section User Byte - This byte is debounced and stored in Location 05D[H] and is also optionally available at the Rx OA/TOH Port.
01E & 01F	RAPS RAIS-L RRDI-L		**Rx Line K1 and K2:** APS Bytes - These bytes are debounced and stored in Locations 05E[H] and 05F[H], respectively. They are monitored for APS Channel Failure. K2 Byte, Bits 6-8 (Line Numbering) are monitored for AIS-L and RDI-L Alarms. These bytes are also available at the Rx OA/TOH Port.
020 & 021			**Internal Use**: Do not access.
022	LPJOF	$\overline{\text{RXRTM}}$ SPE RCLK RRAIS SRLAIS SRPAIS RSWRES	**Local PJ Cnt:** Count of all Positive and Negative Pointer Justifications that are created when Rx Re-timing is enabled. This is an 8 Bit, Clear on Read, Saturating Counter. Counting is inhibited upon declaration of RLOC, RLOS, RLOF, or RAIS-L, or if AIS-L or AIS-P is inserted at the Rx Terminal Port.
023 & 024			**Reserved:** For future use.

Address (Hex)	Status Bits	Control Bits	Description
025 - 027		SPE RRSD	**Rx Insert D1-D3:** Bytes to be multiplexed into Rx Terminal Port Data if insertion option is enabled *where*: 025[H] = D1 and 027[H] = D3.
028 - 030		SPE RRLD	**Rx Insert D4-D12:** Bytes to be multiplexed into Rx Terminal Port Data if insertion option is enabled *where*: 028[H] = D4 and 030[H] = D12.
031 & 032		SPE RRPTR	**Rx Insert H1 and H2:** Bytes to be multiplexed into Rx Terminal Port Data if insertion option is enabled. **WARNING**: This is for test purposes only. The Payload does not track the pointer value written in these locations.
033		SPE RCLK $\overline{\text{RXRTM}}$	**Rx Insert H3:** Rx Terminal Port Data H3 Byte value when Rx Re-timing is enabled and a Pointer Decrement is not performed.
034		SPE RRB1	**Rx Insert B1:** Internally generated B1 Value multiplexed into Rx Terminal Port Data if insertion option is enabled. The Parity Calculation is even parity over all bytes in the frame.
035		SPE RRB2	**Rx Insert B2:** Internally generated B2 Value multiplexed into Rx Terminal Port Data if insertion option is enabled. The Parity Calculation is even parity over all bytes in the frame except the 9 Section Overhead Bytes.
036 & 037		SPE RRFRM	**Rx Insert A1 and A2:** Internally generated A1 and A2 values multiplexed into Rx Terminal Port Data.
038		SPE RRE1 RA2E	**Rx Insert E1:** Byte to be multiplexed into Rx Terminal Port Data if insertion option is enabled. This byte can be optionally used for AIS communication between SOT-1s.
039		SPE RRE2	**Rx Insert E2:** Byte to be multiplexed into Rx Terminal Port Data if insertion option is enabled.
03A		SPE RRZ1	**Rx Insert Z1:** Byte to be multiplexed into Rx Terminal Port Data if insertion option is enabled.
03B		SPE RRZ2	**Rx Insert Z2:** Byte to be multiplexed into Rx Terminal Port Data if insertion option is enabled.
03C		SPE RRC1	**Rx Insert C1:** Byte to be multiplexed into Rx Terminal Port Data if insertion option is enabled.
03D		SPE RRF1	**Rx Insert F1:** Byte to be multiplexed into Rx Terminal Port Data if insertion option is enabled.
03E & 03F		SPE RRAPS	**Rx Insert K1 and K2:** Bytes to be multiplexed into Rx Terminal Port Data if insertion option is enabled.

Address (Hex)	Status Bits	Control Bits	Description
040	RLFEBEOF	RSWRES CNT16EN DISRLAL	**FEBE-L Cnt:** Count of FEBE-L Errors that are incoming on the Rx Line. This is an 8 or 16 Bit, Clear on Read, Saturating Counter. In 8 Bit Mode, the total counter value is available at this location. In 16 Bit Mode, this location is the Lower Order 8 Bits. The Higher Order 8 Bits are readable in Location 1FF[H]. The Lower Order Byte must be Read first in 16 Bit Mode. Counting is inhibited upon declaration of RLOC, RLOS, RLOF, or RAIS-L or by DISRLAL.
041 - 043			**Internal Use:** Do not access.
044	RPJOF	RSWRES	**Rx PJ Cnt:** Count of all Positive and Negative Pointer Justifications that are in-coming on the Rx Line. This is an 8 Bit, Clear on Read, Saturating Counter. Counting is inhibited upon declaration of RLOC, RLOS, RLOF or RAIS-L.
045	RPMOVOF	RSWRES	**Rx Inc Cnt/Dec Cnt:** Two - 4 Bit Counters. Bits 7-4 accumulate Pointer Increments incoming on the Rx Line. Bits 3-0 accumulate Pointer Decrements incoming on the Rx Line. Both Counters are Saturating and Clear on Read. Counting is inhibited upon declaration of RLOC, RLOS, RLOF or RAIS-L.
046	RB1COF	RSWRES CNT16EN DISRLAL	**Rx B1 Err Cnt:** Count of B1 Errors that are incoming on the Rx Line. This is an 8 or 16 Bit, Clear on Read, Saturating Counter. In 8 Bit Mode, the total counter value is available at this location. In 16 Bit Mode, this location is the Lower Order 8 Bits. The Higher Order 8 Bits are readable in Location 1FF[H]. The Lower Order Byte must be Read first in 16 Bit Mode. Counting is inhibited upon declaration of RLOC, RLOS, or RLOF or by DISRLAL.
047	RB2COF	RSWRES CNT16EN DISRLAL	**Rx B2 Err Cnt:** Count of B2 Errors that are incoming on the Rx Line. This is an 8 or 16 Bit, Clear on Read, Saturating Counter. In 8 Bit Mode, the total counter value is available at this location. In 16 Bit Mode, this location is the Lower Order 8 Bits. The Higher Order 8 Bits are readable in Location 1FF[H]. The Lower Order Byte must be Read first in 16 Bit Mode. Counting is inhibited upon declaration of RLOC, RLOS, RLOF, or RAIS-L or by DISRLAL.
048			**Internal Use:** Do not access.
049			**Rx B1 Err Mask:** The contents of this location are exclusive-OR gated, bit by bit, with the B1 Byte output at the Rx Terminal Port.
04A - 04F			**Frm-1 (Z1, Z2, C1, F1, K1, K2):** Respective bytes received in the previous frame *where*: 04A[H] = Frm-1 Z1 and 04F[H] = Frm-1 K2.
050			**Internal Use:** Do not access.
051			**Rx B2 Err Mask:** The contents of this location are exclusive-OR gated, bit by bit, with the B2 Byte output at the Rx Terminal Port.

<table>
<tr><th>Address (Hex)</th><th>Status Bits</th><th>Control Bits</th><th>Description</th></tr>
<tr><td>052
-
057</td><td></td><td></td><td>Frm-2 (Z1, Z2, C1, F1, K1, K2): Respective bytes received two frames earlier where: 052[H] = Frm-2 Z1 and 057[H] = Frm-2 K2.</td></tr>
<tr><td>058
&
059</td><td></td><td></td><td>Internal Use: Do not access.</td></tr>
<tr><td>05A
-
05F</td><td>RTNEW</td><td></td><td>Debounced (Z1, Z2, C1, F1, K1, K2): Respective debounced bytes where:05A[H] = Debounced Z1 and 05F[H] = Debounced K2. Any byte that is received with a New Value, and that New Value is constant for three consecutive frames, will cause the New Value to be written to these locations. The algorithm is illustrated below where:

F and F+k = Frame Numbers in an arbitrary sequence of consecutive frames
N = a Z1, Z2, C1, F1, K1 or K2 Byte Location
X, Y, and Z = Received Values of the N Byte

Rx Frame Number
<table>
<tr><th>Parameter</th><th>F</th><th>F+1</th><th>F+2</th><th>F+3</th><th>F+4</th><th>F+5</th></tr>
<tr><td>Rx Line N</td><td>X</td><td>Y</td><td>X</td><td>Z</td><td>Z</td><td>Z</td></tr>
<tr><td>Frm-1 N</td><td>X</td><td>X</td><td>Y</td><td>X</td><td>Z</td><td>Z</td></tr>
<tr><td>Frm-2 N</td><td>X</td><td>X</td><td>X</td><td>Y</td><td>X</td><td>Z</td></tr>
<tr><td>Deboun. N</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>Z</td></tr>
<tr><td>RTNEW</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td></tr>
</table></td></tr>
<tr><td>060</td><td rowspan="5">B2EBER</td><td rowspan="5">B2RATE0
B2RATE1
B2RATE2</td><td>B2 Multiplier (B2M): See Table 6 (page 113) for B2EBER Parameter settings. Bits 4-7 are not used.</td></tr>
<tr><td>061</td><td>B2WIN: See Table 6 (page 113) for B2EBER Parameter settings.</td></tr>
<tr><td>062</td><td>B2CCV/B2SCV: Bits 0-3 are the B2CCV Parameter. Bits 4-7 are the B2SCV Parameter. See Table 6 (page 113) for B2EBER Parameter settings.</td></tr>
<tr><td>063</td><td>B2 Set (B2SET): See Table 6 (page 113) for B2EBER Parameter settings.</td></tr>
<tr><td>064</td><td>B2 Clear (B2CLR): See Table 6 (page 113) for B2EBER Parameter settings.</td></tr>
<tr><td>065
&
066</td><td></td><td></td><td>Internal Use: Do not access.</td></tr>
<tr><td>067</td><td></td><td></td><td>J0 Expect: Value with which Rx Line C1 Location is compared for Single Byte J0 Processing.</td></tr>
</table>

RX POH BYTES - Read/Write

Address (Hex)	Status Bits	Control Bits	Description
068	B3EBER	B3RATE0 B3RATE1 B3RATE2	**B3 Multiplier (B3M)**: See Table 11 (page 117) for B3EBER Parameter settings. Bits 4-7 are not used.
069			**B3WIN**: See Table 11 (page 117) for B3EBER Parameter settings.
06A			**B3CCV/B3SCV**: Bits 0-3 are the B3CCV Parameter. Bits 4-7 are the B3SCV Parameter. See Table 11 (page 117) for B3EBER Parameter settings.
06B			**B3 Set (B3SET)**: See Table 11 (page 117) for B3EBER Parameter settings.
06C			**B3 Clear (B3CLR)**: See Table 11 (page 117) for B3EBER Parameter settings.
06D & 06E			**Internal Use:** Do not access.
06F			**Reserved**: For future use.
070 - 072			**Internal Use:** Do not access.
073 & 074			**Reserved**: For future use.
075 - 07F			NOT EQUIPPED
080 - 0BF		J0WREN J0EN0 J0EN1 J0SYNC	**Rx Line J0/J1**: Line or Path Trace Bytes - Multiple byte J0 messages and the J1 Bytes are accessed at these locations. These locations are only used for J0 Messages if J0EN1 = "1". If J0SYNCEN = "1" or J0EN(1,0) = "11", the byte immediately following an ASCII <CR> and <LF>, of the appropriate message, will be stored in Location 080[H]. The Rx Line J1 Bytes are always output at the Rx Terminal Port.
0C0			**Rx Line B3**: Path BIP-8 Parity Byte - The Parity Calculation is even parity over all SPE Bytes (the 27 TOH Bytes are excluded). Parity Errors are accumulated by the Rx B3 Error Counter. Additional processing is performed to develop an Excess B3 BER Alarm.
0C1	C2MIS C2UNEQ RPDI-P		**Rx Line C2**: Path Signal Label Byte - This byte is debounced and stored in Location 0D1[H]. Additional processing is performed to develop Mismatch, Unequipped and Path Defect Indications.

Address (Hex)	Status Bits	Control Bits	Description
0C2	RRDI-P RRDI-PSD RRDI-PCD RRDI-PPD	PRDISEL	**Rx Line G1**: Path Status Byte - Bits 1-4 (Line Numbering) are processed for FEBE-P information and the Errors are accumulated by the FEBE-P Counter. Bits 5, 6, and 7 (Line Numbering) are processed as the RDI-P Alarm, either for Single Bit RDI-P or for Three Bit RDI-P applications.
0C3			**Rx Line F2**: Path User Channel Byte - This byte is debounced and stored in Location 0D3[H].
0C4	RLOM	H4INT	**Rx Line H4**: Multiframe Indicator Byte - Bits 7 and 8 (Line Numbering) are optionally used to synchronize an internal, 2 Bit, Modulo 4, Rx Multiframe Counter for VT structured payloads. Bits 1-6 (Line Numbering) are not processed.
0C5 - 0C7			**Rx Line (Z3, Z4 and Z5)**: 3^{RD}, 4^{TH} and 5^{TH} Growth Bytes - These bytes are debounced and stored in Locations 0D5[H], 0D6[H], and 0D7[H], respectively. OC5[H] = Z3 and 0C7[H] = Z5.
0C8		RPATH	**Rx Insert B3**: Internally generated B3 value multiplexed into Rx Terminal Port Data if insertion option is enabled. The Parity Calculation is even parity over all SPE Bytes (the 27 TOH Bytes are excluded).
0C9		RPATH	**Rx Insert C2**: Byte to be multiplexed into Rx Terminal Port Data if insertion option is enabled.
0CA		RPATH	**Rx Insert G1**: Byte to be multiplexed into Rx Terminal Port Data if insertion option is enabled.
0CB		RPATH	**Rx Insert F2**: Byte to be multiplexed into Rx Terminal Port Data if insertion option is enabled.
0CC			**Internal Use**: Do not access.
0CD - 0CF		RPATH	**Rx Insert (Z3, Z4 and Z5)**: Bytes to be multiplexed into Rx Terminal Port Data if insertion option is enabled *where*: OCD[H] = Z3 and 0CF[H] = Z5.
0D0			**Rx B3 Err Mask**: The contents of this location are exclusive-OR gated, bit by bit, with the B3 Byte output at the Rx Terminal Port.
0D1	RPNEW		**Debounced C2**: The Debounce Algorithm is the same as that used for TOH Debouncing.
0D2	RPFEBEOF	RSWRES CNT16EN	**FEBE-P Cnt**: Count of FEBE-P Errors that are incoming on the Rx Line. This is an 8 or 16 Bit, Clear on Read, Saturating Counter. In 8 Bit Mode, the total counter value is available at this location. In 16 Bit Mode, this location is the Lower Order 8 Bits. The Higher Order 8 Bits are readable in Location 1FF[H]. The Lower Order Byte must be Read first in 16 Bit Mode. Counting is inhibited upon declaration of RLOC, RLOS, RLOF, RAIS-L, RLOP or RAIS-P.
0D3	RPNEW		**Debounced F2**: The Debounce Algorithm is the same as that used for TOH Debouncing.

Address (Hex)	Status Bits	Control Bits	Description
0D4	RB3COF	RSWRES CNT16EN	**Rx B3 Err Cnt**: Count of B3 Errors that are incoming on the Rx Line. This is an 8 or 16 Bit, Clear on Read, Saturating Counter. In 8 Bit Mode, the total counter value is available at this location. In 16 Bit Mode, this location is the Lower Order 8 Bits. The Higher Order 8 Bits are readable in Location 1FF[H]. The Lower Order Byte must be Read first in 16 Bit Mode. Counting is inhibited upon declaration of RLOC, RLOS, RLOF, RAIS-L, RLOP or RAIS-P.
0D5 - 0D7	RPNEW		**Debounced (Z3, Z4 and Z5)**: *where*: OD5[H] = Z3 and 0D7[H] = Z5. The Debounce Algorithm is the same as that used for TOH Debouncing.
0D8			**Internal Use**: Do not access.
0D9			**FRM-1 C2**: C2 Byte received in the previous frame.
0DA			**Internal Use**: Do not access.
0DB			**FRM-1 F2**: F2 Byte received in the previous frame.
0DC			**Internal Use**: Do not access.
0DD - 0DF			**Frm-1 (Z3, Z4 and Z5)**: Respective bytes received in the previous frame *where*: 0DD[H] = Frm-1 Z3 and 0DF[H] = Frm-1 Z5.
0E0			**Internal Use**: Do not access.
0E1			**FRM-2 C2**: C2 Byte received two frames earlier.
0E2			**Internal Use**: Do not access.
0E3			**FRM-2 F2**: F2 Byte received two frames earlier.
0E4			**C2 Expect**: Value with which Rx Line C2 Location is compared for Signal Label Mismatch.
0E5 - 0E7			**Frm-2 (Z3, Z4 and Z5)**: Respective bytes received two frames earlier *where*: 0E5[H] = Frm-2 Z3 and 0E7[H] = Frm-2 Z5.

STATUS AND CONTROL REGISTERS (0E8[H]-0FF[H]) - Read/Write

Address [H]	Name[1]	Mode[2]	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0E8	SR3[3]	R	RLFRI	RFE	B2EBER	B3EBER	RCPTR	C2MIS	C2UNEQ	RLOM
0E9	SR3	R/W	Same as 0E8[H] except does not reset on Read. Write "1" to reset individual bits to "0".							
0EA	SR6[3]	R	RRDI-PSD	RRDI-PCD	RRDI-PPD	RPDI-P	J0MIS	Unused		
0EB	SR6	R/W	Same as 0EA[H] except does not reset on Read. Write "1" to reset individual bits to "0".							
0EC	SR3	R	Same as 0E8[H] except unlatched values.							
0ED	SR6	R	Same as 0EA[H] except unlatched values.							
0EE & 0EF			NOT EQUIPPED							
0F0	SR0[3]	R	RLOC	RNPTR	RAIS-P	RAIS-L	RLOP	RLOF	RSEF	RLOS
0F1	SR0	R/W	Same as 0F0[H] except does not reset on Read. Write "1" to reset individual bits to "0".							
0F2	SR1[3]	R	INT	RTNEW	RPNEW	RRDI-P	RRDI-L	RAPS	Unused	
0F3	SR1	R/W	Same as 0F2[H] except does not reset on Read. Write "1" to reset individual bits.							
0F4	SR0	R	Same as 0F0[H] except unlatched values.							
0F5	SR1	R	Same as 0F2[H] except unlatched values.							
0F6	SR7[4]	R	RB3COF	RB2COF	RB1COF	RPFEBEOF	RLFEBEOF	RPMOVOF	RPJOF	LPJOF
0F7	SR9[4]	R	REG0	REG1	REG3	REG6	REG2	REG4	REG5	REG78
0F8	CR0	R/W	RRSD	RRLD	RRE1	RRE2	RPATH	RRAPS	RRPTR	TRLOOP
0F9	CR1	R/W	RRF1	RRC1	RRZ1	RRZ2	RRAIS	LTE	RRFRM	RRB1
0FA	CR2	R/W	STS1	PARA	HWINE	TRLRDI	ALTOW	TIEN	PIEN	-VE
0FB	CR3	R/W	RRFIEN	RFREN	RRFIFO	Unused[5]	DISRLAL	CNT16EN	RSWRES	Unused[5]
0FC	CR4	R/W	SRLAIS	B2XAIS	SRPAIS	B3XPAIS	RLOMPAIS	C2MPAIS	C2UPAIS	RLEAIS
0FD	CR5	R/W	DIEN	Unused[5]			INVPCK	Unused[5]		INVINT
0FE	CR6	R/W	Reserved[5]	RAMTSTEN	H4INT	J1SYNCEN	S1	S0	C1J1EN	OA
0FF	CR16	R/W	Unused[5]	PRDISEL	B2RATE2	B2RATE1	B2RATE0	B3RATE2	B3RATE1	B3RATE0

Notes:
1. SR = Status Register, CR = Control Register. See the detailed descriptions provided in the following tables (starting on page 62).
2. R = Read Only, R/W = Read/Write
3. Resets to all "0"s when Read
4. Unlatched values only
5. All Unused and Reserved control bits are to be written to "0".

TX TOH BYTES - Read/Write

Address (Hex)	Status Bits	Control Bits	Description
100 - 104			**Reserved**: For future use.
105 - 110		SPE	**Tx Term D1-D12**: Information incoming at the Tx Terminal Port *where*: 105[H] = D1 and 110[H] = D12.
111 & 112	TNPTR TLOP TAIS-P TCPTR	SPE C1J1EN	**Tx Term H1 and H2**: Information incoming at the Tx Terminal Port. These bytes are optionally internally processed as Pointer Bytes.
113		SPE	**Tx Term H3**: Information incoming at the Tx Terminal Port.
114		SPE	**Tx Term B1**: Information incoming at the Tx Terminal Port. This byte is optionally processed as a B1 Parity Byte with Parity Errors accumulated by the Tx B1 Error Counter. The Parity Calculation is even parity over all bytes in the frame.
115		SPE	**Tx Term B2**: Information incoming at the Tx Terminal Port. This byte is optionally processed as a B2 Parity Byte with Parity Errors accumulated by the Tx B2 Error Counter. The Parity Calculation is even parity over all bytes in the frame except the 9 Section Overhead Bytes.
116 & 117	TFE TSEF TLOF	SPE C1J1EN	**Tx Term A1 and A2**: Information incoming at the Tx Terminal Port. These bytes are optionally processed as Framing Bytes.
118	TTE1	SPE TE2A	**Tx Term E1**: Information incoming at the Tx Terminal Port. This byte can be optionally used for AIS communication between SOT-1 (TXC-03001 or TXC-03001B), SOT-1E or SOT-3 devices.
119 - 11F	TAIS-L	SPE	**Tx Term E2, Z1, Z2, C1, F1, K1 and K2**: Information incoming at the Tx Terminal Port *where*: 119[H] = E2 and 11F[H] = K2.
120 - 122			NOT EQUIPPED
123 & 124			**Internal Use**: Do not access.
125 - 127		TRSD TXSDEXT SDCCEN OA	**Tx Insert D1-D3**: Section DCC Bytes - Information to be multiplexed into Tx Line Port Data if insertion option is enabled. 125[H] = D1 and 127[H] = D3. These locations may be written by the µPro, or they may contain information input at the Tx Section DCC Port or optionally at the Tx OA/TOH Port.

Address (Hex)	Status Bits	Control Bits	Description
128 - 130		TRLD TXLDEXT LDCCEN OA	**Tx Insert D4-D12**: Line DCC Bytes - Information to be multiplexed into Tx Line Port Data if insertion option is enabled. 128[H] = D4 and 130[H] = D12. These locations may be written by the µPro, or they may contain information input at the Tx Section DCC Port or optionally at the Tx OA/TOH Port.
131 & 132			**Reserved**: For future use.
133		C1J1EN TXRTM	**Tx Insert H3**: Pointer Action Byte - Tx Line Port H3 Byte value when Tx Re-timing is enabled and a Pointer Decrement is not performed. This Location can only be accessed by the µPro.
134			**Internal Use**: Do not access.
135			**Internal Use**: Do not access.
136 & 137		TRFRM TFRMEXT OA	**Tx Insert A1 and A2**: Framing Bytes - Information to be multiplexed into Tx Line Port Data if insertion option is enabled. These locations may be written by the µPro, or they may contain the internally generated values, or they may optionally contain information input at the Tx OA/TOH Port.
138		TRE1 TXE1EXT	**Tx Insert E1**: Section Order Wire Byte - Information to be multiplexed into Tx Line Port Data if insertion option is enabled. This location may be written by the µPro or it may contain information input at the Tx OA/TOH Port.
139		TRE2 TXE2EXT	**Tx Insert E2**: Line Order Wire Byte - Information to be multiplexed into Tx Line Port Data if insertion option is enabled. This location may be written by the µPro or it may contain information input at the Tx OA/TOH Port.
13A		TRZ1 TXZ1EXT OA	**Tx Insert Z1**: 1^{ST} Growth Byte - Information to be multiplexed into Tx Line Port Data if insertion option is enabled. This location may be written by the µPro or it may optionally contain information input at the Tx OA/TOH Port.
13B		TRZ2 TXZ2EXT OA TLFEBEEN	**Tx Insert Z2**: 2^{ND} Growth Byte - Information to be multiplexed into Tx Line Port Data if insertion option is enabled. This location may be written by the µPro or it may optionally contain information input at the Tx OA/TOH Port. If the Line FEBE option is enabled, Bits 5-8 (Line Numbering) will be overwritten by the FEBE-L Value.
13C		J0EN1 TRC1 TXC1EXT OA	**Tx Insert C1**: C1 Byte/Single Byte J0 - Information to be multiplexed into Tx Line Port Data if insertion option is enabled. This location may be written by the µPro or it may optionally contain information input at the Tx OA/TOH Port.

Address (Hex)	Status Bits	Control Bits	Description
13D		TRF1 TXF1EXT OA	**Tx Insert F1**: Section User Byte - Information to be multiplexed into Tx Line Port Data if insertion option is enabled. This location may be written by the µPro or it may optionally contain information input at the Tx OA/TOH Port.
13E & 13F		TRAPS EXAPS TRLRDI	**Tx Insert K1 and K2**: APS Bytes - Information to be multiplexed into Tx Line Port Data if insertion option is enabled. These locations may be written by the µPro or they may contain information input at the Tx OA/TOH Port.
140 - 143			**Internal Use**: Do not access.
144			NOT EQUIPPED
145	TPMOVOF	C1J1EN TSWRES	**Tx Inc/Dec Cnt**: Two - 4 Bit Counters. Bits 7-4 = accumulate Pointer Increments incoming at the Tx Terminal Port. Bits 3-0 accumulate Pointer Decrements incoming at the Tx Terminal Port. Both Counters are Saturating and Clear on Read. Counting is inhibited upon declaration of TLOC, TLOS, TLOF, or TAIS-L, or by C1J1EN.
146	TB1COF	TSWRES INHTB1C	**Tx B1 Err Cnt**: Count of B1 Errors that are incoming at the Tx Terminal Port. This is an 8 Bit, Clear on Read, Rollover Counter. Counting is inhibited upon declaration of TLOC, TLOS, or TLOF, or by INHTB1C.
147	TB2COF	TSWRES INHTB2C	**Tx B2 Err Cnt**: Count of B2 Errors that are incoming at the Tx Terminal Port. This is an 8 Bit, Clear on Read, Rollover Counter. Counting is inhibited upon declaration of TLOC, TLOS, TLOF, or TAIS-L or by INHTB2C.
148			NOT EQUIPPED
149		TRERR	**Tx B1 Err Mask**: The contents of this location are exclusive-OR gated, bit by bit, with the B1 Byte output at the Tx Line Port.
14A - 150			NOT EQUIPPED
151		TRERR	**Tx B2 Err Mask**: The contents of this location are exclusive-OR gated, bit by bit, with the B2 Byte output at the Tx Line Port.
152 - 17F			NOT EQUIPPED

TX POH BYTES - Read/Write

Address (Hex)	Status Bits	Control Bits	Description
180 - 1BF		J0WREN J0EN0 J0EN1 TRC1 TXC1EXT OA TPATH J1SYNCEN	**Tx Insert J0/J1**: Line or Path Trace Bytes - Information to be multiplexed into Tx Line Port Data if insertion option is enabled, or external data input at Tx OA/TOH or Tx Terminal Port. J0 Processing These locations are only used for J0 Messages if J0EN1 = "1". They may be written by the µPro or they may optionally contain information input at the Tx OA/TOH Port. If the Tx OA/TOH Port option is enabled and J0EN(1,0) = "11", the byte immediately following an ASCII <CR> and <LF> will be stored in Location 180[H]. J1 Processing The information in these locations is written by the µPro or input at the Tx Terminal Port. If the Tx Terminal Port option is enabled (TPATH = "0") and J1SYNCEN = "1", the byte immediately following an ASCII <CR> and <LF> will be stored in Location 180[H].
1C0			**Tx Term B3**: Information incoming at the Tx Terminal Port. This byte is optionally processed as a B3 Parity Byte with Parity Errors accumulated by the Tx B3 Error Counter. The Parity Calculation is even parity over all SPE Bytes (the 27 TOH Bytes are excluded).
1C1 - 1C7			**Tx Term C2, G1, F2, H4, Z3, Z4 and Z5**: Information incoming at the Tx Terminal Port *where*: 1C1[H] = C2 and 1C7[H] = Z5.
1C8			**Internal Use:** Do Not Access
1C9		TPATH	**Tx Insert C2**: Signal Label Byte - µPro information to be multiplexed into Tx Line Port Data if insertion option is enabled.
1CA		TPATH TPFEBEEN TPRDIEN	**Tx Insert G1**: Path Status Byte - µPro information to be multiplexed into Tx Line Port Data if insertion option is enabled. Bits 1-4 and/or Bits 5, 6 and 7 (Line Numbering) may be overwritten by FEBE-P and/or RDI-P information.
1CB		TPATH	**Tx Insert F2**: Path User Byte - µPro information to be multiplexed into Tx Line Port Data if insertion option is enabled.
1CC		TPATH H4INT TXH4INS	**Tx Insert H4**: Multiframe Indicator Byte - µPro information to be multiplexed into Tx Line Port Data if insertion option is enabled. Bits 7 and 8 (Line Numbering) may be overwritten by the internal, 2 Bit, Modulo 4, Tx Multiframe Counter.
1CD - 1CF		TPATH	**Tx Insert (Z3, Z4 and Z5)**: 3^{RD}, 4^{TH} and 5^{TH} Growth Bytes - µPro information to be multiplexed into Tx Line Port Data if insertion option is enabled *where*: 1CD[H] = Z3, and 1CF[H] = Z5.

Address (Hex)	Status Bits	Control Bits	Description
1D0		TRERR	**Tx B3 Err Mask**: The contents of this location are exclusive-OR gated, bit by bit, with the B3 Byte output at the Tx Line Port. If the B3 byte is not internally calculated then twice the number of errors will be generated. See Table 19 (page 129).
1D1 - 1D3			NOT EQUIPPED
1D4		TSWRES TPATH	**Tx B3 Err Cnt**: Count of B3 Errors that are incoming at the Tx Terminal Port. This is an 8 Bit, Clear on Read, Rollover Counter. Counting is inhibited upon declaration of TLOC, TLOS, TLOF, TAIS-L, TAIS-P, or TLOP or if TPATH = "1".
1D5 - 1DA			NOT EQUIPPED

STATUS AND CONTROL REGISTERS (1DB[H]-1FF[H]) - Read/Write

Address [H]	Name[1]	Mode[2]	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1DB	CR19	R/W	Reserved[5]		TPRDISD	TPRDICD	TPRDIPD	B3PRDISD	B3PRDICD	TOHPRDISD
1DC	CR18	R/W	J0RWEN	J0MLRDI	J0MLAIS	J0EN1	J0EN0	Unused[5]		CHPRES
1DD	CR17	R/W	SDCCEN	LDCCEN	STLAIS	TEST1	TEST2	LINLOOP	DISTB2R	TPRDI20
1DE	CR7	R/W	TIDL	IDLSEL	TPFEBEEN	TPRDIEN	C2MPRDI	C2UPRDI	Reserved[5]	
1DF	CR15	R/W	TXLDEXT	TSWRES	TTEAIS	TLFEBEEN	INHTB1C	INHTB2C	STLRDI	B2ELRDI
1E0 - 1E7			NOT EQUIPPED							
1E8	SR5[3]	R	Unused	TFE	TCPTR	TTE1	TRCOFA	Unused	LOTR	TFIFOE
1E9	SR5	R/W	Same as 1E8[H] except does not reset on Read. Write "1" to reset individual bits to "0".							
1EA & 1EB			NOT EQUIPPED							
1EC	SR5	R	Same as 1E8[H] except unlatched values.							
1ED - 1EF			NOT EQUIPPED							
1F0	SR2[3]	R	TLOC	TNPTR	TAIS-P	TAIS-L	TLOP	TLOF	TSEF	TLOS
1F1	SR2	R/W	Same as 1F0[H] except does not reset on Read. Write "1" to reset individual bits to "0".							
1F2	SR4[3]	R	RRCOFA	LORR	RFIFOE	RLE1	TAISV	Unused		
1F3	SR4	R/W	Same as 1F2[H] except does not reset on Read. Write "1" to reset individual bits to "0".							
1F4	SR2	R	Same as 1F0[H] except unlatched values.							
1F5	SR4	R	Same as 1F2[H] except unlatched values.							
1F6	SR8[4]	R	Reserved			TPMOVOF	RPAISC	RLAISC	TPAISC	TLAISC
1F7			NOT EQUIPPED							
1F8	CR8	R/W	TRSD	TRLD	TRE1	TRE2	TPATH	TRAPS	EXAPS	RTLOOP
1F9	CR9	R/W	TRF1	TRC1	TRZ1	TRZ2	TRAIS	PTE	$\overline{\text{RXRTM}}$	RRB2
1FA	CR10	R/W	SPE	TCLK	RCLK	NWFTREN	TXRTM	RTDSEL	INC	DEC
1FB	CR11	R/W	TRFRM	TRERR	STPAIS	Unused[5]	RE2A	RA2E	TE2A	TA2E
1FC	CR12	R/W	TFREN	RTFIFO	DISTLAIS	LPAISEN	LPAISSEL	TFRIEN	Unused[5]	Unused[5]
1FD	CR13	R/W	Unused[5]				TXH4INS	Unused[5]		
1FE	CR14	R/W	TFRMEXT	TXC1EXT	TXE1EXT	TXF1EXT	TXSDEXT	TXZ1EXT	TXZ2EXT	TXE2EXT
1FF	HIBYTE	R/W	Most Significant Byte for 16 Bit Counters							

Notes:
1. SR = Status Register, CR = Control Register. See the detailed descriptions provided in the following tables (starting on page 62).
2. R = Read Only, R/W = Read/Write
3. Resets to all "0"s when Read
4. Unlatched values only
5. All Unused, Reserved and Test control bits are to be written to "0".

STATUS REGISTER DESCRIPTIONS

STATUS REGISTER 0

Address [H]	Bit	Symbol	Conditions		Comments
			Enter	Exit	
0F0 0F1 0F4	7	RLOC	**Rx Loss of Clock**: 200 - 2000 ns without transitions at RLCI.	Any Transition at RLCI.	If TRLOOP = "1" Looped Clock is monitored.
	6	RNPTR	**Rx New Pointer**: New Pointer due to NDF or receipt of three consecutive, equal and valid new pointer values.	No Exit Conditions - Latched Values are reset by µPro Read of 0F0[H] or Writing "1" to this bit in 0F1[H].	Inhibited if RLOC, RLOS, RLOF or RAIS-L is declared. For 0F4[H], see Note 2.
	5	RAIS-P	**Rx AIS-P**: 3 consecutive H1 and H2 bytes with all "1".	Receipt of NDF and Valid Pointer or three consecutive, equal and valid new pointer values.	Inhibited if RLOC, RLOS, RLOF or RAIS-L is declared.
	4	RAIS-L	**Rx AIS-L**: K2 Byte bits 6, 7 and 8 = "111" for 5 consecutive frames.	K2 Byte bits 6, 7 and 8 ≠ "111" for 5 consecutive frames.	Inhibited if RLOC, RLOS or RLOF is declared or if DISRLAL = "1".
	3	RLOP	**Rx Loss of Pointer**: 8 consecutive frames of NDF or Invalid Pointer.	3 consecutive frames of Valid Pointer or AIS indicator.	Inhibited if RLOC, RLOS, RLOF or RAIS-L is declared.
	2	RLOF	**Rx Loss of Frame**: RSEF persists for 3 ms.	1 ms without RSEF.	Inhibited if RLOC or RLOS is declared.
	1	RSEF (old ROOF)	**Rx Severely Errored Frame**: RFE Persists for 4 consecutive frames.	2 consecutive frames without RFE, or STS1 = "0" and $\overline{\text{RFRI}}$ Valid followed by A1 and A2 as expected.	Inhibited if RLOC or RLOS is declared.
	0	RLOS	**Rx Loss of Signal**: STS1 = "1": $\overline{\text{RXLOS}}$ ="0" or 720 Bit Times without transitions at RLDI. STS1 = "0": $\overline{\text{RXLOS}}$ ="0" or 6480 Bit Times without transitions at RLDI.	$\overline{\text{RXLOS}}$ ="1" and any transitions at RLDI.	Note 1. Inhibited if RLOC is declared. If TRLOOP = "1" Looped Data is monitored.

Notes:
1. When Internally generated ($\overline{\text{RXLOS}}$ = "1"), this is a device level alarm. It is not the Physical Medium Layer LOS.

2. This is a short duration event (« 1 Frame). The µPro may not be able to read the unlatched value.

STATUS REGISTER 1

Address [H]	Bit	Symbol	Conditions		Comments
			Enter	Exit	
0F2 0F3 0F5	7	INT	**Interrupt**: Any event that causes a µPro Interrupt.	No Exit Conditions - Latched Values are reset by µPro Read of 0F2[H] or Writing "1" to this bit in 0F3[H].	For 0F5[H], see Note 2.
	6	RTNEW	**Rx TOH New**: Any new debounced value of C1, F1, K1, K2, Z1 or Z2.	No Exit Conditions - Latched Values are reset by µPro Read of 0F2[H] or Writing "1" to this bit in 0F3[H].	Inhibited if RLOC, RLOS or RLOF is declared or if DISRLAL = "1". For 0F5[H], see Note 2.
	5	RPNEW	**Rx POH New**: Any new debounced value of C2, F2, Z3, Z4 or Z5.	No Exit Conditions - Latched Values are reset by µPro Read of 0F2[H] or Writing "1" to this bit in 0F3[H].	Inhibited if RLOC, RLOS, RLOF, RAIS-L, RLOP or RAIS-P is declared. For 0F5[H], see Note 2.
	4	RRDI-P (old Path Yellow)	**Rx RDI-P**: PRDISEL = "0" and G1 Byte Bits 5-7 = "100" or "111" for 10 consecutive frames.	PRDISEL = "0" and G1 Byte Bits 5-7 ≠ "100" or "111" for 10 consecutive frames.	See Note 1. Inhibited if RLOC, RLOS, RLOF, RAIS-L, RLOP or RAIS-P is declared.
			PRDISEL = "1" and G1 Byte Bits 5-7 = "100" or "111" for 5 consecutive frames.	PRDISEL = "1" and G1 Byte Bits 5-7 ≠ "100" or "111" for 5 consecutive frames.	
	3	RRDI-L (old FERF)	**Rx RDI-L**: K2 Byte bits 6, 7 and 8 = "110" for 5 consecutive frames.	K2 Byte bits 6, 7 and 8 ≠ "110" for 5 consecutive frames.	Inhibited if RLOC, RLOS or RLOF is declared or if DISRLAL = "1".
	2	RAPS	**Rx APS Fail**: 12 frame sliding window that does not contain 3 consecutive, identical pairs of K1 and K2 Bytes.	Reception of 3 consecutive, identical pairs of K1 and K2 Bytes.	Inhibited if RLOC, RLOS or RLOF is declared or if DISRLAL = "1".
	1	Unused			
	0	Unused			

Notes:

1. This is the alarm that is used to report Single Bit RDI-P. It is retained for backwards compatibility.
2. This is a short duration event (« 1 Frame). The µPro may not be able to read the unlatched value.

STATUS REGISTER 2

Address [H]	Bit	Symbol	Conditions		Comments
			Enter	Exit	
1F0 1F1 1F4	7	TLOC	**Tx Loss of Clock**: Either SPE = "1" or SPE, and PARA = "0" and 200 - 2000 ns without transitions at TTCI. SPE = "0", PARA = "1" and 200 - 2000 ns without transitions at TPCI.	Any transition at the enabled pin.	
	6	TNPTR	**Tx New Pointer**: New Pointer due to NDF or receipt of three consecutive, equal and valid new pointer values.	No Exit Conditions - Latched Values are reset by µPro Read of 1F0[H] or Writing "1" to this bit in 1F1[H].	Inhibited if TLOC, TLOS, TLOF or TAIS-L is declared or if C1J1EN = "1". For 1F4[H], see Note 1.
	5	TAIS-P	**Tx AIS-P**: 3 consecutive H1 and H2 bytes with all "1" at the Tx Terminal Port.	Receipt of NDF and Valid Pointer or three consecutive, equal and valid new pointer values.	Inhibited if TLOC, TLOS, TLOF or TAIS-L is declared or if C1J1EN = "1".
	4	TAIS-L	**Tx AIS-L**: K2 Byte bits 6, 7 and 8 = "111" for 5 consecutive frames at the Tx Terminal Port.	K2 Byte bits 6, 7 and 8 ≠ "111" for 5 consecutive frames.	Inhibited if TLOC, TLOS or TLOF is declared or if DISTLAIS = "1".
	3	TLOP	**Tx Loss of Pointer**: 8 consecutive frames of NDF or Invalid Pointer at the Tx Terminal Port.	3 consecutive frames of Valid Pointer or AIS indicator.	Inhibited if TLOC, TLOS, TLOF or TAIS-L is declared or if C1J1EN = "1".
	2	TLOF	**Tx Loss of Frame**: TSEF persists for 3 ms at the Tx Terminal Port.	1 ms without TSEF.	Inhibited if TLOC or TLOS is declared or if C1J1EN = "1".
	1	TSEF (old TOOF)	**Tx Severely Errored Frame**: TFE Persists for 4 consecutive frames at the Tx Terminal Port.	2 consecutive frames without TFE.	inhibited if TLOC or TLOS is declared or if C1J1EN = "1".

Note:
1. This is a short duration event (« 1 Frame). The µPro may not be able to read the unlatched value.

Address [H]	Bit	Symbol	Conditions		Comments
			Enter	Exit	
1F0 1F1 1F4 (cont.)	0	TLOS	**Tx Loss of Signal**: SPE = "1" and 2 Frames without transitions on TSPEI or TSYNI.	Any transitions on failed input(s).	Inhibited if TLOC is declared.
			SPEONLY = "0", and: 1. If C1J1EN = "0" and PARA = "0", then 6480-12960 bit times without transitions on TTDI. 2. If C1J1EN = "0" and PARA = "1", then 810-1620 byte times without transitions on TPDI0 - TPDI7. 3. If C1J1EN = "1", then 2-4 Frames without transitions on TSPEI or TSYNI.		

STATUS REGISTER 3

Address [H]	Bit	Symbol	Conditions		Comments
			Enter	Exit	
0E8 0E9 0EC	7	RLFRI	**Rx Loss of Frame Input**: 8 frames without transitions on $\overline{\text{RFRI}}$.	Any transitions on $\overline{\text{RFRI}}$.	Inhibited if RLOC or RLOS is declared or TRLOOP = "1" or STS1 = "1".
	6	RFE	**Rx Frame Error**: One or more A1 or A2 bits in error.	A1 and A2 received without errors.	Inhibited if RLOC or RLOS is declared.
	5	B2EBER	**B2 Excessive BER**: B2 Error Rate exceeds 1 in 10^3.	B2 Error Rate less than 1 in 10^3.	Inhibited if RLOC, RLOS, RLOF or RAIS-L is declared or DISRLAL = "1".
	4	B3EBER	**B3 Excessive BER**: B3 Error Rate exceeds 1 in 10^3.	B3 Error Rate less than 1 in 10^3.	inhibited if RLOC, RLOS, RLOF, RAIS-L, RAIS-P or RLOP is declared.

Address [H]	Bit	Symbol	Conditions		Comments
			Enter	Exit	
0E8 0E9 0EC (cont.)	3	RCPTR	**Rx Concatenated Pointer**: RLOP declared and: NDF Bits = "1001" SS Bits = "00" I Bits = "1" D Bits = "1"	RLOP not declared or concatenation indication not received.	Inhibited if RLOC, RLOS, RLOF or RAIS-L is declared.
	2	C2MIS	**C2 Mismatch**: Any of the combinations of Expect C2 Register and 5 consecutive Rx C2 Bytes that are listed below: C2 REG. [H] / Rx C2 [H] 00 / 01-FD 01 / 00 02 / 00, 03-E0, FC, FD-FF 03 / 00, 02, 04-E0, FC, FD-FF 04 / 00, 02, 03, 05-FB, FD-FF 05 ≤ x ≤ 11 / 00, 02-04, 05-11 excluding x, 12-FF 13 / 00, 02-12, 14-FB, FD-FF 14 / 00, 02-13, 15-FB, FD-FF 15 / 00, 02-14, 16-FB, FD-FF 16 ≤ x ≤ E0 / 00,02-15, 16-E0 excluding x, E1-FF	Any of the combinations of Expect C2 Register and 5 consecutive Received C2 Bytes that are not listed as an alarm condition.	Inhibited if RLOC, RLOS, RLOF, RAIS-L, RAIS-P or RLOP is declared.
	1	C2UNEQ	**C2 Unequipped**: 5 consecutive Received C2 Bytes = 00[H].	5 consecutive Received C2 Bytes ≠ 00[H].	Inhibited if RLOC, RLOS, RLOF, RAIS-L, RAIS-P or RLOP is declared.
	0	RLOM	**Rx Loss of Multiframe**: 2 successive frames in which the Received H4 Value does not match the expected sequence.	2 successive frames in which the value of the second H4 byte is equal to the first H4 value +1, modulo 4.	Inhibited if RLOC, RLOS, RLOF, RAIS-L, RAIS-P or RLOP is declared or H4INT = "0".

STATUS REGISTER 4

Address [H]	Bit	Symbol	Conditions		Comments
			Enter	Exit	
1F2 1F3 1F5	7	RRCOFA	**Rx Reference Change of Frame Alignment**: Any $\overline{\text{TFRI}}$ pulse that varies in frame position from the previous pulse.	No Exit Conditions - Latched values are reset by µPro Read of 1F2[H] or Writing "1" to this bit in 1F3[H].	
	6	LORR	**Loss of Rx Reference**: 200 - 2000 ns without transitions at TLCI, or RRFIEN = "1" and 8 frames without transitions on $\overline{\text{TFRI}}$.	Any transitions on the enabled pins.	Inhibited if RCLK = "0".
	5	RFIFOE	**Rx FIFO Error**: Receive FIFO Overflow or Underflow when Rx re-timing is enabled by one of the combinations shown below: SPE / RCLK / $\overline{\text{RXRTM}}$ 1 / - / - 0 / 1 / - 0 / 0 / 0	No Exit Conditions - Latched values are reset by µPro Read of 1F2[H] or Writing "1" to this bit in 1F3[H].	Inhibited if either SPE = "0, RCLK = "0" and $\overline{\text{RXRTM}}$ = "1" . For 1F5[H], see Note 2.
	4	RLE1	**Rx Line E1 Alarm**: 5 or more bits set to "1" in the Rx Line E1 Byte.	Less than 5 bits in the E1 byte set to "1".	Inhibited if RLOC, RLOS or RLOF is declared or RE2A = "0".
	3	TAISV	**Tx AIS Valid**: Pin $\overline{\text{TAIS}}$ at the "0" Logic Level.	Pin $\overline{\text{TAIS}}$ at the "1" Logic Level.	
	2-0	Unused			

Notes:
1. This is a short duration event (« 1 Frame). The µPro may not be able to read the unlatched value.
2. If Automatic Rx FIFO Reset is enabled (RFREN = "1") this is a short duration event and the µPro may not be able to read the unlatched value.

STATUS REGISTER 5

Address [H]	Bit	Symbol	Conditions		Comments
			Enter	Exit	
1E8 1E9 1EC	7	Unused			
	6	TFE	**Tx Frame Error**: One or more A1 or A2 bits in error at Tx Terminal Interface.	A1 and A2 received without errors at Tx Terminal Interface.	Inhibited if TLOC or TLOS is declared, or if C1J1EN = "1".
	5	TCPTR	**Tx Concatenated Pointer**: TLOP declared and: NDF Bits = "1001" SS Bits = "00" I Bits = "1" D Bits = "1"	TLOP not declared or concatenation indication not received.	Inhibited if TLOC, TLOS, TLOF or TAIS-L is declared, or if C1J1EN = "1".
	4	TTE1	**Tx Terminal E1 Alarm**: 5 or more bits set to "1" in the E1 Byte at the Tx Terminal Port.	Less than 5 bits in the E1 Byte set to "1".	Inhibited if TLOC, TLOS or TLOF is declared or if TE2A = "0".
	3	TRCOFA	**Tx Reference Change of Frame Alignment**: Any $\overline{\text{TFRI}}$ pulse that varies in frame position from the previous pulse.	No Exit Conditions - Latched Values are reset by µPro Read of 1E8[H] or Writing "1" to this bit in 1E9[H].	For 1EC[H], see Note 1.
	2	Unused			
	1	LOTR	**Loss of Tx Reference**: Either TCLK = "1" and 200 - 2000 ns without transitions at TLCI, or TFRIEN = "1" and 8 frames without transitions on $\overline{\text{TFRI}}$.	Any transitions on enabled pins.	
	0	TFIFOE	**Tx FIFO Error**: Transmit FIFO Overflow or Underflow when Tx re-timing is enabled by one of the combinations shown below: ↓ ↓ ↓ ↓ SPE 0 0 0 1 TCLK 0 0 1 - C1J1EN 0 1 - - TXRTM 1 - - -	No Exit Conditions - Latched Values are reset by µPro Read of 1E8[H] or Writing "1" to this bit in 1E9[H].	Inhibited when: ↓ SPE 0 TCLK 0 C1J1EN 0 TXRTM 0 For 1EC[H], see Note 2.

Notes:

1. This is a short duration event (« 1 Frame). The µPro may not be able to read the unlatched value.
2. If Automatic Tx FIFO Reset is enabled (TFREN = "1") this is a short duration event and the µPro may not be able to read the unlatched value.

STATUS REGISTER 6

Address [H]	Bit	Symbol	Conditions		Comments
			Enter	Exit	
0EA 0EB 0ED	7	RRDI-PSD	**Rx RDI-P, Signal Defect**: PRDISEL = "0" and G1, Bits 5-7 = "101" for 10 consecutive Frames.	PRDISEL = "0" and G1, Bits 5-7 ≠ "101" for 10 consecutive Frames.	Inhibited if RLOC, RLOS, RLOF, RAIS-L, RLOP or RAIS-P is declared.
			PRDISEL = "1" and G1, Bits 5-7 = "101" for 5 consecutive Frames.	PRDISEL = "1" and G1, Bits 5-7 ≠ "101" for 5 consecutive Frames.	
	6	RRDI-PCD	**Rx RDI-P, Connectivity Defect**: PRDISEL = "0" and G1, Bits 5-7 = "110" for 10 consecutive Frames.	PRDISEL = "0" and G1, Bits 5-7 ≠ "110" for 10 consecutive Frames.	Inhibited if RLOC, RLOS, RLOF, RAIS-L, RLOP or RAIS-P is declared.
			PRDISEL = "1" and G1, Bits 5-7 = "110" for 5 consecutive Frames.	PRDISEL = "1" and G1, Bits 5-7 ≠ "110" for 5 consecutive Frames.	
	5	RRDI-PPD	**Rx RDI-P, Payload Defect**: PRDISEL = "0" and G1, Bits 5-7 = "010" for 10 consecutive Frames.	PRDISEL = "0" and G1, Bits 5-7 ≠ "010" for 10 consecutive Frames.	Inhibited if RLOC, RLOS, RLOF, RAIS-L, RLOP or RAIS-P is declared.
			PRDISEL = "1" and G1, Bits 5-7 = "010" for 5 consecutive Frames.	PRDISEL = "1" and G1, Bits 5-7 ≠ "010" for 5 consecutive Frames.	
	4	RPDI-P	**Rx PDI-P**: Rx C2 Byte equal to any value in the range E1[H] through FC[H], inclusive, for 5 consecutive frames.	Rx C2 Byte not equal to any value in the range E1[H] through FC[H], inclusive, for 5 consecutive frames	Inhibited if RLOC, RLOS, RLOF, RAIS-L, RLOP or RAIS-P is declared.
	3	J0MIS	**J0 Mismatch**: J0EN(1,0) = "01" and Rx J0 Byte ≠ J0 Expect Register in 5 consecutive Frames.	Either J0EN(1,0) ≠ "01" or J0EN(1,0) = "01" and Rx J0 Byte = J0 Expect Register in 5 consecutive Frames.	Inhibited if RLOC, RLOS or RLOF is declared.
	2-0	Unused			

STATUS REGISTER 7

Address [H]	Bit	Symbol	Conditions		Comments
			Enter	Exit	
0F6	7	RB3COF	**Rx B3 Counter Overflow**: Overflow of Rx B3 Counter.	µPro Read of Rx B3 Counter.	
	6	RB2COF	**Rx B2 Counter Overflow**: Overflow of Rx B2 Counter.	µPro Read of Rx B2 Counter.	
	5	RB1COF	**Rx B1 Counter Overflow**: Overflow of Rx B1 Counter.	µPro Read of Rx B1 Counter.	
	4	RPFEBEOF	**Rx Path FEBE Counter Overflow**: Overflow of Rx FEBE-P Counter.	µPro Read of Rx FEBE-P Counter.	
	3	RLFEBEOF	**Rx Line FEBE Counter Overflow**: Overflow of Rx FEBE-L Counter.	µPro Read of Rx FEBE-L Counter.	
	2	RPMOVOF	**Rx Pointer Movement Counters Overflow**: Overflow of either the Rx Pointer Increment or Decrement Counters.	µPro Read of the counter which has overflowed.	
	1	RPJOF	**Rx Pointer Justification Counter Overflow**: Overflow of the Rx Pointer Justification Counter.	µPro Read of the Rx Pointer Justification Counter.	
	0	LPJOF	**Local Pointer Justification Counter Overflow**: Overflow of the Local Pointer Justification Counter.	µPro Read of the Local Pointer Justification Counter.	

STATUS REGISTER 8

Address [H]	Bit	Symbol	Conditions		Comments
			Enter	Exit	
1F6	7-5	Reserved			
	4	TPMOVOF	**Tx Pointer Movement Counters Overflow**: Overflow of either the Tx Pointer Increment or Decrement Counters.	µPro Read of the counter which has overflowed.	
	3	RPAISC	**Rx Path AIS Conditions**: Rx Line conditions are such that: 1. AIS-P will be inserted at the Rx Terminal Port if RRAIS = "1". 2. An E1 Alarm will be output at the Rx Terminal Port if RA2E = "1".	No Rx Line conditions exist that would cause an AIS-P or E1 Alarm to be output at the Rx Terminal Port If the functions were enabled.	See RRAIS and RA2E.
	2	RLAISC	**Rx Line AIS Conditions**: Rx Line conditions are such that: 1. AIS-L will be inserted at the Rx Terminal Port if RRAIS = "1". 2. An E1 Alarm will be output at the Rx Terminal Port if RA2E = "1".	No Rx Line conditions exist that would cause an AIS-L or E1 Alarm to be output at the Rx Terminal Port If the functions were enabled.	See RRAIS and RA2E.
	1	TPAISC	**Tx Path AIS Conditions**: Tx Terminal conditions are such that: 1. AIS-P will be inserted on the Tx Line if TRAIS = "1". 2. An E1 Alarm will be output on the Tx Line if TA2E = "1".	No Tx Terminal conditions exist that would cause an AIS-P or E1 Alarm to be output on the Tx Line if the functions were enabled.	See TRAIS and TA2E.
	0	TLAISC	**Tx Line AIS Conditions**: Tx Terminal conditions are such that: 1. AIS-L will be inserted on the Tx Line if TRAIS = "1". 2. An E1 Alarm will be output on the Tx Line if TA2E = "1".	No Tx Terminal conditions exist that would cause an AIS-L or E1 Alarm to be output on the Tx Line if the functions were enabled.	See TRAIS and TA2E.

STATUS REGISTER 9

Address [H]	Bit	Symbol	Conditions		Comments
			Enter	Exit	
0F7	7	REG0	**Register 0 Status Set**: One or more latched bits set in Status Register 0.	All latched Bits = "0" in Status Register 0.	0F0[H] 0F1[H]
	6	REG1	**Register 1 Status Set**: One or more latched bits set in Status Register 1.	All latched Bits = "0" in Status Register 1.	OF2[H] 0F3[H]
	5	REG3	**Register 3 Status Set**: One or more latched bits set in Status Register 3.	All latched Bits = "0" in Status Register 3.	0E8[H] 0E9[H]
	4	REG6	**Register 6 Status Set**: One or more latched bits set in Status Register 6.	All latched Bits = "0" in Status Register 6.	0EA[H] 0EB[H]
	3	REG2	**Register 2 Status Set**: One or more latched bits set in Status Register 2.	All latched Bits = "0" in Status Register 2.	1F0[H] 1F1[H]
	2	REG4	**Register 4 Status Set**: One or more latched bits set in Status Register 4.	All latched Bits = "0" in Status Register 4.	1F2[H] 1F3[H]
	1	REG5	**Register 5 Status Set**: One or more latched bits set in Status Register 5.	All latched Bits = "0" in Status Register 5.	1E8[H] 1E9[H]
	0	REG78	**Registers 7 or 8 Status Set**: One or more bits in Status Register 7 or Bits 7-4 in Status Register 8 = "1".	All bits in Status Register 7 and Bits 7-4 in Status Register 8 = "0".	0F6[H] 1F6[H], Bits 7-4

CONTROL REGISTER DESCRIPTIONS

CONTROL REGISTER 0

Address [H]	Bit	Symbol	Conditions		Comments
			Bit Equal to "1"	Bit Equal to "0"	
0F8	7	RRSD	**Rx Terminal Port Section Datacom Bytes Control**: Outgoing Terminal Data contains D1-D3 Bytes from Rx TOH Insert RAM Locations.	Outgoing Terminal Data contains D1-D3 Bytes from the Rx Line.	Notes 1 and 2.
	6	RRLD	**Rx Terminal Port Line Datacom Bytes Control**: Outgoing Terminal Data contains D4-D12 Bytes from Rx TOH Insert RAM Locations.	Outgoing Terminal Data contains D4-D12 Bytes from the Rx Line.	Notes 1 and 2.
	5	RRE1	**Rx Terminal Port E1 Byte Control**: Outgoing Terminal Data contains E1 Byte from Rx TOH Insert RAM Location.	Outgoing Terminal Data contains E1 Byte from the Rx Line.	Notes 1, 2 and 3.
	4	RRE2	**Rx Terminal Port E2 Byte Control**: Outgoing Terminal Data contains E2 Byte from Rx TOH Insert RAM Location.	Outgoing Terminal Data contains E2 Byte from the Rx Line.	Notes 1 and 2.
	3	RPATH	**Rx Terminal Port POH Bytes Control**: Outgoing Terminal Data contains POH Bytes from Rx POH Insert RAM Locations.	Outgoing Terminal Data contains POH Bytes from the Rx Line.	Note 4. See H4INT.
	2	RRAPS	**Rx Terminal Port APS Bytes Control**: Outgoing Terminal Data contains K1 and K2 Bytes from Rx TOH Insert RAM Locations.	Outgoing Terminal Data contains K1 and K2 Bytes from the Rx Line.	Notes 1 and 2.
	1	RRPTR	**Rx Terminal Port Pointer Bytes Control**: Outgoing Terminal Data contains H1, H2 and H3 Bytes from Rx TOH Insert RAM Locations.	1. Re-timing disabled: Outgoing Terminal Data contains H1, H2 and H3 Bytes from the Rx Line. 2. Re-timing enabled: H1 and H2 recalculated and H3 from Rx TOH Insert RAM Location.	This is for test purposes only. Payload does not track insert location H1 and H2 values.

Address [H]	Bit	Symbol	Conditions		Comments
			Bit Equal to "1"	Bit Equal to "0"	
0F8 (cont.)	0	TRLOOP	**Tx-Rx Loopback Enable**: Tx Line Output looped back to Rx Line Input.	Normal operation.	See LPAISEN and LPAISSEL.

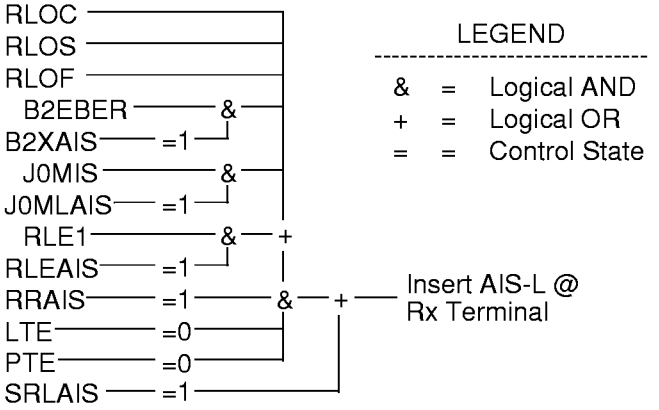
Notes:
1. This control is only effective if SPE = "0".
2. If RCLK = "1", this control is disabled and BIT EQUAL TO "1" condition applies.
3. This control is only enabled if RA2E = "0".
4. The J1 Bytes are always passed through from the Rx Line. The H4 Byte selection is controlled by H4INT. The Rx POH Insert RAM B3 Location contains the recalculated B3 value. B3 Recalculation is performed and the Insert Location is used if RPATH or H4INT = "1".

CONTROL REGISTER 1

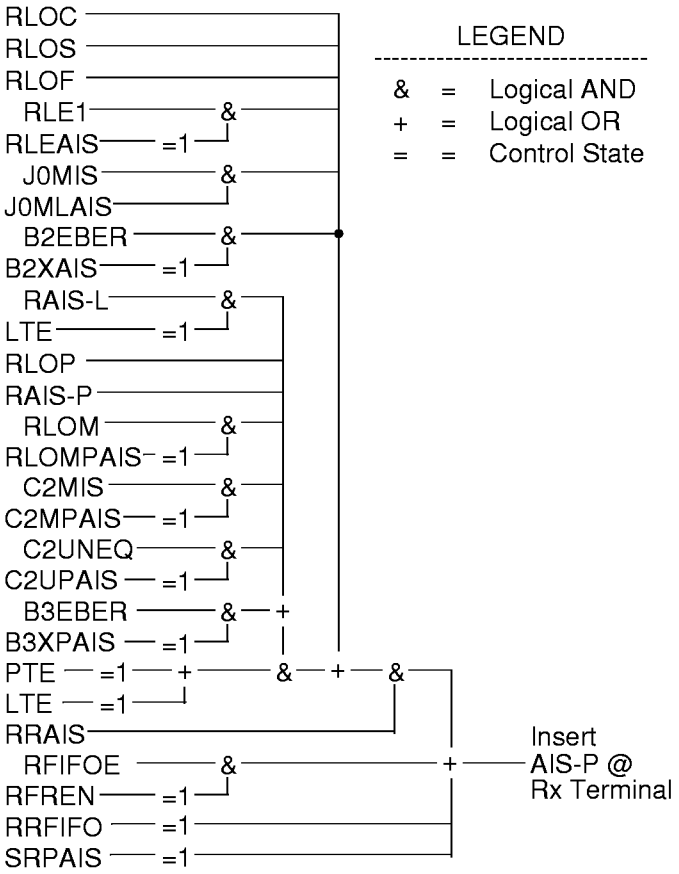
Address [H]	Bit	Symbol	Conditions		Comments
			Bit Equal to "1"	Bit Equal to "0"	
0F9	7	RRF1	**Rx Terminal Port F1 Byte Control**: Outgoing Terminal Data contains F1 Byte from Rx TOH Insert RAM Location.	Outgoing Terminal Data contains F1 Byte from the Rx Line.	Notes 1 and 2.
	6	RRC1	**Rx Terminal Port C1 Byte Control**: Outgoing Terminal Data contains C1 Byte from Rx TOH Insert RAM Location.	Outgoing Terminal Data contains C1 Byte from the Rx Line	Notes 1 and 2.
	5	RRZ1	**Rx Terminal Port Z1 Byte Control**: Outgoing Terminal Data contains Z1 Byte from Rx TOH Insert RAM Location.	Outgoing Terminal Data contains Z1 Byte from the Rx Line.	Notes 1 and 2.
	4	RRZ2	**Rx Terminal Port Z2 Byte Control**: Outgoing Terminal Data contains Z2 Byte from Rx TOH Insert RAM Location.	Outgoing Terminal Data contains Z2 Byte from the Rx Line.	Notes 1 and 2.

Address [H]	Bit	Symbol	Conditions		Comments
			Bit Equal to "1"	Bit Equal to "0"	
0F9 (cont.)	3	RRAIS	**Rx Terminal Port AIS Insert Control**: Enables the automatic insertion of AIS into Rx Terminal Data.	Disables the automatic insertion of AIS into Rx Terminal Data.	

Rx Terminal AIS-L Insertion



Rx Terminal AIS-P Insertion

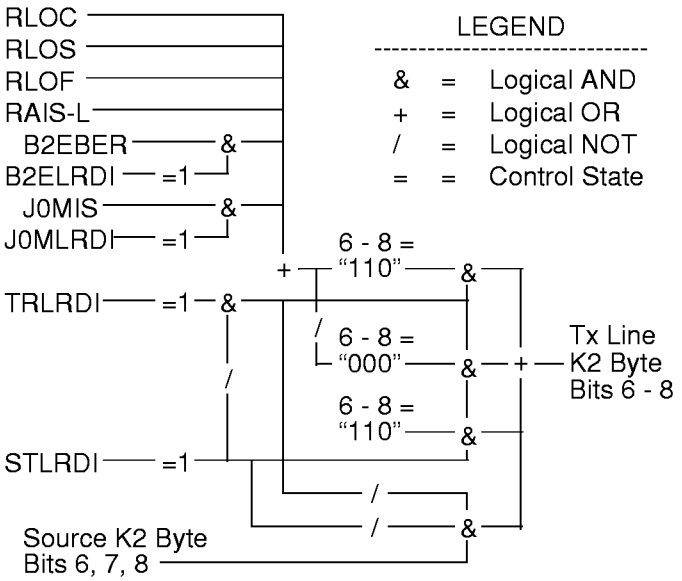


Address [H]	Bit	Symbol	Conditions		Comments
			Bit Equal to "1"	Bit Equal to "0"	
0F9 (cont.)	2	LTE	**Line Terminating Equipment Enable**: Defines Line Terminating Equipment Mode for AIS transmission and Introduction.	Defines not Line Terminating Equipment Mode for AIS transmission and Introduction.	Section Terminating Equipment Mode if LTE = "0" and PTE = "0".
	1	RRFRM	**Rx Terminal Port Framing Bytes Control**: Framing Bytes are regenerated in Rx Terminal Data and placed in Rx TOH Insert RAM Locations.	Rx Terminal Data has Framing Bytes from Rx Line.	Notes 1 and 2.
	0	RRB1	**Rx Terminal Port B1 Byte Control**: B1 Byte is recalculated for Rx Terminal Data and placed in Rx TOH Insert RAM Location.	Outgoing Terminal Data contains B1 Byte from the Rx Line.	Notes 1, 2 and 3.

Notes:
1. This control is only effective if SPE = "0".
2. If RCLK = "1", this control is disabled and BIT EQUAL TO "1" condition applies.
3. If STS1 = "1" control is disabled and value is recalculated.

CONTROL REGISTER 2

Address [H]	Bit	Symbol	Conditions		Comments
			Bit Equal to "1"	Bit Equal to "0"	
0FA	7	STS1	**STS-1/STS-N Mode Control**: Line Side in STS-1 Mode. Rx and Tx Data scrambled. Rx and Tx B1 contains BIP-8 Parity.	Line Side in STS-N Mode. Data is not scrambled. Rx B1 Byte contains Error indication. Tx B1 Byte contains Error Mask.	
	6	PARA	**Parallel/Serial Mode Control**: Tx Terminal Port is Parallel. Rx Terminal Port has both Serial and Parallel Interfaces active.	Tx Terminal Port is Serial. Rx Terminal Port has both Serial and Parallel Interfaces active.	Note 1.
	5	HWINE	**Hardware Interrupt Enable**: Enables Hardware Interrupts via INT/$\overline{TRQ}$ Pin.	Disables Hardware Interrupt Pin.	

Address [H]	Bit	Symbol	Conditions		Comments
			Bit Equal to "1"	Bit Equal to "0"	
0FA (cont.)	4	TRLRDI	**Tx Line Port Line RDI Enable**: Enables automatic insertion of RDI-L in Tx Line Data. K2 Byte Bits 6-8 controlled by alarm conditions.	K2 Byte Bits 6-8 are not modified and automatic insertion of RDI-L in Tx Line Data is disabled.	
			Tx Line RDI-L Insertion  		
	3	ALTOW	**Order Wire Mode Control**: OW Frame Pulse at OW/APS Port coincident with MSB of E1 and E2 Bytes.	OW Frame Pulse at OW/APS Port leads MSB of E1 and E2 Bytes by 1 bit.	Effective only if OA = "1".
	2	TIEN	**Transport Layer Interrupt Enable**: Enables Transport Layer Interrupts.	Disables Transport Layer Interrupts.	See Table 22 (page 141).
	1	PIEN	**Path Layer Interrupt Enable**: Enables Path Layer Interrupts.	Disables Path Layer Interrupts.	See Table 23 (page 142).
	0	-VE	**Interrupt Edge Control**: Interrupts on both positive and negative edges of alarms.	Interrupts on positive edge of alarms.	

Note 1. If SPE = "1", this control must = "0". Only the Serial Interfaces are active the Tx Terminal Port. See Table 1 (page 101).

CONTROL REGISTER 3

Address [H]	Bit	Symbol	Conditions		Comments
			Bit Equal to "1"	Bit Equal to "0"	
0FB	7	RRFIEN	**Rx Reference Frame Input Enable**: Failure of $\overline{\text{TFRI}}$ input is part of LORR Equation.	$\overline{\text{TFRI}}$ failure is not part of LORR Equation.	
	6	RFREN	**Rx FIFO Reset Enable**: Automatic recovery from Rx FIFO under/over flow enabled.	Automatic recovery from Rx FIFO under/over flow disabled.	Note 1.
	5	RRFIFO	**Reset Rx FIFO**: Rising edge causes a reset of the Rx FIFO. Control bit is reset to "0" upon completion of operation.	Normal operation.	Note 1.
	4	Unused			Note 2.
	3	DISRLAL	**Disable Rx Line Alarms**: Rx Line Level Alarms, B1, B2, and FEBE-L, Counters disabled.	Rx Line Level Alarms, B1, B2, and FEBE-L, Counters enabled.	
	2	CNT16EN	**Counter 16 Bit Enable**: Enables 16 bit count mode for Rx Side B1, B2, B3, FEBE-L and FEBE-P counters.	Rx Side B1, B2, B3, FEBE-L and FEBE-P counters are 8 bits.	
	1	RSWRES	**Rx Software Reset**: Resets all Rx Side counters, and clears Rx Side Status Bits. Normal operation is inhibited.	Cancels Rx Side Reset. Normal operation resumed.	
	0	Unused			Note 2.

Notes:

1. The following operations are performed during an Rx FIFO Reset:
   (1) AIS-P output at Rx Terminal Port,
   (2) FIFO is re-centered,
   (3) New Pointer Value is calculated,
   (4) AIS-P is terminated with the New Pointer value and active NDF indication.
2. Unused bits are to be written to "0".

CONTROL REGISTER 4

Address [H]	Bit	Symbol	Conditions		Comments
			Bit Equal to "1"	Bit Equal to "0"	
0FC	7	SRLAIS	**Send Rx Line AIS**: AIS-L inserted in Rx Terminal Port Data.	AIS-L not forced in Rx Terminal Port Data.	See RRAIS.
	6	B2XAIS	**B2 Excess BER Line AIS Enable**: Excess B2 Error condition included in equation for AIS-L insertion at Rx Terminal Port.	Excess B2 Error condition excluded from equation for AIS-L insertion at Rx Terminal Port.	See RRAIS.
	5	SRPAIS	**Send Rx Path AIS**: AIS-P inserted in Rx Terminal Port Data.	AIS-P not forced in Rx Terminal Port Data.	See RRAIS.
	4	B3XPAIS	**B3 Excess BER Path AIS Enable**: Excess B3 Error condition included in equation for AIS-P insertion at Rx Terminal Port.	Excess B3 Error condition excluded from equation for AIS-P insertion at Rx Terminal Port.	See RRAIS.
	3	RLOMPAIS	**Rx Loss of Multiframe Path AIS Enable**: RLOM condition included in equation for AIS-P insertion at Rx Terminal Port.	RLOM condition excluded from equation for AIS-P insertion at Rx Terminal Port.	See RRAIS.
	2	C2MPAIS	**C2 Mismatch Path AIS Enable**: C2 Mismatch condition included in equation for AIS-P insertion at Rx Terminal Port.	C2 Mismatch condition excluded from equation for AIS-P insertion at Rx Terminal Port.	See RRAIS.
	1	C2UPAIS	**C2 Unequipped Path AIS Enable**: Rx C2 Unequipped condition included in equation for AIS-P insertion at Rx Terminal Port.	C2 Unequipped condition excluded from equation for AIS-P insertion at Rx Terminal Port.	See RRAIS.
	0	RLEAIS	**RLE1 Path AIS Enable**: RLE1 condition included in equations for AIS-P and AIS-L insertion at Rx Terminal Port.	RLE1 condition excluded from equations for AIS-P and AIS-L insertion at Rx Terminal Port.	See RRAIS.

CONTROL REGISTER 5

Address [H]	Bit	Symbol	Conditions		Comments
			Bit Equal to "1"	Bit Equal to "0"	
0FD	7	DIEN	**Device Layer Interrupt Enable**: Enables Device Layer Interrupts.	Disables Device Layer Interrupts.	See Table 24 (page 142).
	6-4	Unused			Note 1.
	3	INVPCK	**Invert Parallel Clock**: TPDO(0-7), RSPE and RSYN occur on rising edge of TPCO. TPDI(0-7), TSPEI and TSYNI are sampled on the falling edge of TPCI.	TPDO(0-7), RSPE and RSYN occur on falling edge of TPCO. TPDI(0-7), TSPEI and TSYNI are sampled on the rising edge of TPCI.	
	2-1	Unused			Note 1.
	0	INVINT	**Invert Interrupt**: Pin INT transitions low to indicate interrupt.	Pin INT transitions high to indicate interrupt.	

Note:
1. Unused bits are to be written to "0".

CONTROL REGISTER 6

Address [H]	Bit	Symbol	Conditions		Comments
			Bit Equal to "1"	Bit Equal to "0"	
0FE	7	Reserved			Note 1.
	6	RAMTSTEN	**RAM Test Enable**: Internal operations are inhibited from writing to RAM Locations.	Normal operation.	
	5	H4INT	**H4 Internal**: Rx Side; H4 Byte output at Rx Terminal Port is regenerated. If SPE = "0" then RSYN = C1J1V1. If SPE = "1" then RSYN = J1V1. Tx Side; If SPE = "0" and C1J1EN = "1" then TSYNI = C1J1V1. If SPE = "1" then TSYNI = J1V1.	Rx Side; H4 Byte output at Rx Terminal Port as received from Rx Line. If SPE = "0" then RSYN = C1J1. If SPE = "1" then RSYN = J1. Tx Side; If SPE = "0" and C1J1EN = "1" then TSYNI = C1J1. If SPE = "1" then TSYNI = J1.	See RPATH, TXH4INS and TPATH.
	4	J1SYNCEN	**J1 Synchronization Enable**: Incoming J1 Message is stored such that the byte following ASCII (CR) and (LF) characters is stored in the Lowest address location.	Incoming J1 Bytes are stored in rotating fashion with no specific starting point.	Note 2.
	3	S1	**Pointer S1 Bit**: H1 Byte Bit 5 = "1"	H1 Byte Bit 5 = "0"	Note 3.
	2	S0	**Pointer S0 Bit**: H1 Byte Bit 6 = "1"	H1 Byte Bit 6 = "0"	
	1	C1J1EN	**C1/J1 Enable**: TSYNI and TSPEI are used for Frame and SPE alignment at Tx Terminal Port.	A1/A2 and H1/H2 are used for Frame and SPE alignment at Tx Terminal Port.	Note 4.
	0	OA	**OW/APS Port or All TOH Port Mode Control**: E1, E2, K1 and K2 Bytes output and input at Rx and Tx OA/TOH Ports, respectively.	All TOH Bytes output and input at Rx and Tx OA/TOH Ports, respectively.	

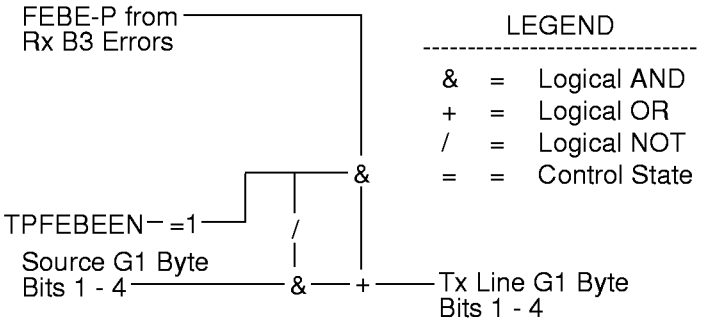
Notes:

1. Reserved bit is to be written to "0".
2. This applies to inputs from Rx Line, Tx Terminal and Tx TOH Port.
3. This applies to Tx and Rx Side Pointer Generation.
4. If SPE = "1", this control is disabled. The methodologies for Frame Delineation are inherent to these modes of operation.

CONTROL REGISTER 7

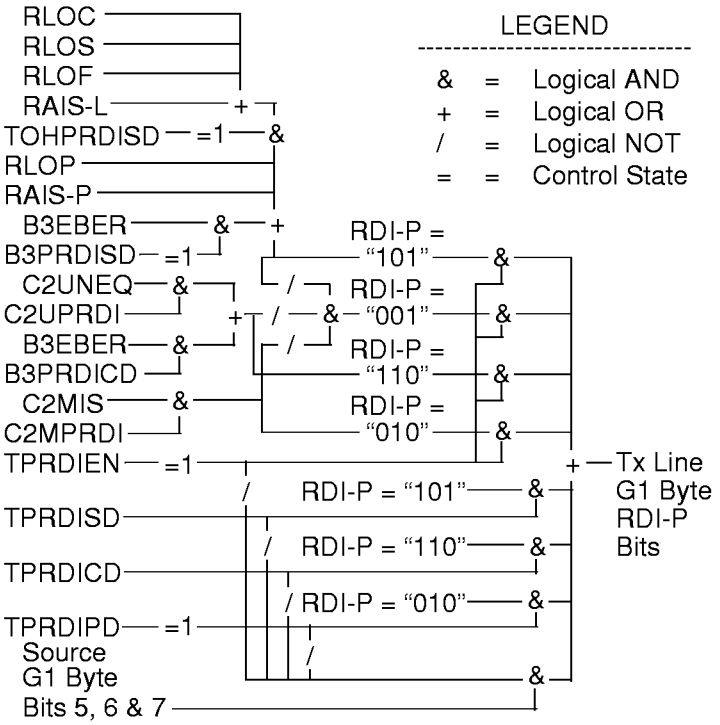
Address [H]	Bit	Symbol	Conditions		Comments
			Bit Equal to "1"	Bit Equal to "0"	
1DE	7	TIDL	**Tx Idle**: Path Idle signal is inserted at the Tx Line Port.	Path Idle signal is not inserted at the Tx Line Port.	Notes 3 and 4.
	6	IDLSEL	**Idle Signal Select**: All SPE bytes except POH Bytes are set to "0".	All SPE Bytes including POH Bytes are set to "0".	Notes 2, 3 and 4.
	5	TPFEBEEN	**Path FEBE Enable**: G1 Byte, Bits 1-4 in the Tx Line Port Data are overwritten by FEBE-P derived from Rx B3 Byte.	G1 Byte, Bits 1-4 in the Tx Line Port Data are not over-written.	

Tx Line FEBE-P Insertion



Address [H]	Bit	Symbol	Conditions		Comments
			Bit Equal to "1"	Bit Equal to "0"	
1DE (cont.)	4	TPRDIEN	**Tx Line Port Path RDI Enable**: Automatic insertion of RDI-P in Tx Line Port Data enabled. G1 Byte RDI-P Bits are controlled by alarm conditions.	G1 Byte RDI-P Bits are not modified and automatic insertion of RDI-P in Tx Line Port Data disabled.	
	3	C2MPRDI	**C2 Mismatch Path RDI Enable**: C2 Mismatch condition included in equation for RDI-PPD insertion at Tx Line Port.	C2 Mismatch condition excluded from equation for RDI-PPD insertion at Tx Line Port.	
	2	C2UPRDI	**C2 Unequipped Path RDI Enable**: Rx C2 Unequipped condition included in equation for RDI-PCD insertion at Tx Line Port.	C2 Unequipped condition excluded from equation for RDI-PCD insertion at Tx Line Port.	
	1-0	Reserved	These bits must be set to "0" if NWFTREN = "1".		Note 1.

Tx Line RDI-P Insertion



Notes:
1. Reserved bits are to be written to "0".
2. This control is effective only if TIDL = "1".
3. If TIDL and IDLSEL = "1", TPATH is disabled and the POH Bytes are taken from the Tx POH Insert locations. The controls TXH4INS, TPFEBEEN, TPRDIEN, TPRDICD, TPRDISD, and TPRDIPD are functional.
4. If TIDL = "1" and IDLSEL = "0", the Tx POH Bytes are forced to "0" and all Tx POH selection controls are disabled.

CONTROL REGISTER 8

Address [H]	Bit	Symbol	Conditions		Comments
			Bit Equal to "1"	Bit Equal to "0"	
1F8	7	TRSD	**Tx Line Port Section Datacom Bytes Control**: Outgoing Line Data contains D1-D3 Bytes from Tx TOH Insert RAM Locations.	Outgoing Line Data contains D1-D3 Bytes from Tx Terminal Port.	Note 1. See TXSDEXT.
	6	TRLD	**Tx Line Port Line Datacom Bytes Control**: Outgoing Line Data contains D4-D12 Bytes from Tx TOH Insert RAM Locations.	Outgoing Line Data contains D4-D12 Bytes from Tx Terminal Port.	Note 1. See TXLDEXT.
	5	TRE1	**Tx Line Port E1 Byte Control**: Outgoing Line Data contains E1 Byte from Tx TOH Insert RAM Locations.	Outgoing Line Data contains E1 Byte from Tx Terminal Port.	Notes 1 and 2. See TXE1EXT.
	4	TRE2	**Tx Line Port E2 Byte Control**: Outgoing Line Data contains E2 Byte from Tx TOH Insert RAM Locations.	Outgoing Line Data contains E2 Byte from Tx Terminal Port.	Note 1. See TXE2EXT.
	3	TPATH	**Tx Line Port POH Bytes Control**: Outgoing Line Data contains POH Bytes from Tx POH Insert RAM Locations.	Outgoing Line Data contains POH Bytes from the Tx Terminal Port. The Tx POH Insert Locations contain J0 Bytes input at Tx Terminal Port.	Notes 3, 4. See J1SYNCEN.
	2	TRAPS	**Tx Line Port APS Bytes Control**: Outgoing Terminal Data contains K1 and K2 Bytes from Tx TOH Insert RAM Locations.	Outgoing Terminal Data contains K1 and K2 Bytes from the Tx Terminal Port.	Note 1. See EXAPS.
	1	EXAPS	**External APS Bytes Control**: Tx TOH RAM Insert K1 and K2 Byte Locations contain data from Tx OA/TOH Port.	Tx TOH RAM Insert K1 and K2 Byte Locations written by µPro.	Note 5.
	0	RTLOOP	**Rx-Tx Loopback Enable**: Rx Terminal Output looped back to Tx Terminal Input.	Normal operation.	

Notes:

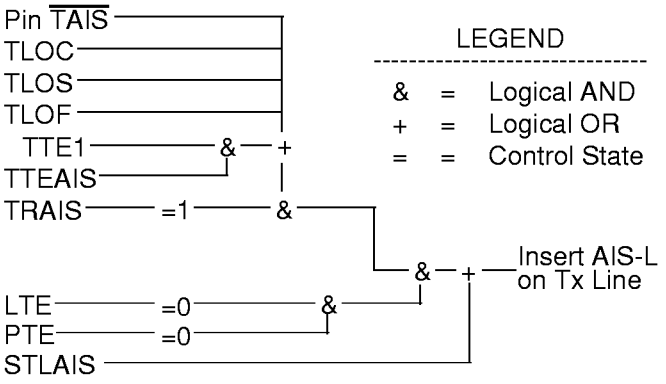
1. If SPE or TCLK = "1", this control is disabled and BIT EQUAL TO "1" condition applies.
2. This control is only enabled if TA2E = "0".
3. If TIDL = "1", this control is disabled and BIT EQUAL TO "1" condition applies.
4. The H4 Byte is also controlled by H4INT and TXH4INS. The Tx POH Insert RAM B3 Location contains the recalculated B3 Value. If TPATH = "0" and H4INT, TPFEBEEN, TPRDIEN, TPRDICD, TPRDISD or TPRDIPD = "1", then B3 will be recalculated and the Insert Location will be used.
5. This control is enabled if SPE or TRAPS = "1".

CONTROL REGISTER 9

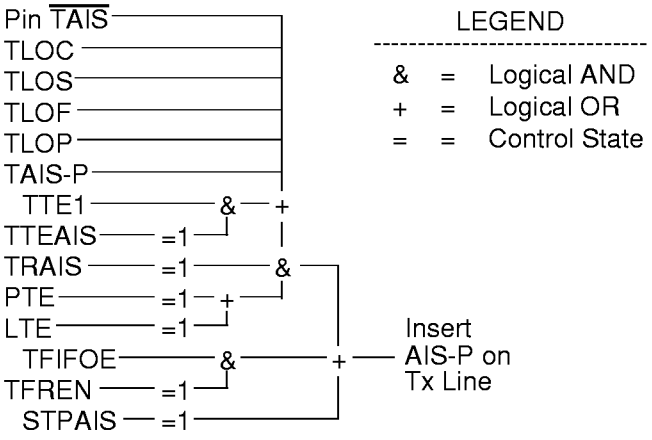
Address [H]	Bit	Symbol	Conditions		Comments
			Bit Equal to "1"	Bit Equal to "0"	
1F9	7	TRF1	**Tx Line Port F1 Byte Control**: Outgoing Line Data contains F1 Byte from Tx TOH Insert RAM Locations.	Outgoing Line Data contains F1 Byte from Tx Terminal Port.	Note 1. See TXF1EXT.
	6	TRC1	**Tx Line Port C1/J0 Byte Control**: Outgoing Line Data contains C1/J0 Byte(s) from Tx TOH Insert RAM Locations.	Outgoing Line Data contains C1/J0 Byte(s) from Tx Terminal Port.	Note 1. See TXC1EXT and J0EN(0,1).
	5	TRZ1	**Tx Line Port Z1 Byte Control**: Outgoing Line Data contains Z1 Byte from Tx TOH Insert RAM Locations.	Outgoing Line Data contains Z1 Byte from Tx Terminal Port.	Note 1. See TXZ1EXT.
	4	TRZ2	**Tx Line Port Z2 Byte Control**: Outgoing Line Data contains Z2 Byte from Tx TOH Insert RAM Locations.	Outgoing Line Data contains Z2 Byte from Tx Terminal Port.	Note 1. See TXZ2EXT.

Address [H]	Bit	Symbol	Conditions		Comments
			Bit Equal to "1"	Bit Equal to "0"	
1F9 (cont.)	3	TRAIS	**Tx Line Port AIS Insert Control**: Enables the automatic insertion of AIS into Tx Line Data.	Disables the automatic insertion of AIS into Tx Line Data.	
	2	PTE	**Path Terminating Equipment Enable**: Defines Path Terminating Equipment Mode for AIS transmission and Introduction.	Defines not Path Terminating Equipment Mode for AIS transmission and Introduction.	Section Terminating Equipment Mode if LTE = "0" and PTE = "0".
	1	$\overline{\text{RXRTM}}$	**Rx Re-Timing Mode Control**: Rx Re-timing disabled.	Rx Re-timing enabled.	Note 2.

Tx Line AIS-L Insertion



Tx Line AIS-P Insertion



Address [H]	Bit	Symbol	Conditions		Comments
			Bit Equal to "1"	Bit Equal to "0"	
1F9 (cont.)	0	RRB2	**Rx Terminal Port B2 Byte Control**: B2 Byte is recalculated in Rx Terminal Data and placed in Rx TOH Insert RAM Location.	Outgoing Terminal Data contains B2 Byte from the Rx Line.	Notes 3 and 4.

Notes:
1. If SPE or TCLK = "1", this control is disabled and BIT EQUAL TO "1" condition applies.
2. If SPE or RCLK = "1", this control is disabled and BIT EQUAL TO "0" condition applies.
3. If RCLK = "1", this control is disabled and BIT EQUAL TO "1" condition applies.
4. If SPE = "1", this control is disabled.

CONTROL REGISTER 10

Address [H]	Bit	Symbol	Conditions		Comments
			Bit Equal to "1"	Bit Equal to "0"	
1FA	7	SPE	**SPE-only Mode Select**: Places the device in SPE-only Mode.	Device not in SPE-only Mode.	Note 1.
	6	TCLK	**Tx Clock Source Select**: External Timing: TLCO derived from TLCI and start of Tx Frame derived from $\overline{TFRI}$ Tx Line.	PARA = "0" - External Timing: TLCO derived from $\overline{TTCI}$ and start of Tx Frame derived from TSYNI if C1J1EN = "1" or A1 and A2 Bytes input at the Tx Terminal Port if C1J1EN = "0".	Notes 2, 3, 4 and 5.
				PARA = "1" - External Timing: TLCO derived from TLCI and start of Tx Frame derived from $\overline{TFRI}$.	Notes 2, 3, 4, 5 and 6.
	5	RCLK	**Rx Clock Source Select**: External Timing: Rx Terminal Port Clock is derived from TLCI and start of Rx Frame is derived from $\overline{TFRI}$.	Line Timing: Rx Terminal Port Clock is derived from RXCK and start of Rx Frame derived from $\overline{RXFR}$.	Note 4.
	4	NWFTREN	**New Features Enable**: New features are available ("B" mode).	New features are disabled ("A" mode).	Note 8.
	3	TXRTM	**Tx Re-Timing Mode Control**: Tx Re-timing enabled.	Tx Re-timing disabled.	Note 7.

Address [H]	Bit	Symbol	Conditions		Comments
			Bit Equal to "1"	Bit Equal to "0"	
1FA (cont.)	2	RTDSEL	**Rx Terminal Delay Select**: Rx Terminal Port Serial Interface - output of MSB of C1 Byte coincident with the falling edge of $\overline{TFRI}$. Rx Terminal Port Parallel Interface: 1. ↓ TPCO coincident with the MSB of RTDO. 2. TPDO Byte boundaries coincident with MSB of RTDO. 3. RSYN and RSPE coincident with MSB of RTDO.	Rx Terminal Port Serial Interface - output of MSB of C1 Byte occurs 2 RTCO periods after the falling edge of $\overline{TFRI}$. Rx Terminal Port Parallel Interface: 1. ↓ TPCO occurs 1 RTCO period after the MSB of RTDO. 2. TPDO Byte boundaries occur 2 RTCO periods before MSB of RTDO. 3. RSYN and RSPE coincident with MSB of RTDO.	Note 9.
	1	INC	**Tx Pointer Increment**: Forces Pointer Increments in every frame in Tx Line Data.	Normal operation.	These bits must be used with extreme caution. Consecutive PJs will cause downstream alarms. Multiple PJs can cause FIFO spills.
	0	DEC	**Tx Pointer Decrement**: Forces Pointer Decrements in every frame in Tx Line Data.	Normal operation.	

Notes:

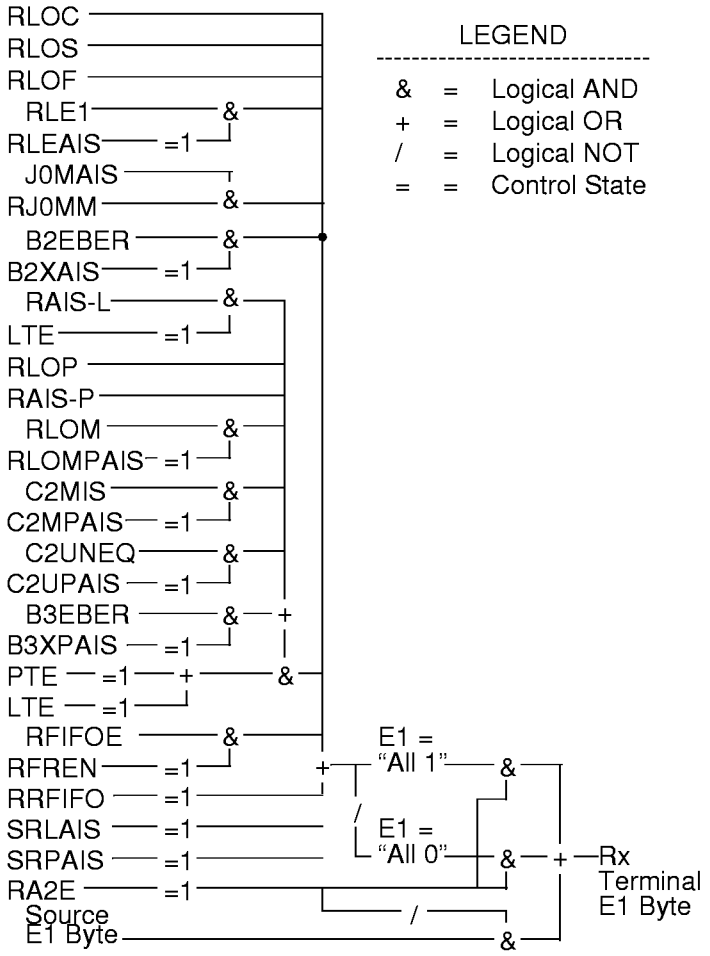
1. If SPE = "0", the device is in SONET Mode. See Table 1 (page 101).
2. If SPE = "1", this control is disabled and BIT EQUAL TO "1" condition applies.
3. If TCLK = "1", the Tx Terminal Option for Tx Line TOH Bytes and the option to turn off Tx Re-timing are disabled. If TCLK = "0", these options are enabled.
4. If a Frame Pulse is not supplied the starting point of the generated frame will be arbitrary.
5. See TRC1, TRE1, TRE2, TRF1, TRSD, TRLD, TRZ1 and TRZ2.
6. If TCLK = "0" and the Terminal Port is in a mode that does not have a 51.84 Mb/s Clock, TLCI and $\overline{TFRI}$ must adhere to the relationship shown in Figure 18, page 31.
7. If either SPE = "1"; SPE = "0 and C1J1EN = "1"; or TCLK = "1" then this control is disabled and BIT EQUAL TO "1" condition applies. Tx Re-timing is only an option if SPE, TCLK, and C1J1EN = "0".
8. This bit must be set"1" to for the SOT-1 to function as described in this Data Sheet.
9. The BIT EQUAL TO "0" conditions provide backwards compatibility with the SOT-1 TXC-03001 device.

CONTROL REGISTER 11

Address [H]	Bit	Symbol	Conditions		Comments
			Bit Equal to "1"	Bit Equal to "0"	
1FB	7	TRFRM	**Tx Line Port Framing Bytes Control**: A1 and A2 Bytes in the Tx Line Port Data are generated internally and placed in Tx TOH Insert RAM Locations for µPro Read.	Outgoing Line Data contains A1 and A2 Bytes from Tx TOH Insert RAM Locations.	See TFRMEXT.
	6	TRERR	**Tx Parity Error Control**: Automatic reset of Tx Side B1, B2 and B3 Error Masks after one frame.	Automatic reset of Error Masks disabled.	
	5	STPAIS	**Tx Path AIS Control**: Path AIS inserted in Tx Line Port Data.	Insertion of Path AIS in Tx Line Port Data not forced.	See TRAIS.
	4	Unused			Note 1.
	3	RE2A	**Rx E1 to AIS Mode Control**: E1 Byte incoming at Rx Line Port interpreted as AIS Indication.	E1 Byte incoming at Rx Line Port not interpreted as AIS Indication.	See RLE1.

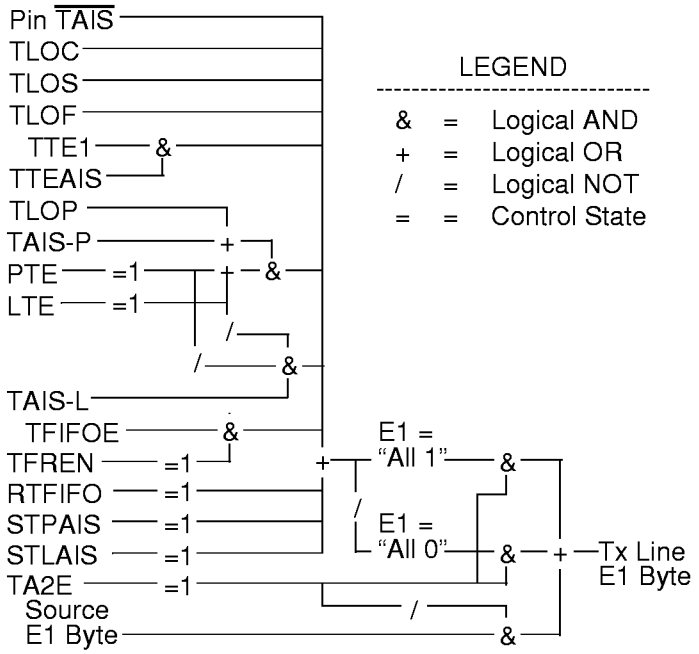
Address [H]	Bit	Symbol	Conditions		Comments
			Bit Equal to "1"	Bit Equal to "0"	
1FB (cont.)	2	RA2E	**Rx AIS to E1 Mode Control**: E1 Byte outgoing at Rx Terminal Port used for AIS Indication.	E1 Byte outgoing at Rx Terminal Port not used for AIS Indication.	
	1	TE2A	**Tx E1 to AIS Mode Control**: E1 Byte incoming at Tx Terminal Port interpreted as AIS Indication.	E1 Byte incoming at Tx Terminal Port not interpreted as AIS Indication.	

Rx Terminal E1 Alarm Insertion



Address [H]	Bit	Symbol	Conditions		Comments
			Bit Equal to "1"	Bit Equal to "0"	
1FB (cont.)	0	TA2E	**Tx AIS to E1 Mode Control**: E1 Byte outgoing at Tx Line Port used for AIS Indication.	E1 Byte outgoing at Tx Line Port not used for AIS Indication.	

Tx Line E1 Alarm Insertion



Note:
1. Unused bits are to be written to "0".

CONTROL REGISTER 12

Address [H]	Bit	Symbol	Conditions		Comments
			Bit Equal to "1"	Bit Equal to "0"	
1FC	7	TFREN	**Tx FIFO Reset Enable**: Automatic recovery from Tx FIFO under/over flow enabled.	Automatic recovery from Tx FIFO under/over flow disabled.	Note 2.
	6	RTFIFO	**Reset Tx FIFO**: Rising edge causes a reset of the Tx FIFO. Control bit is reset to "0" upon completion of operation.	Normal operation.	Note 2.
	5	DISTLAIS	**Disable Tx Line AIS Detection**: Detection of AIS-L at Tx Terminal Port disabled.	Detection of AIS-L at Tx Terminal Port enabled.	
	4	LPAISEN	**Loopback AIS Generation Enable**: Generate AIS in Tx Line Port Data during Tx-Rx Loop.	Looped data is output at Tx Line Port during Tx-Rx Loop.	Note 3.
	3	LPAISSEL	**Loopback AIS Select**: AIS-L generated (all Bytes = "1" except the 9 SOH Bytes).	AIS-P Generated (H1, H2, H3, and all POH Bytes = "1").	Effective only if LPAISEN = "1".
	2	TFRIEN	**Tx Frame Reference Input Enable**: Failure at $\overline{\text{TFRI}}$ pin included in LOTR equation.	Status of $\overline{\text{TFRI}}$ Pin disregarded in LOTR equation.	
	1-0	Unused			Note 1.

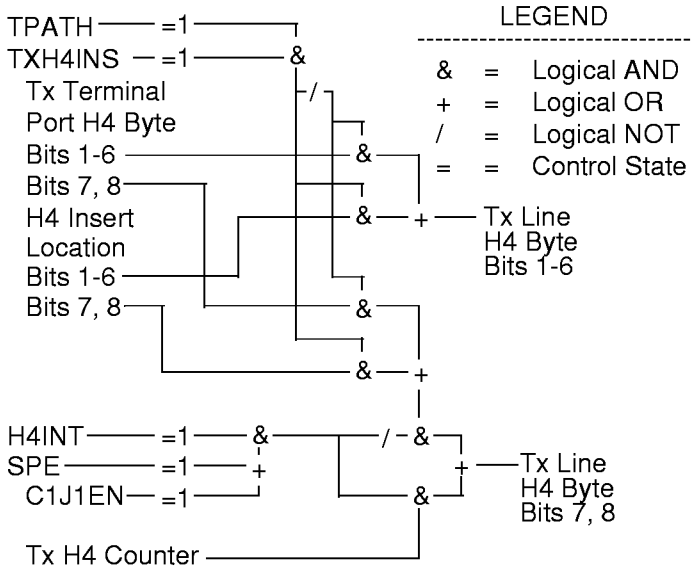
Notes:

1. Unused bits are to be written to "0".
2. The following operations are performed during a Tx FIFO Reset:
   (1) AIS-P output at Tx Line Port,
   (2) FIFO is re-centered,
   (3) New Pointer Value is calculated,
   (4) AIS-P is terminated with the New Pointer value and active NDF indication.
3. This control is only enabled if TRLOOP = "1".

CONTROL REGISTER 13

Address [H]	Bit	Symbol	Conditions		Comments
			Bit Equal to "1"	Bit Equal to "0"	
1FD	7-4	Unused			Note 1.
	3	TXH4INS	**Tx H4 Byte Control**: Outgoing Line Data contains H4 Byte from Tx POH Insert RAM Location.	Outgoing Line Data contains H4 Byte from the Tx Terminal Port.	
	2-0	Unused			Note 1.

Tx Line H4 Byte Selection



Note:
1. Unused bits are to be written to "0".

CONTROL REGISTER 14

Address [H]	Bit	Symbol	Conditions		Comments
			Bit Equal to "1"	Bit Equal to "0"	
1FE	7	TFRMEXT	**Tx Framing Bytes External Control**: Insert Tx TOH RAM Locations contain A1 and A2 Bytes from Tx TOH Port.	Insert Tx TOH RAM Locations for A1 and A2 Bytes written by µPro.	Notes 1 and 2. See TRFRM.
	6	TXC1EXT	**Tx C1/J0 Byte External Control**: Insert Tx TOH RAM Location(s) contains C1 Byte(s) from Tx TOH Port.	Insert Tx TOH RAM Location(s) for C1 Byte(s) written by µPro.	Notes 1 and 2. See TRC1 and J0EN(0,1).
	5	TXE1EXT	**Tx E1 Byte External Control**: Insert Tx TOH RAM Location contains E1 Byte from Tx TOH Port.	Insert Tx TOH RAM Location for E1 Byte written by µPro.	Notes 2 and 3. See TRE1.
	4	TXF1EXT	**Tx F1 Byte External Control**: Insert Tx TOH RAM Location contains F1 Byte from Tx TOH Port.	Insert Tx TOH RAM Location for F1 Byte written by µPro.	Notes 1 and 2. See TRF1.
	3	TXSDEXT	**Tx D1-D3 Bytes External Control**: Insert Tx TOH RAM Locations contain D1-D3 Bytes from Tx TOH Port or Tx Section DCC Port.	Insert Tx TOH RAM Locations for D1-D3 Bytes written by µPro.	Note 2. See TRSD and SDCCEN.
	2	TXZ1EXT	**Tx Z1 Byte External Control**: Insert Tx TOH RAM Location contains Z1 Byte from Tx TOH Port.	Insert Tx TOH RAM Location for Z1 Byte written by µPro.	Notes 1 and 2. See TRZ1.
	1	TXZ2EXT	**Tx Z2 Byte External Control**: Insert Tx TOH RAM Location contains Z2 Byte from Tx TOH Port.	Insert Tx TOH RAM Location for Z2 Byte written by µPro.	Notes 1 and 2. See TRZ2.
	0	TXE2EXT	**Tx E2 Byte External Control**: Insert Tx TOH RAM Location contains E2 Byte from Tx TOH Port.	Insert Tx TOH RAM Location for E2 Byte written by µPro.	Note 2. See TRE2.

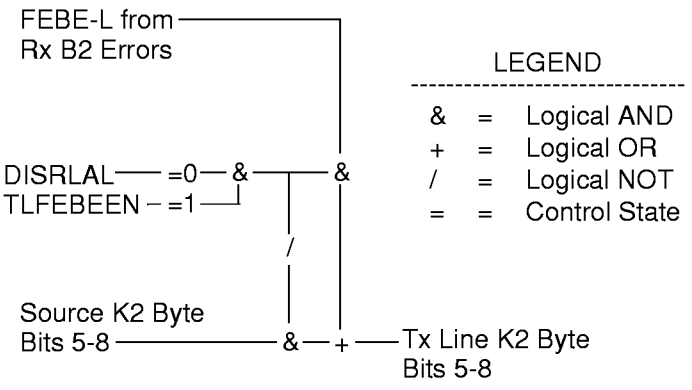
Notes:

1. If OA = "1", Control is disabled and BIT EQUAL TO "0" condition applies.
2. The settings for the appropriate 1^{ST} Level Control (TRFRM, TRC1, TRE1, TRF1, TRSD, TRZ1, TRZ2 or TRE2) must be such that the Tx TOH Insert RAM Location(s) is(are) enabled for output at the Tx Line Port.
3. This control is only enabled if TA2E = "0".

CONTROL REGISTER 15

Address [H]	Bit	Symbol	Conditions		Comments
			Bit Equal to "1"	Bit Equal to "0"	
1DF	7	TXLDEXT	**Tx D4-D12 Bytes External Control**: Insert Tx TOH RAM Locations contain D4-D12 Bytes from Tx TOH Port or Tx Section DCC Port.	Insert Tx TOH RAM Locations for D4-D12 Bytes written by µPro	See TRLD and LDCCEN.
	6	TSWRES	**Tx Software Reset**: Resets all Tx Side counters, and clears Tx Side Status Bits. Normal operation is inhibited.	Cancels Tx Side Reset. Normal operation resumed.	
	5	TTEAIS	**TTEI AIS Enable**: TTEI condition included in equations for AIS-P and AIS-L insertion at Tx Line Port.	TTEI condition excluded from equations for AIS-P and AIS-L insertion at Tx Line Port.	See TRAIS.
	4	TLFEBEEN	**Line FEBE Enable**: Tx Side - K2 Byte, Bits 5-8 in the Tx Line Port Data are overwritten by FEBE-L derived from Rx B2 Byte.	Tx Side - K2 Byte, Bits 5-8 in the Tx Line Port Data are not overwritten.	
	3	INHTB1C	**Inhibit Tx B1 Counter**: Accumulation of B1 errors at Tx Terminal Port inhibited.	Accumulation of B1 errors at Tx Terminal Port enabled.	
	2	INHTB2C	**Inhibit Tx B2 Counter**: Accumulation of B2 errors at Tx Terminal Port inhibited.	Accumulation of B2 errors at Tx Terminal Port enabled.	

Tx Line FEBE-L Insertion



Address [H]	Bit	Symbol	Conditions		Comments
			Bit Equal to "1"	Bit Equal to "0"	
1DF (cont.)	1	STLRDI	**Send Tx Line RDI**: RDI-L inserted in Tx Line Port output data.	Insertion of RDI-L at Tx Line Port Data not forced.	See TRLRDI.
	0	B2ELRDI	**B2 Excess BER Line RDI Enable**: Excess B2 Error condition included in equation for RDI-L insertion at Tx Line Port.	Excess B2 Error condition excluded from equation for RDI-L insertion at Tx Line Port.	Note 1. See TRLRDI.

Note:
1. If B2RATE(2-0) = "110" or "111", control is disabled and BIT EQUAL TO "0" condition applies.

CONTROL REGISTER 16

Address [H]	Bit	Symbol	Conditions		Comments
			Bit Equal to "1"	Bit Equal to "0"	
0FF	7	Unused			Note 1.
	6	PRDISEL	**Path RDI Select**: RDI-P indication must be received for 5 consecutive frames for alarm declaration.	RDI-P indication must be received for 10 consecutive frames for alarm declaration.	
	5	B2RATE2	**B2 Excess BER Rate Parameter**: Supplies the exponent for the B2BLK Parameter and disables the B2 Excess BER function.		B2 Excess BER calculation must be disabled when Parameters or B2 Rate are changed.
	4	B2RATE1			
	3	B2RATE0			
	2	B3RATE2	**B3 Excess BER Rate Parameter**: Supplies the exponent for the B3BLK Parameter and disables the B3 Excess BER function.		B3 Excess BER calculation must be disabled when Parameters or B3 Rate are changed.
	1	B3RATE1			
	0	B3RATE0			

B2RATE2	B2RATE1	B2RATE0	Function
0	0	0	10^0
1	1	-	disabled

B3RATE2	B3RATE1	B3RATE0	Function
0	0	0	10^0
1	1	-	disabled

Note:
1. Unused bits are to be written to "0".

CONTROL REGISTER 17

Address [H]	Bit	Symbol	Conditions		Comments
			Bit Equal to "1"	Bit Equal to "0"	
1DD	7	SDCCEN	**Section Datacom Select**: External D1-D3 Bytes are accepted from the Tx TOH Port.	External D1-D3 Bytes are accepted from the Tx Section DCC Port.	Note 1. See TRSD and TXSDEXT
	6	LDCCEN	**Line Datacom Select**: External D4-D12 Bytes are accepted from the Tx TOH Port.	External D4-D12 Bytes are accepted from the Tx Line DCC Port.	Note 1. See TRLD and TXLDEXT.
	5	STLAIS	**Send Tx Line AIS**: AIS-L inserted in Tx Line Port Data.	Insertion of AIS-L in Tx Line Port Data not forced.	See TRAIS.
	4	TEST1	**TXC Test Mode 1**: Test active.	Normal operation.	Note 2.
	3	TEST2	**TXC Test Mode 2**: Test active.	Normal operation.	Note 2.
	2	LINLOOP	**Line Loopback**: Rx Line input looped back to Tx Line output.	Normal operation.	
	1	DISTB2R	**Disable Tx B2 Recalculation**: B2 Byte input at Tx Terminal Port is output at Tx Line Port.	B2 Byte output at Tx Line Port is calculated.	
	0	TPRDI20	**Transmit Path RDI 20 Times**: RDI-P sent for 20 frames or the duration of the causative event, whichever is longer.	RDI-P is sent for the duration of the causative event.	

Notes:
1. If OA = "1", control is disabled and BIT EQUAL TO "0" condition applies.
2. Test bits are to be written to "0".

CONTROL REGISTER 18

Address [H]	Bit	Symbol	Conditions		Comments
			Bit Equal to "1"	Bit Equal to "0"	
1DC	7	J0RWEN	**J0 Read/Write Enable**: J0 Bytes accessed by µPro at addresses 080[H] - 0BF[H] (Rx Port J0 RAM Location) and 180[H] - 1BF[H] (Tx J0 Insert RAM Location).	J1 Bytes accessed by µPro at addresses 080[H] - 0BF[H] (Rx Port J1 RAM Location) and 180[H] - 1BF[H] (Tx J1 Insert RAM Location).	Effective only if J0EN(1,0) = "1-".
	6	J0MLRDI	**J0 Mismatch Line RDI Enable**: J0 Mismatch condition included in equation for RDI-L insertion at Tx Line Port.	J0 Mismatch condition excluded from equation for RDI-L insertion at Tx Line Port.	Effective only if J0EN(1,0) = "01". See TRLRDI.
	5	J0MLAIS	**J0 Mismatch Line AIS Enable**: J0 Mismatch condition included in equation for AIS-L insertion at Rx Terminal Port.	J0 Mismatch condition excluded from equation for AIS-L insertion at Rx Terminal Port.	Effective only if J0EN(1,0) = "01".
	4 3	J0EN1 J0EN0	**J0 Enable(1,0)**: Selects the J0 processing, as shown below: J0EN1 J0EN0 Function 0 0 J0 processing inhibited. The Byte following A2 is a C1 Byte. 0 1 Single Byte J0 processing: J0MIS declared if Rx Side mismatch. 1 0 16 or 64 byte message received and transmitted with incoming message (at Rx Line Port, Tx TOH Port, or Tx Terminal Port) stored in rotating fashion with no specific starting point. 1 1 64 byte message received and transmitted with incoming message (at Rx Line Port, Tx TOH Port, or Tx Terminal Port) stored such that the byte following ASCII (CR) and (LF) characters is stored in the Lowest address location.		Notes 2 and 3. See J0RWEN, TRC1 and TXC1EXT.
	2-1	Unused			Note 1.
	0	CHPRES	**Chip Reset**: Similar to Device Reset (Pin RST) except that Control Register settings are not affected. Normal operation is inhibited.	Cancels Chip Reset. Normal operation resumed.	

Notes:
1. Unused bits are to be written to "0".
2. If J0EN1 = "0", the Rx Line C1/J0 RAM Location is 01C[H] and the C1/J0 Tx Insert RAM Location is 13C[H].
3. If J0EN1 = "1", the Rx Line J0 Message RAM locations are accessed at 080[H] - 0BF[H] and the J0 Message Tx Insert RAM Locations are accessed at 180[H] - 1BF[H].

CONTROL REGISTER 19

Address [H]	Bit	Symbol	Conditions		Comments
			Bit Equal to "1"	Bit Equal to "0"	
1DB	7	Reserved			Note 1.
	6	Reserved			Note 1.
	5	TPRDISD	**Transmit Path RDI-SD**: RDI-PSD inserted in Tx Line Port Data.	RDI-PSD not forced in Tx Line Port Data.	Note 2.
	4	TPRDICD	**Transmit Path RDI-CD**: RDI-PCD inserted Tx Line Port Data.	RDI-PCD not forced	Note 2.
	3	TPRDIPD	**Transmit Path RDI-PD**: RDI-PPD inserted in Tx Line Port Data.	RDI-PPD not forced.	Note 2.
	2	B3PRDISD	**B3 Excess BER Path RDI-SD Enable**: Excess B3 Error condition included in equation for RDI-PSD insertion at Tx Line Port.	Excess B3 Error condition excluded from equation for RDI-PSD insertion at Tx Line Port.	
	1	B3PRDICD	**B3 Excess BER Path RDI-CD Enable**: Excess B3 Error condition included in equation for RDI-PCD insertion at Tx Line Port.	Excess B3 Error condition excluded from equation for RDI-PCD insertion at Tx Line Port.	
	0	TOHPRDISD	**TOH Alarms Path RDI-SD Enable**: TOH conditions (RLOC, RLOS, RLOF, RAIS-P) included in equation for RDI-PSD insertion at Tx Line Port.	TOH condition excluded from equation for RDI-PSD insertion at Tx Line Port.	

Notes:
1. Reserved bits must be written to "0".
2. RDI-PxD is inserted at the Tx Line Port by overwriting the selected bits of the G1 Byte. See TPRDIEN.

OPERATION

In this section the following nomenclature is used to identify memory locations:

(CRx; $y^{256}y^{16}y^{0}$[H], Bit z), (SRx; $y^{256}y^{16}y^{0}/y^{0}/y^{0}$[H], Bit z), and $y^{256}y^{16}y^{0}$[H]

where: CRx = Control Register number x (0-19)

SRx = Status Register number x (0-9)

$y^{256}y^{16}y^{0}$ = the address in Hex (000[H]-FFF[H])

z = the Bit Number (0-7)

In the text which follows, the first occurrence of a Control Bit, Status Bit or Memory Location will be identified as described above. Subsequent references to that entity will not have the location identified. The locations of all Control and Status Bits can be found on pages 55 and 61.

PRIMARY OPERATING MODES

The SOT-1 may be operated in either of two Primary Operating Modes (P.O.M.):

1. SONET 2. SPE-only

The P.O.M. of the device determines the form and content of the information at the Rx and Tx Terminal Ports.

In SONET Mode, the Terminal Side information consists of the full SONET Format (TOH and SPE consisting of POH and Payload). The Control Signals are used to differentiate between the TOH and SPE portions. The Rx Terminal Port Data, Clock and Control Signals are all outputs. The Tx Terminal Port Data, Clock and Control Signals are all inputs. When this mode of operation is used an external source is required to create the Tx Terminal Port Clock and Control signals (TTCI or TPCI, TSYNI, and TSPEI).

The Terminal I/O in SPE-only mode consists only of the SPE portion of the SONET signal. The TOH Bytes are not present. The Rx Terminal Port Data, Clock and Control Signals are all outputs. The Tx Terminal Port Data, Clock and Control Signals are all inputs. When this mode of operation is used an external source is required to create the Tx Terminal Port Timing and Control Signals.

In SONET mode, the Rx Terminal Port provides both Serial and Parallel outputs (51.84 Mb/s and 6.48 Mb/s) and the Tx Terminal Port can be configured for Serial operation at 51.84 Mb/s or Parallel operation at 6.48 Mb/s. When SPE-only mode is selected, Rx and Tx Terminal Port operation is restricted to Serial I/O. The control SPE (CR10; 1FA[H], Bit 7) is used to define the P.O.M. Serial or parallel operation is invoked with the control PARA (CR2; 0FA[H], Bit 6).

There are two additional Tx Terminal Port Modes that are invoked when SONET Mode is selected. These are C1J1 Mode and Framing Mode. They are controlled by C1J1EN (CR6; 0FE[H], Bit 1). When set to "1", Frame Delineation is accomplished with the signals TSYNI and TSPEI. When set to "0", the incoming A1/A2 and H1/H2 Bytes are used to determine Frame and SPE alignment. The interaction of the SPE, PARA and C1J1En hierarchical in nature, as shown in Table 1.

The interaction of the SPE, PARA and C1J1EN controls is hierarchical in nature, as shown in Table 1.

Table 1. Primary Operating Modes

SPE	C1J1EN	PARA	P.O.M.
0	0	0	Serial SONET Framing
0	0	1	Parallel SONET Framing
0	1	0	Serial SONET C1J1
0	1	1	Parallel SONET C1J1
1	-	0	SPE-only

TIMING GENERATORS

The SOT-1 contains two timing generators. They are the Terminal Timing Generator and the Line Timing Generator. These reside in the Receive Side and Transmit Side, respectively. A common set of pins TLCI and $\overline{\text{TFRI}}$ provide external reference inputs for both timing generators.

Terminal Timing Generator

The Terminal Timing Generator (TTG) creates the signals required for the Rx Re-timing FIFO (when Receive Re-timing is enabled), the Rx Terminal Generator, and the Rx Terminal Port. The use of $\overline{\text{TFRI}}$ is optional. If a frame pulse is not supplied, the start of the frame generated at the Rx Terminal Port will be arbitrary. If it is not used, RRFIEN (CR3; 0FB[H], Bit 7) should be set to "0" to prevent alarm generation. When employed, the generated frame will track the reference frame. If $\overline{\text{TFRI}}$ fails, the alignment of the generated frame will be maintained. Any change in position of $\overline{\text{TFRI}}$ is reported as Rx Reference Change of Frame Alignment - RRCOFA (SR4; 1F2/3/5[H], Bit 7). The Loss Of Rx Reference (TLCI and/or $\overline{\text{TFRI}}$) is reported as LORR (SR4; 1F2/3/5[H], Bit 6).

In addition to the external signals mentioned above, the TTG may also utilize internal signals generated by the Rx TOH Processor. These internal signals are referred to as RXCK (51.84 Mb/s clock) and $\overline{\text{RXFR}}$ (frame). The availability of internal or external inputs to the TTG provides two Receive Timing Modes: Line Timing or External Rx Timing. Timing mode selection is controlled by RCLK (CR10; 1FA[H], Bit 5). When set to "1", External Rx Timing mode is selected. RCLK = "0" selects Line Timing mode.

Line Timing Generator

The Line Timing Generator (LTG) creates the signals required for the Tx Re-timing FIFO (when Transmit Re-timing is enabled) and the Tx Line OH Generator. The use of $\overline{\text{TFRI}}$ is optional. If it is not used the start of the frame output at the Tx Line Port will be arbitrary. If $\overline{\text{TFRI}}$ is not used, the control TFRIEN (CR12; 1FC[H], Bit 2) should be set to "0" to prevent alarm generation. Loss Of Tx Reference is reported as LOTR (SR5; 1E8/9/C[H], Bit 1).

The timing source for the Tx Line may be either the external references TLCI and $\overline{\text{TFRI}}$, or, in Serial SONET Mode, the Tx Terminal Port signals TTCI and TSYNI. The first option is referred to as External Tx Timing. The latter option constitutes Terminal Timing. The selection is controlled by TCLK (CR10; 1FA[H]. When set to "1", External Tx Timing is selected. A setting of "0" results in Terminal Timing. If the P.O.M. is Parallel SONET and TCLK is set to "0", then External Tx Timing will be forced and TLCI and $\overline{\text{TFRI}}$ must be supplied with the relationship shown in Figure 18 (page 31). The TCLK = "0" setting is used in those special applications where the line clock (TLCO) needs to be synchronous with the terminal clock (TPCI) so that either Tx re-timing can be turned off (TXRTM = "0") or some of the Tx Terminal TOH bytes (TPPI(0-7)) can be passed to the Tx line output (TLDO). When present, $\overline{\text{TFRI}}$ or TSYNI is used to synchronize the transmitted frame to the reference frame. The Transmit frame will always track the Reference Frame. As long as the associated clock (TLCI or TTCI) input is valid, loss of the framing pulse does not impair the output at the Tx Line. The Frame alignment prior to the framing pulse loss will be maintained. Any frame pulse ($\overline{\text{TFRI}}$) that varies from the previous position will be reported as a Transmit Reference Change Of Frame Alignment - TRCOFA (SR5; 1E8/9/C[H], Bit 3). In SONET Mode, if C1J1EN = "0", the A1 and A2 Bytes of the Input Signal at the Tx Terminal Port may be used for Frame Delineation instead of TSYNI. If Terminal Timing is selected, with this option enabled, the start of the generated Tx Line Port Frame will be determined by the A1 and A2 bytes and not by TSYNI.

RE-TIMING

Re-timing can be independently selected in the Transmit and Receive Sides. When not enabled, the Rx Re-timing and/or Tx Re-timing FIFOs are bypassed.

Rx Side

Receive re-timing is always performed in SPE-only Mode. Receive Re-timing is an option for Serial or Parallel SONET Modes. Receive re-timing is controlled by RCLK, and $\overline{\text{RXRTM}}$ (CR9; 1F9[H], Bit 1). As shown in Table 2, the interaction of these bits is hierarchical in nature.

Table 2. Rx Re-Timing Control

P.O.M.	RCLK	$\overline{\text{RXRTM}}$	Rx Re-Timing
SPE-only	1/0	-	Enabled
Serial and Parallel SONET	0	0	Enabled
	0	1	Disabled
	1	-	Enabled

When Rx Re-timing is performed, the Rx Re-timing FIFO is the elastic store between the Rx POH Processor and the Rx Terminal Generator. The inputs to the FIFO are the SPE Portion of the Rx Line signal. Information is clocked in at the line rate. The Terminal Timing Generator provides the read clock and the signals necessary for Pointer Generation. The new Pointer is calculated and Positive or Negative Justifications are made, as necessary, to prevent FIFO overflow or underflow. The values placed in the "SS" Bit positions of the H1 Byte are determined by the controls S0 and S1 (CR6; 0FE[H], Bits 2 and 3). All justifications are accumulated by the Local PJ Counter (022[H]). Counter overflow is indicated by LPJOF (SR7; 0F6[H], Bit 0). FIFO underflow or overflow is reported as Rx FIFO Error - RFIFOE (SR4; 1F2/3/5[H], Bit 5). Automatic recovery from an underflow or overflow condition can be enabled with RFREN (CR3; 0FB[H], Bit 6). The FIFO may also be re-centered with RRFIFO (CR3; 0FB[H], Bit 5).

Tx Side

Transmit re-timing is always performed in SPE-only Mode, SONET Mode where TSYNI is enabled, and when TCLK = "1". It is an option for SONET Modes having valid A1, A2, H1, and H2 Bytes at the Tx Terminal Port. Transmit re-timing is controlled by the bits TCLK, C1J1EN, and TXRTM (CR10; 1FA[H], Bit 3). As shown in Table 3, the interaction of these bits is hierarchical in nature.

Table 3. Tx Re-Timing Control

P.O.M.	TCLK	C1J1EN	TXRTM	Tx Re-Timing
SPE-only	-	-	-	Enabled
Serial or Parallel SONET	0	0	0	Disabled
	0	0	1	Enabled
	0	1	-	Enabled
	1	-	-	Enabled

The Tx Re-timing FIFO is the elastic store between the Tx Terminal Processor and the Tx OH Generator, when re-timing is performed. The inputs to the FIFO are the SPE Portion of the Tx Terminal Signal. Information is clocked in at the terminal rate. The LTG provides the read clock and the signals necessary for Pointer Generation. The new Pointer is calculated and Positive or Negative Justifications are made, as necessary, to prevent FIFO overflow or underflow. The values used for the H1 Byte "SS" bits are determined by the controls S0 and S1. Pointer Increments and Decrements can be forced with INC and DEC (CR10; 1FA[H], Bits 1 and 0)[1]. FIFO underflow or overflow is reported as Tx FIFO Error - TFIFOE (SR5; 1E8/9/C[H], Bit 0). Automatic recovery from an underflow or overflow condition can be enabled with TFREN (CR12; 1FC[H], Bit 7). The FIFO may also be re-centered with RTFIFO (CR12; 1FC[H], Bit 6).

LINE FORMATS

The Line Formats for the SOT-1 are designed for use in two applications. The first is for use in a native STS-1 Environment. The second is for use in a situation where the SOT-1 is preceded, on the Line Side, by additional circuitry such as an STS-1 to STS-N multiplexer. The choice of applications is controlled by STS1 (CR2; 0FA[H], Bit 7). When set to "1", the Line Side signals are treated as an STS-1.

Rx Line Port Format

The inputs at the Rx Line Port are RLDI, $\overline{\text{RFRI}}$, RLCI and $\overline{\text{RXLOS}}$. RLDI and $\overline{\text{RFRI}}$ are clocked in on the Rising Edge of RLCI. $\overline{\text{RXLOS}}$ is an optional asynchronous input from an external LOS detector.

If STS1 = "1":

1. Full framing is performed using the A1 and A2 Bytes and $\overline{\text{RFRI}}$ is ignored.
2. The B1 Errors are calculated using the B1 Byte.
3. Unscrambling is performed.

1. These features must be used judiciously. If either is enabled, disabling must occur within 2 Frames to prevent multiple PJs. In addition, consecutive, forced PJs may cause FIFO spills.

If STS1 = "0":

1. The input $\overline{\text{RFRI}}$ is enabled and a partial framing algorithm is employed where the A1 and A2 Bytes are used to verify the frame position defined by $\overline{\text{RFRI}}$.
2. The content of the B1 Byte is interpreted as a count of B1 Errors.
3. Unscrambling is not performed.

Tx Line Port Format

The Tx Line Port Outputs are TLDO and TLCO, where TLDO is clocked out on the Falling Edge of TLCO.

If STS1 = "1"

1. B1 Parity is calculated and placed in the B1 Byte.
2. Scrambling is performed.

If STS1 = "0"

1. The outgoing B1 Byte contains a mask that can be used to create B1 Parity errors.
2. Scrambling is not performed.

The relationship between TLCO, TLDO, and the reference inputs used by the LTG is shown in Figure 35. When External Transmit Timing is employed, the MSB of the A1 Byte occurs 3½ bit times after $\overline{\text{TFRI}}$ is sampled. If Terminal Timing is employed the MSB of the A1 Byte is as follows:

1. C1J1EN = "0" - 22½ bit times after the MSB of the A1 Byte input at TTDI is sampled by TTCI
2. C1J1EN = "1" - 6½ bit times after the Rising Edge of TSYNI and the Falling Edge of TSPEI is sampled by TTCI

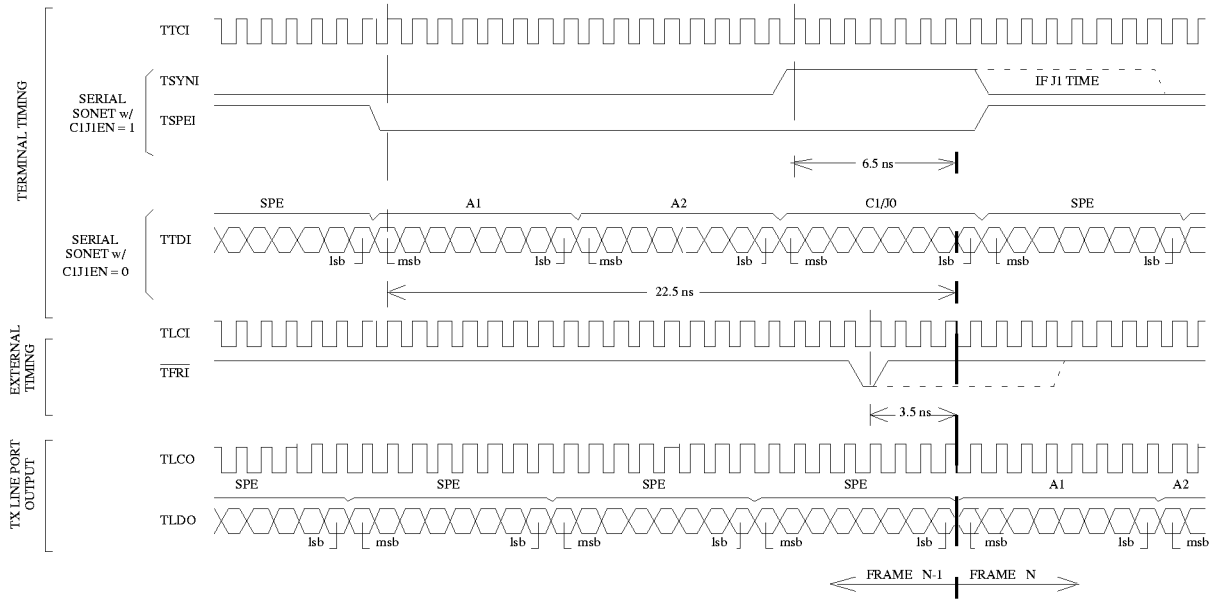


Figure 35. Tx Line Format

TERMINAL FORMATS

All of the following descriptions assume that the generated frame is synchronized to a reference frame pulse. If the applicable reference frame signal is not provided, then the start of the generated frame at the Rx Terminal Port will be arbitrary.

Serial SONET

The Rx Terminal Port Serial SONET Format is shown in Figure 36. The Reference inputs may be either TLCI/$\overline{\text{TFRI}}$ or RXCK/$\overline{\text{RXFR}}$. The external reference frame pulse ($\overline{\text{TFRI}}$) may be from one to eight clock periods in duration. The relationship between the external reference and the generated frame is variable and is controlled by RTDSEL (CR10; 1FA[H], Bit 2). RTDO is output on the Falling Edge of RTCO. The order of output is MSB → LSB. RSPE is Low during the TOH Byte Times. RSYN is High during the C1, J1, and, optionally, V1 Byte times. The V1 Byte time option is enabled when the control H4INT (CR6; 0FE[H], Bit 5) is set to "1".

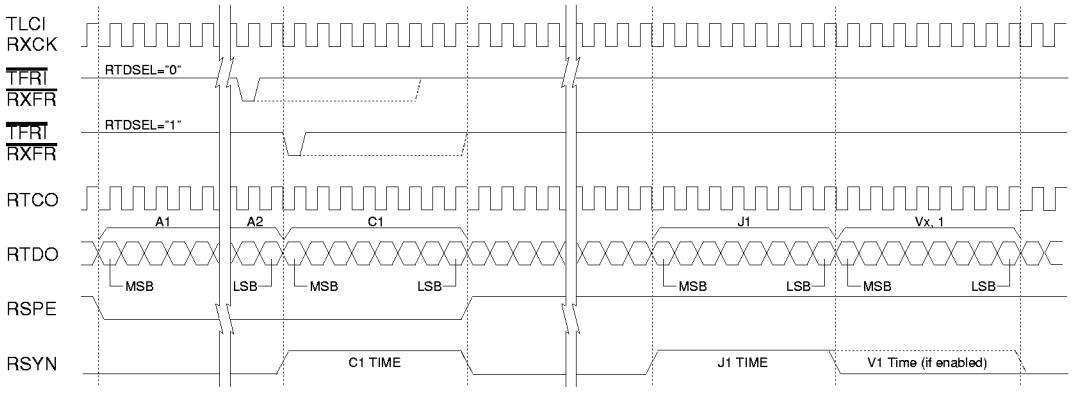


Figure 36. Rx Terminal Port Serial SONET Format

The Tx Terminal Port Serial SONET Format is shown in Figure 37. TTCI is the 51.84 Mb/s input clock. TTDI is the serial data where the order of input is MSB → LSB. TTDI, TSPEI, and TSYNI are clocked in on the Rising Edge of TTCI. Input Frame Delineation is controlled by C1J1EN. When set to "0", TSYNI and TSPEI are disregarded and the incoming A1/A2 and H1/H2 Bytes are used to determine Frame and SPE alignment. If C1J1EN = "1", the information content of the A1, A2, H1, and H2 Bytes is disregarded and TSPEI and TSYNI are enabled. TSPEI is Low during the TOH Byte Times. TSYNI is High during the C1, J1, and, optionally, V1 Byte times. The V1 Byte time option is enabled when the control H4INT is set to "1".

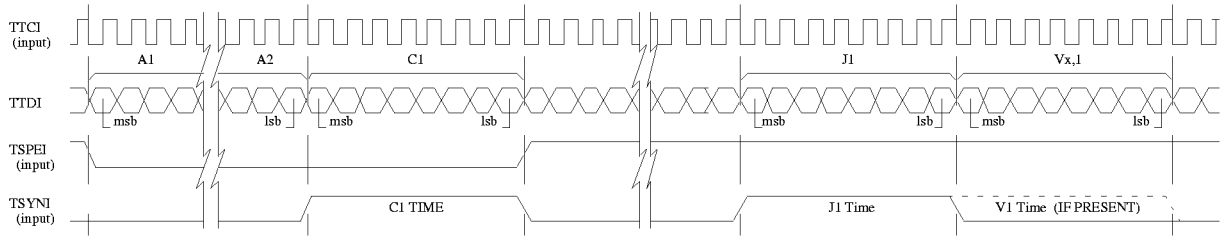


Figure 37. Tx Terminal Port Serial SONET Format

Parallel SONET

Figure 38 depicts the Rx Terminal Port Parallel SONET Format. The Reference inputs may be either TLCI/$\overline{\text{TFRI}}$ or RXCK/$\overline{\text{RXFR}}$. The external reference frame pulse ($\overline{\text{TFRI}}$) may be from one to eight clock periods in duration. The relationship between the external reference and the generated frame is variable and is controlled by RTDSEL. TPDO0 through TPDO7 are the byte wide data outputs where the LSB is TPDO0. RSPE is Low during the TOH Byte Times. RSYN is High during the C1, J1, and, optionally, V1 Byte times. The V1 Byte time option is enabled when the control H4INT is set to "1". The polarity of TPCO can be inverted with the control INVPCK (CR5; 0FD[H], Bit 3). A value of "0" results in TPDO(0-7), RSPE, and RSYN being output on the Falling Edge. When INVPCK = "1", the information is output on the Rising Edge of TPCO.

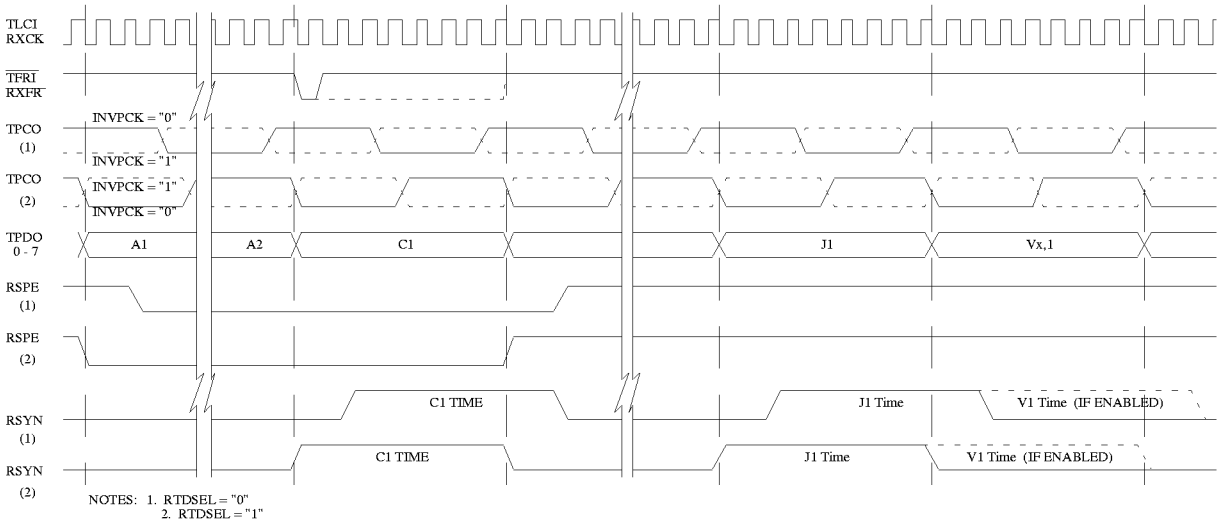


Figure 38. Rx Terminal Port Parallel SONET Format

Figure 39 depicts the Tx Terminal Port Parallel 6.48 Mb/s SONET Format. TPCI is the 6.48 Mb/s input clock. TPDI0 through TPDI7 are the byte wide data inputs where the LSB is TPDI0. When INVPCK = "0", TPDI(0-7), TSPEI, and TSYNI are clocked in on the Rising Edge of TPCI. TPDI(0-7), TSPEI, and TSYNI are clocked in on the Falling Edge of TPCI if INVPCK = "1". Input Frame Delineation is controlled by C1J1EN. When set to "0", TSYNI and TSPEI are disregarded and the incoming A1/A2 and H1/H2 Bytes are used to determine Frame and SPE alignment. If C1J1EN = "1", the information content of the A1, A2, H1, and H2 Bytes is disregarded and TSPEI and TSYNI are enabled. TSPEI is Low during the TOH Byte Times. TSYNI is high during the C1, J1, and, optionally, V1 Byte times. The V1 Byte time option is enabled when the control H4INT is set to "1".

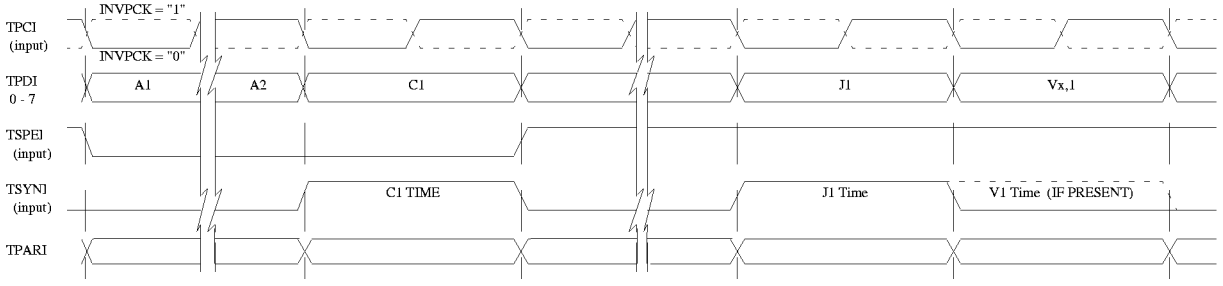


Figure 39. Tx Terminal Port Parallel SONET Format

SPE-only

Figure 40 shows the Rx Terminal Port SPE-only Format. This is a serial, 51.84 Mb/s format in which TOH Bytes are not present in the output. In their place, one bit gaps are inserted, uniformly, in the data stream. The Reference inputs may be either TLCI/$\overline{\text{TFRI}}$ or RXCK/$\overline{\text{RXFR}}$. The external reference frame pulse ($\overline{\text{TFRI}}$) may be from one to eight clock periods in duration. RTDO is output on the Falling Edge of RTCO. The order of output is MSB → LSB. RSPE is Low during the gaps in RTDO. RSYN is High during the J1 Byte time and, optionally, V1 Byte times. The V1 Byte time option is enabled when the control H4INT is set to "1". For gapping purposes, the signal is divided into nine contiguous subframes. The start of the first subframe occurs eight bit times before $\overline{\text{TLCI}}$ or $\overline{\text{RXFR}}$ transitions Low. Each subframe contains 720 bit times. Normally there will be 696 data bits per subframe. In this situation the resulting 24 gaps will be performed every 30 bits, with the first gap in the subframe occurring at the 30^{TH} Bit time. Subframes containing Pointer Decrements will contain 704 data bits and will require 16 gaps. These will be introduced every 45 bit times with the first gap occurring at the 45^{TH} bit position. Subframes containing Pointer Increments will contain 688 data bits and will require 32 gaps. These subframes will have the gaps occurring in pairs of 22 and 23 Bit times, i.e., two gaps in 45 Bit times. The first gap will occur at the 22^{ND} bit position.

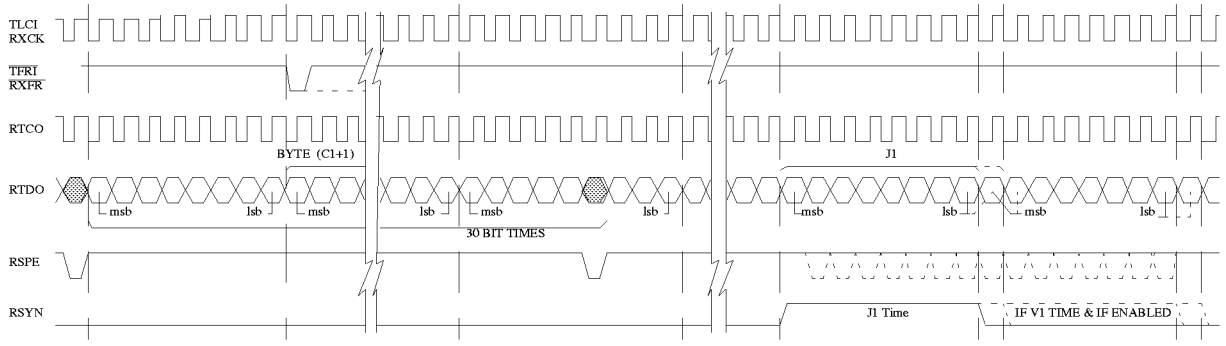


Figure 40. Rx Terminal Port SPE-only Format

The Tx Terminal Port SPE-only Format is shown in Figure 41. This is a serial, 51.84 Mb/s format in which TOH Bytes are not present. In their place, gaps are inserted in the data stream. TTDI is clocked in on the Rising Edge of TTCI. The order of input is MSB → LSB. TSPEI is Low during the gaps in TTDI. TSYNI is High during the J1 Byte time and, optionally, V1 Byte times. The V1 Byte time option is enabled when the control H4INT is set to "1". As indicated, the J1 or V1 Byte may have a gap(s) within it. For gapping purposes, the signal is divided into nine contiguous subframes. Each subframe contains 720 bit times. Normally there will be 696 data bits per subframe. This situation requires 24 gaps. Subframes containing Pointer Decrements will contain 704 data bits and will require 16 gaps. Subframes containing Pointer Increments will contain 688 data bits and will require 32 gaps. In all subframes the required gaps may occur at any time. Figure 41 depicts spacing identical to the Rx Terminal Port output.

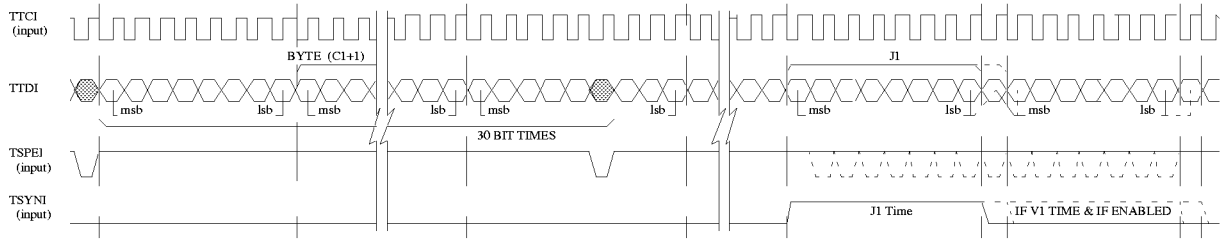


Figure 41. Tx Terminal Port SPE-only Format

EX-KX / TOH PORTS

The SOT-1 has two ports for external access to the TOH Bytes. These are the Rx and Tx Ex-Kx / TOH Ports. They may be operated in either of two operating modes. The first is OW/APS, which affords access to the E1, E2, K1, and K2 Bytes. The second operating mode is All TOH. In this mode of operation all TOH bytes are accessible. The operating mode is controlled by OA (CR6; 0FE[H], Bit 0). When set to "1", the OW/APS Mode is selected. A Logic level of "0" selects All TOH Mode. The pins for these ports are shown below.

Rx OW/APS - TOH Port			Tx OW/APS - TOH Port		
ORCO	-	Clock; 576 kb/s in OW/APS Mode 1.728 Mb/s in All TOH Mode	OTCO	-	Clock; 576 kb/s in OW/APS Mode 1.728 Mb/s in All TOH Mode
ORDO	-	Output Data	OTDI	-	Input Data
SRFR	-	E1 Byte Identifier	STFR	-	E1 Byte Identifier
LRFR	-	E2 Byte Identifier	LTFR	-	E2 Byte Identifier
$\overline{RAP}/\overline{RTS}$	-	K1, K2 Byte Strobe in OW/APS Mode A1 Byte Identifier in All TOH Mode	$\overline{TAP}/\overline{TTS}$	-	K1, K2 Byte Strobe in OW/APS Mode A1 Byte Identifier in All TOH Mode

OW/APS Mode

The Rx Ex-Kx / TOH Port operation is shown in Figure 42. All outputs occur on the Rising Edge of ORCO. The output data (ORDO) consists of the E1 Byte, four Null Bytes, the K1 Byte, the K2 Byte, one Null Byte and the E2 Byte. The order of output is MSB → LSB. SRFR and LRFR are used to identify the E1 and E2 Bytes, respectively. The position of these two signals is determined by ALTOW (CR2; 0FA[H], Bit 3). When set to a "0" value, SRFR occurs one clock period before the MSB of E1 and LRFR occurs one clock period before the MSB of E2. A Setting of "1" results in SRFR and LRFR occurring coincident with the MSB of the E1 and E2 Bytes, respectively. The signal $\overline{RAP}$ is an active low pulse that occurs one clock time after the LSB of the K2 Byte.

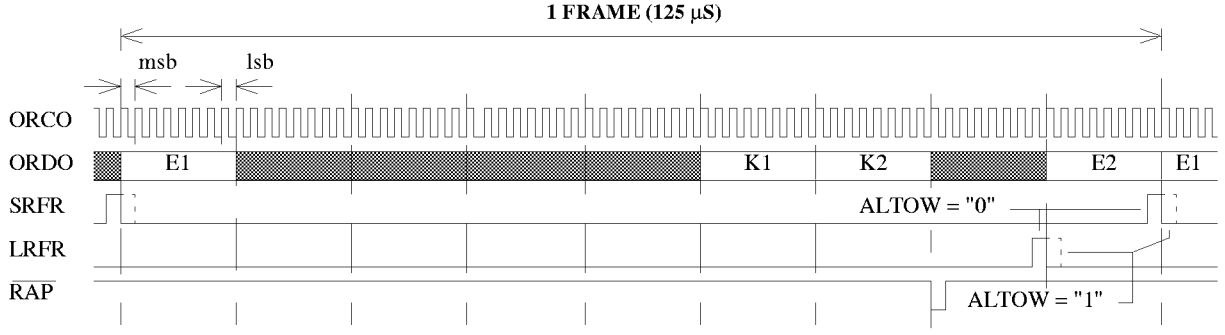


Figure 42. Rx OW/APS Port

Figure 43 depicts the operation of the Tx Ex-Kx / TOH Port. STFR and LTFR are output on the Rising Edge of OTCO. The input data (OTDI) is clocked in and $\overline{TAP}$ is clocked out on the Falling Edge. OTDI consists of the E1 Byte, one Null Byte, the K1 and K2 Bytes, three Null Bytes, the E2 Byte, and a Null Byte. The order of input is MSB → LSB. STFR and LTFR are used to identify the E1 and E2 Bytes, respectively. The position of these two signals is determined by ALTOW. When ALTOW is "0", STFR occurs 1½ clock periods before the MSB of E1 is sampled and LTFR occurs 1½ clock periods before the MSB of E2 is sampled. A Setting of "1" for ALTOW results in STFR and LTFR occurring one half clock cycle before the MSB of the E1 and E2 Bytes, respectively, is sampled. The signal $\overline{RAP}$ is an active low pulse that occurs one clock time before the MSB of the K1 Byte is sampled.

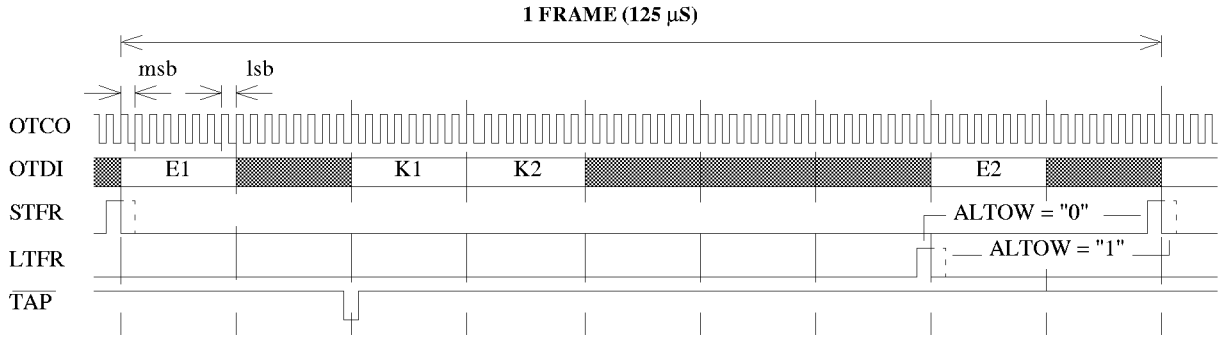


Figure 43. Tx OW/APS Port

All TOH Mode

The operation of the Rx Ex-Kx / TOH Port in All TOH Mode is shown in Figure 44. All outputs occur on the Rising Edge of ORCO. The output data (ORDO) consists of all 27 TOH Bytes. They are output in the order in which they are received from the line, with the MSB occurring first. The signal $\overline{RTS}$ is an active low pulse that occurs one clock time before the MSB of the A1 Byte. SRFR and LRFR are used to identify the E1 and E2 Bytes, respectively. The position of these two signals is determined by ALTOW. The operation is as explained above.

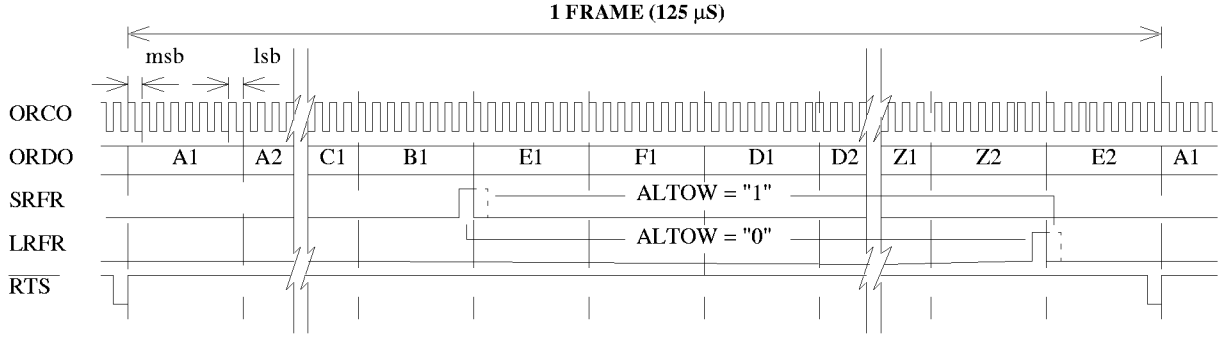


Figure 44. Rx All TOH Port

The operation of the Tx Ex-Kx / TOH Port in All TOH Mode is shown in Figure 45. STFR and LTFR are output on the Rising Edge of OTCO. The input data (OTDI) is clocked in and $\overline{TTS}$ is clocked out on the Falling Edge. OTDI consists of all 27 TOH Bytes. They are input in the order in which they are sent to the line with the MSB of each Byte occurring first. Although byte times are afforded for the B1, B2, H1, H2, and H3 Bytes, they are discarded inside the SOT-1. STFR and LTFR are used to identify the E1 and E2 Bytes, respectively. The position of these two signals is determined by ALTOW, as was explained earlier. The signal $\overline{TTS}$ is an active low pulse that occurs one clock time before the MSB of the A1 Byte is sampled.

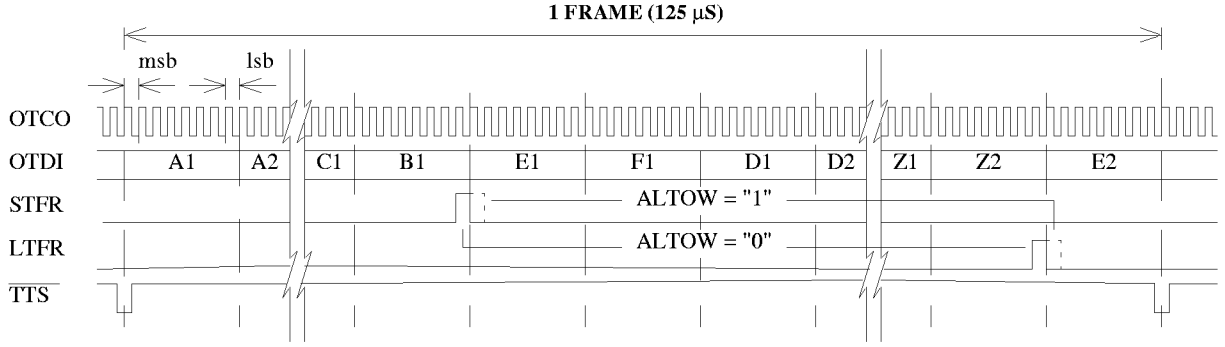


Figure 45. Tx All TOH Port

DCC PORTS

The SOT-1 has four ports that provide external access to the Datacom Channels. Two are used for the Section DCC Bytes. These are the Rx Section DCC Port and Tx Section DCC Port. The other two ports are the Rx and Tx Line DCC Ports which afford access to the Line DCC Bytes. The pins are listed below.

		Rx Section DCC Port			Rx Line DCC Port
SRCO	-	192 kb/s Clock	LRCO	-	576 kb/s Clock
SRDO	-	Output Data (serial, D1-D3 Bytes)	LRDO	-	Output Data (serial, D4-D12 Bytes)
		Tx Section DCC Port			Tx Line DCC Ports
STCO	-	192 kb/s Clock	LTCO	-	576 kb/s Clock
STDI	-	Input Data (serial, D1-D3 Bytes)	LTDI	-	Input Data (serial, D4-D12 Bytes)

SRDO and LRDO are clocked out on the Falling Edges of SRCO and LRCO, respectively. STDI and LTDI are clocked in on the Rising Edges of STCO and LTCO, Respectively. The Data is input or output in the order it is sent to or received from the line with the MSB of a byte occurring first.

RX TOH PROCESSING

The Rx TOH Processing Block is responsible for Framing, De-scrambling (if STS1 = "1"), Overhead Distribution, Overhead Processing, and Pointer Tracking. As discussed in the section "Rx Line Port Format", the external inputs are RLDI (data), RLCI (clock), $\overline{\text{RFRI}}$ (frame) and $\overline{\text{RXLOS}}$ (LOS Input). When used, $\overline{\text{RFRI}}$ consists of an active Low Pulse during the MSB Time of the C1 Byte. RLCI, RLDI, and $\overline{\text{RFRI}}$ are monitored for persistence. An absence of transitions is reported as RLOC (SR0; 0F0/1/4[H], Bit 7), RLOS[1] (SR0; 0F0/1/4[H], Bit 0), and RLFRI (SR3; 0E8/9/C[H], Bit 7), respectively. As previously discussed, external access to the Rx TOH Bytes is available at the Rx Ex-Kx / All TOH Port, the Rx Section DCC Port, and the Rx Line DCC Port.

Framing

The Framing portion detects Framing Errors - RFE (SR3; 0E8/9/C[H], Bit 6), Severely Errored Frame - RSEF (SR0; 0F0/1/4[H], Bit 1), and Loss of Frame - RLOF (SR0; 0F0/1/4[H], Bit 2). The Framer is a full off Line synchronizer, i.e., upon declaration of RSEF the previous frame alignment will be maintained until frame acquisition is completed and RSEF cleared. The framing algorithm used, when STS1 = "1", meets the Bellcore requirement that a BER of 10^{-3}, assuming a Poisson distribution of bit errors, will not cause an RSEF more than once in six minutes. If STS1 = "0", it is assumed that there is a framing device (such as an STS-n Multiplexer) between the SOT-1 and the Line. The upstream device provides the signal $\overline{\text{RFRI}}$, which is used to set the Frame Delineation Counters to the appropriate value such that the subsequent A1 and A2 Bytes may be detected at the expected positions.

Rx TOH Byte Storage

On a per frame basis, all Received TOH Bytes are written into RAM Segment 005[H] - 01F[H] for µPro access. The Memory Locations are given in Table 4.

Table 4. Received TOH Locations

	Byte	Location	Byte	Location	Byte	Location
Section	A1	016 [H]	A2	017 [H]	C1	01C [H]
	B1	014 [H]	E1	018 [H]	F1	01D [H]
	D1	005 [H]	D2	006 [H]	D3	007 [H]
Line	H1	011 [H]	H2	012 [H]	H3	013 [H]
	B2	015 [H]	K1	01E [H]	K2	01F [H]
	D4	008 [H]	D5	009 [H]	D6	00A [H]
	D7	00B [H]	D8	00C [H]	D9	00D [H]
	D10	00E [H]	D11	00F [H]	D12	010 [H]
	Z1	01A [H]	Z2	01B [H]	E2	019 [H]

1. RLOS is only a device level failure indication. It is not the Physical Medium Layer LOS Defect.

The C1, F1, K1, K2, Z1 and Z2 bytes are de-bounced. This function provides the means for detecting and reporting persistent changes that occur. De-bouncing is performed on a per byte basis and occurs over a three frame period. The values for each individual byte are compared in frames n, n-1 and n-2. Any byte that is received with a new value, and that new value is constant for three consecutive frames, will cause the indicator RTNEW (SR1; 0F2/3/5[H], Bit 6) to be set to "1". The interstitial and de-bounced values are stored in RAM and are accessible by the μPro. The Locations are given in Table 5.

Table 5. De-Bounced TOH Locations

Byte	Frame n	Frame n-1	Frame n-2	De-Bounced Value
Z1	01A [H]	04A [H]	052 [H]	05A [H]
Z2	01B [H]	04B [H]	053 [H]	05B [H]
C1	01C [H]	04C [H]	054 [H]	05C [H]
F1	01D [H]	04D [H]	055 [H]	05D [H]
K1	01E [H]	04E [H]	056 [H]	05E [H]
K2	01F [H]	04F [H]	057 [H]	05F [H]

Rx TOH Alarms

Two Transport Alarms are extracted from Bits 6-8 of the K2 Byte. Line AIS is reported as RAIS-L (SR0; 0F0/1/4[H], Bit 4) and is detected as a "111" condition. Line RDI is reported as RRDI-L (SR1; 0F2/3/5[H], Bit 3) and is detected as "110". A Received APS Alarm - RAPS (SR1; 0F2/3/5[H], Bit 2) is derived from a consistency check of the K1 Byte. Additionally, a Received Line E1 Alarm - RLE1 (SR4; 1F2/3/5[H], Bit 4) is extracted from the E1 Byte, when so optioned. RLE1 detection assumes that some upstream entity has detected an AIS condition and uses the E1 Byte for in band communication of the condition. Use of the Rx Line E1 Byte in this manner is enabled when RE2A (CR11; 1FB[H], Bit 3) is set to "1".

Rx C1/J0 Processing

In addition to the debouncing described earlier, optional processing of the C1 Byte can be performed to support J0 Functionality (Section Trace). Four forms of J0 Processing are supported. They consist of:

1. One Byte J0 Hardware Compare
2. Reception and Storage of a 16 Byte message
3. Reception and Storage of a 64 Byte message with ASCII CR/LF alignment
4. Reception and Storage of a 64 Byte message without ASCII CR/LF alignment

J0 Processing is controlled by J0EN0 and J0EN1 (CR18; 1DC[H], Bits 3 and 4)

One Byte Processing consists of comparing the content of the received C1 Byte to the value in the J0 EXPECT RAM Location (067[H]). Mismatch results in an alarm which is reported to the μPro as J0MIS (SR6; 0EA/B/D[H], Bit 3).

When multiple byte J0 options are selected, no hardware mismatch detection is performed. It is assumed that this will be performed by software. Received, multiple byte J0 messages are stored in a 64 byte RAM segment. This means that there will be four copies of a 16 byte message or one copy of a 64 byte message. The RAM Segment is accessible by the μPro through addresses 080[H] - 0BF[H]. This address space is shared by the 64 byte memory segment used to store the received J1 Bytes. The control J0RWEN (CR18; 1DC[H], Bit) is used to control the address space. When set to "1", the J0 Bytes are available.

Rx B1 Processing

B1 Errors are accumulated in an eight or sixteen bit saturating counter designated Rx B1 Err Cnt (046[H]), which is readable by the µPro. The selection of Eight Bit Mode or Sixteen Bit Mode is controlled by CNT16EN (CR3; 0FB[H], Bit 2). CNT16EN = "0" defines Eight Bit Mode. Counter overflow is indicated by RB1COF (SR7; 0F6[H], Bit 5). The manner in which B1 Byte errors are determined is dependent on the setting of STS1. When set to "0", the incoming B1 Byte may contain from zero to eight ones. Each "1" represents an error detected by an upstream device. The number of bits at the "1" Level is accumulated. If STS1 = "1", the B1 Byte extracted after unscrambling is compared to a B1 value calculated before unscrambling. The calculation is Even Parity, independently performed, in parallel, over the eight bit positions. The errors (up to eight per frame) are accumulated.

Rx B2 Processing

B2 Errors are readable by the µPro at the location Rx B2 Err Cnt (047[H]) and counter overflow is indicated by RB2COF (SR7; 0F6[H], Bit 6). They are accumulated in the same manner as with the B1 Byte, with STS1 = 1, except that the B2 calculation is performed after unscrambling and excludes the nine Section Bytes. The number of received errors (including zero) is made available to the Transmit Side for use as a Line FEBE.

Additional processing is performed to develop an Excess B2 BER Alarm. The threshold is determined by the following parameters:

B2WIN	@	Location 061[H]	B2SCV	@	Location 062[H], Bits 4-7
B2M	@	Location 060[H], Bits 0-3	B2CLR	@	Location 064[H]
B2RATE	@	CR16; 0FF[H], Bits 3-5	B2CCV	@	Location 062[H], Bits 0-3
B2SET	@	Location 063[H]			

The parameter values to be used for a 10^{-3} error rate are given in Table 6. Exceeding the programmed threshold is reported as B2EBER (SR3; 0E8/9/C[H], Bit 5).

Table 6. B2EBER Parameters

BER	B2WIN	B2M	B2RATE	B2SET	B2SCV	B2CLR	B2CCV
10^{-3}	67	1	0	39	3	28	1

The SOT-1 implements a reset window algorithm to detect and clear 1 x 10^{-3} line error rates. The recommended values provide the threshold performance shown in Table 7 under random error conditions and will resist burst errors of up to 39 STS-1 frames.

The verification of the EBER threshold detection requires the test equipment to generate truly random errors at the desired rate. Some test equipment injects error on the B2 byte itself. Such error injection is not random and does not allow for the effect of error cancellation due to double error on the same bit position of the bytes in the same frame or errors that are not counted because they happen in the section overhead bytes. Therefore, if tests are conducted by injecting error to the B2 byte, the effective random error rate is expected to be higher than the injected error rate.

Table 7. B2 Error Alarm Performance

BER	Mean time to alarm (sec)	Probability of alarm	Mean time to clear (sec)	Probability of clear
1.2×10^{-3}	0.00661	1.0		
1.0×10^{-3}	0.00734	0.97		
9.0×10^{-4}	0.00845	0.89		
7.0×10^{-4}	0.0281	0.29		
5.0×10^{-4}	9.24	0.0009		
3.0×10^{-4}			1.1×10^{3}	7.6×10^{-6}
1.0×10^{-4}			0.00658	0.98
8.0×10^{-5}			0.00575	1.0

Rx Line FEBE Processing

Processing of FEBE-L consists of recording the number of errors received in Z2 Byte Bits 5 - 8. Line FEBE Errors are accumulated in an eight or sixteen bit saturating counter designated FEBE-L Cnt (040[H]). Counter overflow is indicated by RLFEBEOF (SR7; 0F6[H], Bit 3).

Rx Pointer Tracking

The H1 and H2 Bytes are used to determine the Received J1 Position and are interpreted for:

1. New Pointer - RNPTR (SR0; 0F0/1/4[H], Bit 6)
2. Concatenation - RCPTR (SR3; 0E8/9/C[H], Bit 3)
3. Loss of Pointer - RLOP (SR0; 0F0/1/4[H], Bit 3)
4. Path AIS - RAIS-P (SR0; 0F0/1/4[H], Bit 5)
5. Pointer Increment
6. Pointer Decrement

RCPTR is not an alarm per se. Reception of a Concatenation Indication will always result in the declaration of RLOP. RCPTR serves as an indication of an illegal condition that has caused the RLOP Alarm. Pointer Increments and Decrements are accumulated in four bit Counters which are accessed at the RAM Location designated Rx Inc Cnt/Dec Cnt (045[H]). Bits 0 through 3 indicate the Decrement Count. Bits 4 through 7 are for Increments. In addition, both Pointer Increments and Decrements are accumulated in an eight bit counter which can be read by the µPro in the RXPJCNT Location (044[H]). RPMOVOF (SR7; 0F6[H], Bit 2) is the overflow indication for the Inc and Dec counters and RPJOF (SR7; 0F6[H], Bit 1) indicates overflow of RXPJCNT.

RX POH PROCESSING

All received POH processing is performed by the Rx POH Processor Block. All Received POH Bytes are written into RAM for access by the µPro. Selected bytes are debounced. Further processing is executed for alarm extraction and for performance monitoring.

Received POH Byte Locations

The Memory Locations for the Received POH Bytes are given in Table 8. The locations 080[H] - 0BF[H] are shared with the J0 bytes and access is controlled by J0RWEN. J1 Byte storage is controlled by J1SYNCEN (CR6; 0FE[H], Bit 4). When set to "0", the J1 Bytes are stored in the 64 Byte Segment, in rotating fashion, with no specific starting point. If J1SYNCEN = "1", reception of ASCII characters CR and LF, in sequence, will cause the next J1 Byte to be written at address 080[H], with subsequent bytes being stored in succeeding locations.

Table 8. Rx POH Locations

Byte	Location
J1	080 [H] - 0BF [H]
B3	0C0 [H]
C2	0C1 [H]
G1	0C2 [H]
F2	0C3 [H]
H4	0C4 [H]
Z3	0C5 [H]
Z4	0C6 [H]
Z5	0C7 [H]

The C2, F2, Z3, Z4 and Z5 bytes are de-bounced. This function provides the means for detecting and reporting persistent changes that occur. The de-bouncing operation is identical to the TOH De-bouncing Mechanism. The interstitial and de-bounced value locations are given in Table 9. Any byte that is received with a new value, and that new value is constant for three consecutive frames, will cause the indicator RPNEW (SR1; 0F2/3/5[H], Bit 5) to be set to "1".

Table 9. De-Bounced POH Locations

Byte	Frame n	Frame n-1	Frame n-2	De-bounced Value
C2	0C1 [H]	0D9 [H]	0E1 [H]	0D1 [H]
F2	0C3 [H]	0DB [H]	0E3 [H]	0D3 [H]
Z3	0C5 [H]	0DD [H]	0E5 [H]	0D5 [H]
Z4	0C6 [H]	0DE [H]	0E6 [H]	0D6 [H]
Z5	0C7 [H]	0DF [H]	0E7 [H]	0D7 [H]

Rx POH Alarm Processing

At present, the only Path level alarm that is defined is Path RDI. The mechanism that is implemented is the new Three Bit RDI-P format. This format is compatible with previous equipment (One Bit RDI-P - old Path Yellow) and the new Four State RDI-P. The Three Bit RDI-P format uses bits 5, 6 and 7 of the G1 Byte. The coding is shown in Table 10. Four Status Bits are used to report Path RDI. These are:

RRDI-P (SR1; 0F2/3/5[H], Bit 4)
RRDI-PSD (SR6; 0EA/B/D[H], Bit 7)
RRDI-PCD (SR6; 0EA/B/D[H], Bit 6)
RRDI-PPD (SR6; 0EA/B/D[H], Bit 5)

The first represents codes that are received only from old equipment. The latter three are used to identify new equipment. PRDISEL (CR16; 0FF[H], Bit 6) is used to select either a five or ten frame filter for Path RDI detection.

Table 10. RDI-P Format

G1 Byte, Bit			Interpretation	Alarm Bit Affected
5	6	7		
0	0	0	No Remote Defect[1]	RRDI-P
0	0	1	No Remote Defect[2]	RRDI-P(PD, SD, & CD)
0	1	0	Remote Payload Defect[2]	RRDI-PPD
0	1	1	No Remote Defect[1]	RRDI-P
1	0	0	Remote Defect[1]	RRDI-P
1	0	1	Remote Server Defect[2]	RRDI-PSD
1	1	0	Remote Connectivity Defect[2]	RRDI-PCD
1	1	1	Remote Defect[1]	RRDI-P

Notes:
1. This code is only transmitted by Old Equipment. New Equipment can therefore identify that it is interworking with old Equipment.
2. This code is only generated by New Equipment.

Rx B3 Processing

B3 Errors are readable by the µPro at the location Rx B3 Err Cnt (0D4[H]). Counter overflow is indicated by RB3COF (SR7; 0F6[H], Bit 7). Their accumulation is identical to B2 accumulation except that only the SPE bytes are included in the calculation. The number of received errors (including zero) is made available to the Transmit Side for use as a Path FEBE.

Additional processing is performed to develop an Excess B3 BER Alarm. The threshold is determined by the following parameters:

B3WIN	@	Location 069[H]	B3SCV	@	Location 06A[H], Bits 4-7
B3M	@	Location 068[H], Bits 0-3	B3CLR	@	Location 06C[H]
B3RATE	@	CR16; 0FF[H], Bits 0-2	B3CCV	@	Location 06A[H], Bits 0-3
B3SET	@	Location 06B[H]			

The parameter values to be used for a 10^{-3} error rate are given in Table 11. Exceeding the programmed threshold is reported as B3EBER (SR3; 0E8/9/C[H], Bit 4).

Table 11. B3EBER Parameters

BER	B3WIN	B3M	B3RATE	B3SET	B3SCV	B3CLR	B3CCV
10^{-3}	67	1	0	39	3	28	1

This is the same algorithm that is used for B2 EBER. The performance listed in Table 12 is slightly different due to the smaller frame size of 783 bytes (please see Table 7 and its associated text).

Table 12. B3 Error Alarm Performance

BER	Mean time to alarm (sec)	Probability of alarm	Mean time to clear (sec)	Probability of clear
1.2×10^{-3}	0.00667	1.00		
1.0×10^{-3}	0.00751	0.96		
9.0×10^{-4}	0.00886	0.86		
7.0×10^{-4}	0.0347	0.29		
5.0×10^{-4}	17.20	0.0009		
3.0×10^{-4}			5.76×10^{3}	1.5×10^{-5}
1.0×10^{-4}			0.00646	0.99
8.0×10^{-5}			0.00569	1.0

Rx C2 Processing

All C2 processing is based on the receipt of five consecutive C2 Bytes with the specified value. The Received C2 Byte is compared to the value written by the µPro in EXPECTC2 (0E4 [H]). Mismatch results in the alarm C2MIS (SR3; 0E8/9/C[H], Bit 2). The Received C2 Byte is also checked for the Unequipped Value - C2UNEQ (SR3; 0E8/9/C[H], Bit 1) and Payload Defect Indication - RPDI-P (SR6; 0EA/B/D[H], Bit 4).

Rx H4 Processing

The H4 Byte sent to the Terminal Bus Interface may be either the received, unaltered H4 Byte received from the Rx Line or it may be the output of a two bit H4 Counter. Selection is made by the control H4INT. When optioned for local generation (H4INT = "1"), Bits 7 and 8 of the received H4 Byte are used to synchronize a two bit, modulo four counter. If the H4 Pattern incoming to the SOT-1 from the Rx Line does not match the pattern generated by the counter, a Loss of Multiframe Alarm, RLOM (SR3; 0E8/9/C[H], Bit 0), is generated. When in the RLOM State, the phase of the previous Multiframe will be maintained until the new Multiframe phase is determined. The output of the counter is used to create the V1 Portion of C1J1V1. When optioned for H4 pass through (H4INT = "0"), the V1 portion of C1J1V1 will be suppressed, i.e., the Signal will be C1J1, the Modulo Four Counter will not be activated, and declaration of RLOM will be inhibited.

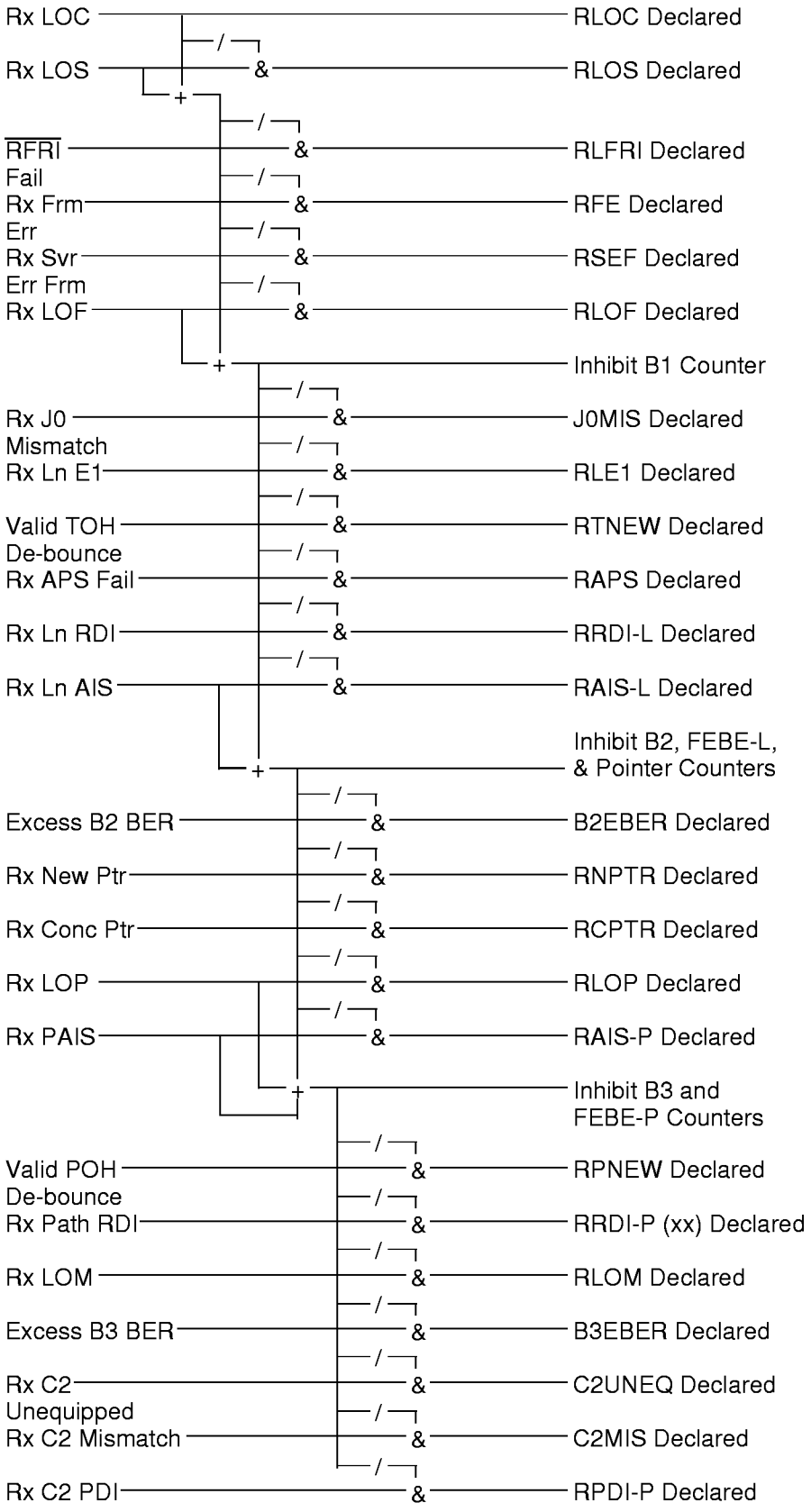
Rx Path FEBE Processing

Rx Path FEBE Processing consists of recording the number of errors received in G1 Byte Bits 1 - 4. Path FEBE Errors are accumulated in an eight or sixteen bit saturating counter designated FEBE-P Cnt (0D2[H]). Counter overflow is indicated by RPFEBEOF (SR7; 0F6[H], Bit 4).

RX SIDE ALARM HIERARCHY

A compilation of the hierarchical scheme used for Rx Side Alarm reporting is given in Equation 1 *where*: **+** represents the "OR" function, **&** represents the "AND" function, and / denotes the "NOT" function. It does not include the complete definitions for declaring or clearing each individual alarm. It is a reference that portrays the suppression effect of higher order alarms. The order of precedence is top to bottom. Also included are the conditions that inhibit the various performance counters.

Equation 1. Reporting Hierarchy for Rx Alarms



RX TERMINAL OUTPUT GENERATION

The Rx Terminal Generator and the Rx Terminal Port are responsible for assembling the information that appears at the Rx Side Terminal Output. The input to the Rx Terminal Generator is either the output from the Rx Re-timing FIFO, if Rx Re-timing is enabled, or the Rx POH Processor, if Rx Re-timing is disabled. Terminal Line AIS, Path AIS and the E1 alarm are also generated at this point.

Rx Terminal TOH Creation

The format is determined by the P.O.M. of the SOT-1. The TOH Bytes output at the Rx Terminal Port are dependent on the reference source being used by the Terminal Timing Generator (Line Timing or External Receive Timing) and by the enabling or disabling of Received Re-timing. When SPE-only mode is active no TOH bytes are output at the Rx Terminal Port.

In general, the TOH bytes output at the Rx Terminal Port may be either those received from the line or may be selected from the Terminal Insert Locations shown in Table 13.

The µPro can write all Insert Locations except A1, A2, B1 and B2. Table 14 shows the Terminal TOH Byte options. TOH Byte selection is controlled by the 13 listed Control Bits and RCLK.

When generated internally, A1 and A2 Bytes contain the values F6[H] and 28[H], respectively. Internally generated B1 and B2 Bytes contain calculated Section and Line BIP-8 values. The Calculation is Even Parity, independently performed, in parallel, over the eight bit positions of the outgoing bytes. The B1 calculation will be performed over all bytes. The B2 calculation excludes the nine Section Bytes. The value calculated for Frame n is placed in the B1 or B2 Byte of Frame n+1. Prior to output, the B1 and B2 Bytes are Exclusive-ORed, respectively, with the B1 and B2 Error Masks. These are Locations 049[H] and 051[H].

Table 13. Terminal Insert TOH Locations

	Byte Location	Byte Location	Byte Location
Section	(A1) 036 [H]	(A2) 037 [H]	C1 03C [H]
	(B1) 034 [H]	E1 038 [H]	F1 03D [H]
	D1 025 [H]	D2 026 [H]	D3 027 [H]
Line	H1 031 [H]	H2 032 [H]	H3 033 [H]
	(B2) 035 [H]	K1 03E [H]	K2 03F [H]
	D4 028 [H]	D5 029 [H]	D6 02A [H]
	D7 02B [H]	D8 02C [H]	D9 02D [H]
	D10 02E [H]	D11 02F [H]	D12 030 [H]
	Z1 03A [H]	Z2 03B [H]	E2 039 [H]

Note: Parentheses indicate addresses not written by µPro.

Table 14. Terminal TOH Options

Byte(s)	Control Bit	Location CR#; Reg, Bit	RCLK = "1"	RCLK = "0"	
				Control=0	Control=1
A1, A2	RRFRM	CR1; 0F9[H], 1	Insert[1,2]	Line	Insert[2]
C1	RRC1	CR1; 0F9[H], 6	Insert[1]	Line	Insert
B1	RRB1	CR1; 0F9[H], 0	Insert[1,3]	Line[4]	Insert[3]
E1	RRE1	CR0; 0F8[H], 5	Insert[1]	Line	Insert
F1	RRF1	CR1; 0F9[H], 7	Insert[1]	Line	Insert
D1-D3	RRSD	CR0; 0F8[H], 7	Insert1	Line	Insert
H1-H3	RRPTR	CR0; 0F8[H], 1	Line[5,6] / Insert[7]		
B2	RRB2	CR1; 1F9[H], 0	Insert[1,3]	Line[8]	Insert[3]
K1, K2	RRAPS	CR0; 0F8[H], 2	Insert[1]	Line	Insert
D4-D12	RRLD	CR0; 0F8[H], 6	Insert[1]	Line	Insert
Z1	RRZ1	CR1; 0F9[H], 5	Insert[1]	Line	Insert
Z2	RRZ2	CR1; 0F9[H], 4	Insert[1]	Line	Insert
E2	RRE2	CR0; 0F8[H], 4	Insert[1]	Line	Insert

Notes:

1. Control Bit Disabled - insert values used if RCLK = "1".
2. Generated A1 and A2 written to Insert Locations.
3. Calculated B1 and B2 written to Insert Locations.
4. Insert Value used if STS1 = "1".
5. H1 and H2 = value calculated by Rx Re-timing if Re-timing enabled.
6. Insert Value used for H3 Byte if Control Bit is disabled and re-timing is enabled.
7. This is for test purposes only - payload does not track pointer value.
8. Insert Value used if Re-timing enabled.

Rx Terminal POH Creation

The Received J1 Bytes are always passed through to the Rx Terminal Port. The H4 Byte may be either the unaltered H4 Byte from the Rx Line or the internally generated output of the two bit H4 Counter. H4INT (CR6; 0FE[H], Bit 5) controls the selection. When set to "0", the Received H4 Byte is selected. A value of "1" selects the counter output.

The remaining POH Bytes may be selected from the Rx Line or the Insert Locations given in Table 15. All locations except 0C8[H] are written by the µPro. The B3 Location is the calculated BIP-8. The Calculation is Even Parity, independently performed, in parallel, over the eight bit positions of the outgoing SPE Bytes. The value calculated for Frame n is placed in the B3 Byte of Frame n+1. Prior to output, the B3 value is Exclusive-ORed with the B3 Error Mask. This is Location 0D0 [H].

Selection is controlled by RPATH (CR0; 0F8[H], Bit 3). A Setting of "0" selects the Bytes from the Rx Line. When set to "1", the Insert POH Bytes will appear at the Rx Terminal Port.

Table 15. Terminal Insert POH Locations

Byte	Location
(B3)	0C8 [H]
C2	0C9 [H]
G1	0CA [H]
F2	0CB [H]
Z3	0CD [H]
Z4	0CE [H]
Z5	0CF [H]

Note: Parentheses indicate address not written by µPro.

Rx Terminal Alarm Generation

Line AIS insertion consists of forcing all Line Overhead Bytes (H1, H2, ..., Z2, E2) and all SPE Bytes to "1". AIS-L insertion is directly controlled by the µPro via the command SRLAIS (CR4; 0FC[H], Bit 7). In addition AIS-L may, as an option, be automatically inserted upon certain Receive Side anomalies. Enabling of automatic insertion is controlled by RRAIS (CR1; 0F9[H], Bit 3) and LTE (CR1; 0F9[H], Bit 2). The Inclusion of B2EBER is enabled by B2XAIS (CR4; 0FC[H], Bit 6) and the Inclusion of J0MIS is enabled by J0MLAIS (CR18; 1DC[H], Bit 5). When re-timing is employed, the insertion of AIS-L will terminate with the sending of a valid pointer with the NDF Bits active ("1001") for one frame. Subsequent pointer values are transmitted with an inactive NDF ("0110") indication. If re-timing is disabled, termination will consist of removing the "1" forcing function. If the conditions are such that a Line AIS will be inserted (if enabled by RRAIS) it will be indicated by RLAISC (SR8; 1F6[H], Bit 2).

Path AIS insertion consists of setting the H1, H2 and H3 Bytes and all SPE Bytes to "1". AIS-P insertion is directly controlled by the µPro via the command SRPAIS (CR4; 0FC[H], Bit 5). PAIS insertion will also occur on Receive FIFO underflow or overflow, if the automatic FIFO recovery option is set. In addition, AIS-P may, as an option, be automatically inserted upon certain received alarms. Five of the conditions for autonomous insertion are options. They are B3EBER, RLOM, C2MIS, C2UNEQ and RLE1. They are enabled, respectively, by the controls: B3XPAIS, RLOMPAIS, C2MPAIS, C2UPAIS and RLEAIS (CR4; 0FC[H], Bits 4, 3, 2, 1 and 0). Enabling of automatic insertion is controlled by RRAIS, LTE and PTE (CR9; 1F9[H], Bit 2). If re-timing is enabled the insertion of AIS-P will terminate with the sending of a valid pointer with the NDF Bits active

("1001") for one frame. Subsequent pointer values are transmitted with an inactive NDF ("0110") indication. When re-timing is disabled, termination of will consist of removing the "1" forcing function. When the conditions are such that a Path AIS will be inserted (if enabled by RRAIS) it will be indicated by RPAISC (SR8; 1F6[H], Bit 3).

The E1 Byte sent to the Rx Terminal Port may optionally be used to communicate an in band AIS Indication. This is controlled by command RA2E (CR11; 1FB[H], Bit 2). When Enabled:

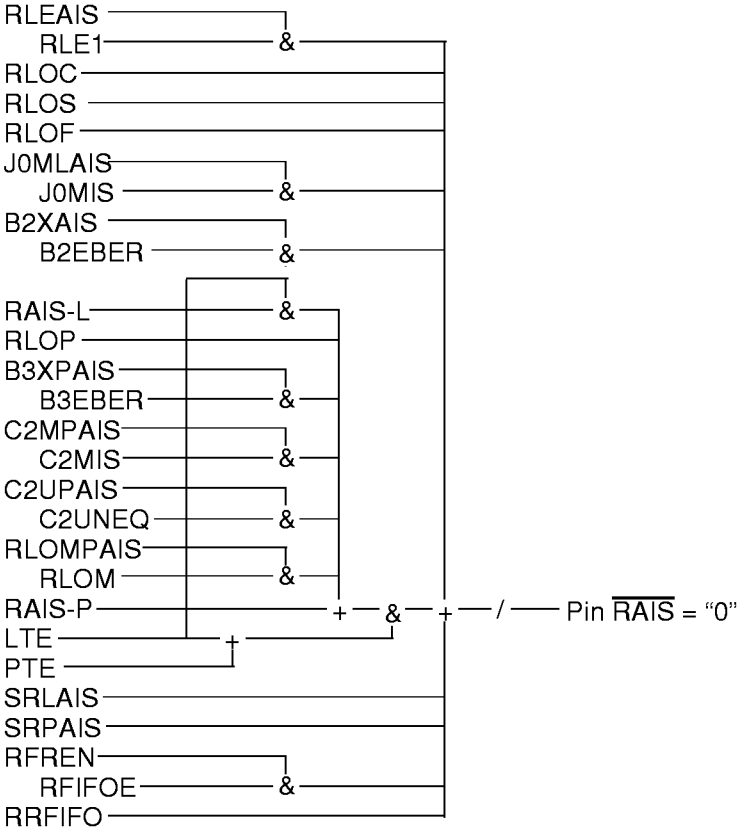
1. The Setting of RRE1 (in Line Timed Mode) will be disregarded.
2. The normal state of the E1 Byte will be all "0".
3. The occurrence of certain anomalies will result in the E1 Byte being set to all "1".

If the conditions are such that the E1 Alarm will be inserted (if enabled by RA2E) it will be indicated by the setting of RPAISC or RLAISC.

RX TERMINAL OUTPUTS

The Receive Side Signal Outputs from the Rx Terminal Port are RTCO (Serial Clock), RTDO (Serial Data), TPCO (Parallel Clock), TPDO0-TPDO7 (Parallel Data), RSPE (Payload Indication) and RSYN (Sync Pulse). The Alarm Port pin $\overline{\text{RAIS}}$ (Rx AIS) provides an external indication of Receive Side anomalies that will cause an AIS to be generated. Equation 2 provides the activation conditions *where*: **+** represents the "OR" function, **&** represents the "AND" function, and / denotes the "NOT" function.

Equation 2. Pin $\overline{\text{RAIS}}$ Activation Conditions



TX TERMINAL INPUTS

The Inputs to the Tx Terminal Port are TTDI (Serial Data) and TPDI0-TPDI7 (Parallel Data), TTCI (Serial Clock), TPCI (Parallel Clock), TSPEI (Payload Indication) and TSYNI (Sync Pulse). Failures at the Tx Terminal Port are indicated by TLOC (SR2; 1F0/1/4[H], Bit 7) and TLOS (SR2; 1F0/1/4[H], Bit 0). The Alarm Port input pin $\overline{\text{TAIS}}$ can be used to force an AIS condition at the Tx Line output. Pin $\overline{\text{TAIS}}$ at the Low level results in the setting of TAISV (SR4; 1F2/3/5[H], Bit 3).

TX TERMINAL OVERHEAD PROCESSING

The Tx Terminal Port and Tx TOH Processing Blocks are responsible for Signal Failure Detection, Frame Delineation, Overhead Distribution and Overhead Processing.

Input Frame Delineation

In all SONET Modes there are two methodologies for determining the start of the Frame and the SPE: Framing Mode and C1J1 Mode. The selection is determined by C1J1EN. The setting of C1J1EN is disregarded in SPE-only Mode.

Framing Mode

In this mode of operation (C1J1EN = "0") TSYNI and TSPEI are disregarded. The A1/A2 and H1/H2 Bytes incoming to the Tx Terminal Port are used to determine Frame and SPE alignment. In Parallel modes the F6[H], 28[H] Framing Pattern (A1 and A2) must occur on byte boundaries. The Framing Circuitry detects Framing Errors - TFE (SR5; 1E8/9/C[H], Bit 6), Severely Errored Frame - TSEF (SR2; 1F0/1/4[H], Bit 1) and Loss of Frame - TLOF (SR2; 1F0/1/4[H], Bit 2).

Line AIS detection is optionally performed using the K2 Byte. This function is enabled by DISTLAIS (CR12; 1FC[H], Bit 5) and the alarm is reported as TAIS-L (SR2; 1F0/1/4[H], Bit 4).

Pointer Processing results in the generation of the following alarms: Loss of Pointer - TLOP (SR2; 1F0/1/4[H], Bit 3), New Pointer - TNPTR (SR2; 1F0/1/4[H], Bit 6), Concatenated Pointer - TCPTR (SR5; 1E8/9/C[H], Bit 5), Path AIS - TAIS-P (SR2; 1F0/1/4[H], Bit 5). TCPTR is not a true alarm. Detection of a Concatenation Indication will always result in the declaration of TLOP. TCPTR serves as an indication of an illegal condition that has caused the TLOP Alarm. Pointer Increments and Decrements are accumulated in four bit counters which are accessed at the RAM Location designated Tx Inc/Dec Count (145[H]). Bits 0 through 3 indicate the Decrement Count. Bits 4 through 7 are for Increments. Overflow of either counter is indicated by TPMOVOF (SR8; 1F6[H], Bit 4).

C1J1 Mode

Under this condition (C1J1EN = "1") the TSYNI and TSPEI signals are enabled. The information content of the A1, A2, H1 and H2 Bytes is disregarded. Framing and Pointer Tracking are not performed and the associated alarms are inhibited. If bits 6, 7 and 8 of the K2 Byte are indeterminate then DISTLAIS must be set to "1" to inhibit the TAIS-L Alarm.

In SONET modes, TSYNI is an input and contains C1, J1, and optional V1 Information. The relationships of TSPEI and TSYNI to the input data and clock are shown in Figures 37 (page 105) and 39 (page 106). The V1 portion of TSYNI is enabled when the control H4INT = "1". Under these conditions the V1 pulse is used to synchronize a two bit, modulo four counter which creates the information for the H4 Byte that is sent to the Tx Line.

Input TOH Storage

On a per frame basis all Overhead Bytes are written into RAM Segment 105[H] - 11F[H] for µPro access. The Memory Locations for the TOH Bytes are given in Table 16. In SPE-only mode, these bytes will be "Don't Care".

Table 16. Terminal TOH Locations

	Byte	Location	Byte	Location	Byte	Location
Section	A1	116 [H]	A2	117 [H]	C1	11C [H]
	B1	114 [H]	E1	118 [H]	F1	11D [H]
	D1	105 [H]	D2	106 [H]	D3	107 [H]
Line	H1	111 [H]	H2	112 [H]	H3	113 [H]
	B2	115 [H]	K1	11E [H]	K2	11F [H]
	D4	108 [H]	D5	109 [H]	D6	10A [H]
	D7	10B [H]	D8	10C [H]	D9	10D [H]
	D10	10E [H]	D11	10F [H]	D12	110 [H]
	Z1	11A [H]	Z2	11B [H]	E2	119 [H]

Input B1 Processing

When enabled by INHTB1C (CR15; 1DF[H], Bit 3), the B1 Byte is compared to a calculated B1 value. The calculation is Even Parity, independently performed, in parallel, over the eight bit positions of all incoming bytes. The errors (up to eight per frame) are accumulated in an eight bit rollover counter designated Tx B1 Err Cnt (146[H]) which is readable by the µPro. There is no counter overflow indication bit.

Input B2 Processing

B2 Errors are accumulated in the same manner as with the B1 Byte, except that the nine SOH Bytes are excluded, the function is enabled by INHTB2C (CR15; 1DF[H], Bit 2), and the rollover counter is designated Tx B2 Err Cnt (147[H]). There is no counter overflow indication bit.

Input E1 Processing

A Transmit Terminal E1 Alarm - TTE1 (SR5; 1E8/9/C[H], Bit 4) is extracted from the E1 Byte, when so optioned by TE2A (CR11; 1FB[H], Bit 1). TTE1 detection assumes that some terminal side entity has detected an AIS condition and uses the E1 Byte for in band communication of the condition. TTE1 can be used for autonomous generation of AIS at the Tx Line Port.

Input POH Storage

On a per frame basis, the B3 through Z5 bytes incoming at the Tx Terminal Port are stored in the RAM Segment 1CO[H] - 1C7[H]. If the Control TPATH (CR8; 1F8[H], Bit 3) = "0", the J1 Bytes will be stored in memory locations that are accessible at the RAM Segment 180[H] - 1BF[H]. This address space is shared with the Tx J0 Bytes. J1 Access is enabled when J0RWEN = "0". The Memory Locations for the POH Bytes are given in Table 17. When enabled, J1 Byte storage is controlled by J1SYNCEN. J1SYNCEN = "0" results in the J1 Bytes being stored in the 64 Byte Segment, in rotating fashion, with no specific starting point. When J1SYNCEN is set to "1" reception of ASCII characters CR and LF, in sequence, will cause the next J1 Byte to be written at address 180 [H] with subsequent J1 bytes being written in succeeding locations.

Table 17. Terminal POH Locations

Byte	Location
J1*	180 [H] - 1BF [H]
B3	1C0 [H]
C2	1C1 [H]
G1	1C2 [H]
F2	1C3 [H]
H4	1C4 [H]
Z3	1C5 [H]
Z4	1C6 [H]
Z5	1C7 [H]

* J0 when J0RWEN = “1”

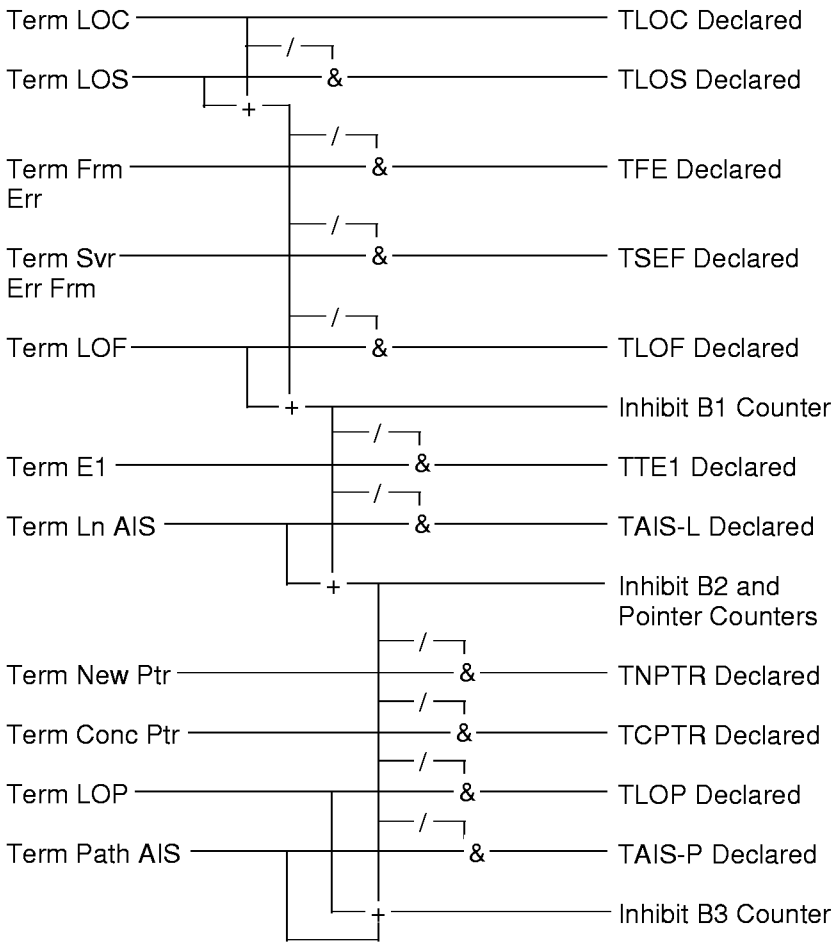
Input B3 Processing

Input B3 processing is performed if TPATH = "0". B3 Processing is identical to B2 Processing except that only the SPE bytes are included in the calculation. The errors are accumulated with the rollover counter designated Tx B3 Err Cnt (1DF[H]). There is no counter overflow indication bit.

TX SIDE ALARM HIERARCHY

A compilation of the hierarchical scheme used for Transmit Side alarm reporting is given in Equation 3 *where*: **+** represents the "OR" function, **&** represents the "AND" function, and / denotes the "NOT" function. It does not include the complete definitions for declaring or clearing each individual alarm. It is a reference that portrays the suppression effect of higher order alarms. The order of precedence is top to bottom. Also included are the conditions that inhibit the various performance counters.

Equation 3. Reporting Hierarchy for Tx Alarms



TRANSMIT POH ASSEMBLY

The Tx POH Generator is responsible for assembling the POH that will be output on the Tx Line. The Payload portion of the SPE is input from the Tx Terminal Processor. In general, the POH Bytes have two possible sources:

1. The POH Bytes input at the Tx Terminal Port
2. Information written by the µPro.

TPATH = "0" selects Option 1. When set to "1", Option 2 is enabled and makes use of the Tx Insert POH Byte locations shown in Table 18.

Table 18. Tx Insert POH Locations

Byte	Location
J1[1]	180 [H] - 1BF [H]
(B3)[2,3]	1C8 [H]
C2	1C9 [H]
G1	1CA [H]
F2	1CB [H]
H4	1CC [H]
Z3	1CD [H]
Z4	1CE [H]
Z5	1CF [H]

Notes:
1. Used for Insert if TPATH = "1".
2. Calculated Value.
3. Parentheses indicate address not written by µPro.

The 64 Byte J1 Segment is common to Tx Terminal Input storage and Tx Line Insert storage. When TPATH = "1", the µPro will write these locations. When the J1 Locations are being filled from the Tx Terminal Port (TPATH = "0"), J1SYNCEN controls whether the storage is rotating or synchronized as explained above in the "Input POH Storage" section. The B3 location contains an internally generated value. The calculation is Even Parity, independently performed, in parallel, over the eight bit positions of the SPE Bytes to be transmitted. The value calculated for Frame n is placed in the B3 Byte of Frame n+1. All other locations are written by the µPro. Table 19 presents the available options for Transmit POH.

Table 19. Tx Line POH Options

Byte(s)	TPATH = "0"	TPATH = "1"
J1[1]	Tx Term. J1 Byte	Insert J1 Bytes
B3[1]	Tx Term. B3 Byte[2]	Calculated Value
C2[1]	Tx Term. C2 Byte	Insert C2 Byte
G1[1]	Tx Term. G1 Byte	Insert G1 Byte
F2[1]	Tx Term. F2 Byte	Insert F2 Byte
H4[1,4]	Tx Term. H4 Byte	Insert H4 Byte[3]
Z3[1]	Tx Term. Z3 Byte	Insert Z3 Byte
Z4[1]	Tx Term. Z4 Byte	Insert Z4 Byte
Z5[1]	Tx Term. Z5 Byte	Insert Z5 Byte

Notes:

1. Selection options are affected by the generation of Path Idle. See "Tx Idle Insertion" (page 130).
2. Only if H4INT, TPFEBEEN, TPRDIEN, TPRDIPD, TPRDICD and TPRDISD = "0". If H4INT, TPFEBEEN, TPRDIEN, TPRDIPD, TPRDICD or TPRDISD = "1" then Calculated Value will be used.
3. Only if TXH4INS = "1". If TXH4INS = "0", the Tx Term H4 Byte will be used.
4. In SPE-only Mode or SONET Mode with C1J1EN = "1" and if H4INT = "1", and RTLOOP = "0": then the two LSBs will be overwritten by the Internal H4 Counter value.

The selected B3 Byte will be Exclusive-ORed with the Tx B3 Err Mask (1D0[H]). TRERR (CR11; 1FB[H], Bit 6) is used to enable an automatic reset to all "0" of the B3 Mask. When set to "1", the B3 Error Mask will be reset after one frame. A value of "0" disables the automatic reset feature. If the B3 Byte is not internally calculated then multiple frames will be transmitted with errors since the Errored B3 Byte that is transmitted will not be included in the B3 calculation for the succeeding frame.

Tx Path FEBE Insertion

The Path FEBE (FEBE-P) function is enabled by TPFEBEEN. When activated, Bits 1 through 4 of the G1 Byte selected above are overwritten with a value of "0000" - "1000". The number of received B3 Errors is the source for the FEBE-P Value. Since the received and transmitted SPE Rates may differ, an accumulation mechanism is employed to ensure that the FEBE-P Count returned will equal the B3 Errors received.

Tx Path RDI Insertion

Path RDI transmission (RDI-Pxx *where*: xx = SD, PD or CD) is accomplished using the coding described in Table 10 (page 116). Transmission of RDI-Pxx consists of overwriting bits 5-7 of the G1 Byte selected above with the appropriate code. There are ten controls associated with Path RDI insertion. Automatic RDI-Pxx insertion is enabled by TPRDIEN. B3PRDISD, B3PRDICD and TOHPRDISD (CR19; 1DB[H], Bits 2, 1 and 0) enable the B3 Excessive Bit Error Rate and TOH Faults in the appropriate RDI-Pxx equations. C2MPRDI and C2UPRDI (CR7; 1DE[H], Bits 3 and 2) enable Signal Label Mismatch and Signal Label Unequipped in the appropriate RDI-Pxx equations. The duration for sending RDI-Pxx is controlled by TPRDI20 (CR17; 1DD[H], Bit 0). If it is at the "0", Logic Level RDI-Pxx will be sent for the duration of the causative event. When it is set to "1", RDI-Pxx will be sent for a minimum of 20 Frames. TPRDISD, TPRDICD and TPRDIPD (CR19; 1DB[H], Bits 5, 4 and 3) are used to force the insertion of RDI-Pxx.

Tx Idle Insertion

The Insertion of a Path Idle Signal is performed at the command of the µPro via the control TIDL (CR7; 1DE[H], Bit 7). The Path Idle Signal that is inserted may be one of two forms:

1. All bytes of the SPE (including the POH Bytes) are set to zero.
2. All bytes of the SPE except the POH Bytes are set to zero.

The form of the idle signal is selected by the control IDLSEL (CR7; 1DE[H], Bit 6). The first form is selected when IDLSEL = "0". The second type of Path Idle is selected when IDLSEL = "1". When TIDL = "0", POH byte selection is as described above. When TIDL = "1" and IDLSEL = "0", all POH selection controls are disregarded. When TIDL and IDLSEL both are set to "1", TPATH is disregarded and all POH bytes are taken from the Insert Locations.

TRANSMIT TOH ASSEMBLY

The Tx OH Generator is responsible for creating the signal that will be output on the Tx Line. The Tx Line Outputs consist of serial data - TLDO, and serial clock - TLCO. The functions performed include TOH Selection, Alarm Insertion, BIP-8 Calculation and Scrambling. The assembled SPE is taken from either the Tx Re-timing FIFO or the Tx POH Generator (Tx Re-timing disabled). In SONET Mode, the TOH Bytes sent to the Tx Line have four possible sources:

1. The TOH Bytes input at the Tx Terminal Port
2. Information written by the µPro.
3. The TOH Bytes input at the Order Wire/APS Port, Section DCC Port and Line DCC Port
4. The TOH Bytes input at the Tx TOH Port in All TOH Mode

Individual controls are used to select, on a per byte (or functional byte group) basis, between the various options. If SPE-only Mode is selected or TCLK = "1", then the settings which would enable Option 1 are disregarded and only options 2 through 4 are available.

Table 20 lists the Tx Insert TOH locations. These locations contain the TOH Bytes that will appear in the signal sent to the Tx Line when Option 1 is not selected. The B1 and B2 locations contain internally generated values. All other locations contain values written by the µPro or external values from the Tx TOH Port. In the OW/APS Mode, only the E1, E2, K1 and K2 Bytes may be externally created. In All TOH Mode, all TOH Bytes except B1, B2, H1, H2 and H3 may be externally generated.

Table 20. Tx Insert TOH Locations

	Byte	Location	Byte	Location	Byte	Location
Section	A1	136 [H]	A2	137 [H]	C1	13C [H]
	(B1)	134 [H]	E1	138 [H]	F1	13D [H]
	D1	125 [H]	D2	126 [H]	D3	127 [H]
Line					H3	133 [H]
	(B2)	135 [H]	K1	13E [H]	K2	13F [H]
	D4	128 [H]	D5	129 [H]	D6	12A [H]
	D7	12B [H]	D8	12C [H]	D9	12D [H]
	D10	12E [H]	D11	12F [H]	D12	130 [H]
	Z1	13A [H]	Z2	13B [H]	E2	139 [H]

Note: Parentheses indicate address not written by µPro.

Tx A1 and A2 Selection

The A1 and A2 Bytes sent to the Tx Line are always taken from the Insert A1 and A2 Locations. TRFRM (CR11; 1FB[H], Bit 7) and TFRMEXT (CR14; 1FE[H], Bit 7) determine the Insert Location content. The source selection is shown below *where*: **&** = the logical "AND", **+** = the logical "OR" function, and **=** represents a control state.

Generate	µPro[1]	External
TRFRM = "1"	TRFRM = "0" & TFRMEXT = "0" + TRFRM = "0" & TFRMEXT = "1" & OA = "1"	TRFRM = "0" & TFRMEXT = "1" & OA = "0"

Note 1: If the µPro writes values other than F6[H] and 28[H] for A1 and A2, respectively, then they must be changed to the correct values within 500 µs to prevent an upstream SEF Alarm or 3 ms to prevent an upstream LOF Alarm.

Tx C1/J0 Selection

Controls J0EN0, J0EN1, TXC1EXT (CR14; 1FE[H], Bit 6), TRC1(CR9; 1F9[H], Bit 6) and OA are used to control the C1 Selection. J0ENx selects the Insert Location as shown in Table 21. If J0EN1 = "1", the Insert locations consist of a 64 Byte RAM segment. Microprocessor access to these locations is by means of Locations 180 [H] - 1BF [H], and is controlled by J0RWEN. When the Multiple Byte J0 messages are input via the TOH Port, the storage method is controlled by J0ENx. When J0EN(1,0) = "10", the bytes are stored in rotating fashion with no specific starting point. If J0EN(1,0) = "11", the reception of ASCII characters CR and LF, in sequence, will synchronize the J0 Counter so that the next J0 Byte will be written at the location that is accessed at address 180 [H].

Table 21. Tx C1/J0 Options

J0EN1	J0EN0	TRANSMIT FUNCTION
0	-	Single Byte C1/J0 - 13C[H]
1	0	16/64 byte RAM segment used for J0 - accessed at 180[H]-1BF[H]. If external, storage is not aligned.
1	1	16/64 byte RAM segment used for J0 - accessed at 180[H]-1BF[H]. If external, storage is aligned.

The source selection is shown below *where*: **&** = the logical "AND", **+** = the logical "OR" function, and **=** represents a control state.

Tx Terminal Port	Insert Location	
	µPro	External
SPE-only Mode not selected **&** TRC1 **=** "0"	SPE-only Mode selected **&** TXC1EXT **=** "0" + SPE-only Mode selected **&** OA **=** "1" + TRC1 **=** "1" **&** TXC1EXT **=** "0" + TRC1 **=** "1" **&** OA **=** "1"	SPE-only Mode selected **&** TXC1EXT **=** "1" **&** OA **=** "0" + TRC1 **=** "1" **&** TXC1EXT **=** "1" **&** OA **=** "0"

Tx B1 Selection

The B1 Byte sent to the Tx Line is dependent on the setting of STS1 and TRERR.

When STS1 = "0", the outgoing B1 Byte will contain the contents of the Tx B1 Err Mask (149 [H]). The control TRERR is used to enable an automatic reset to all "0" of the B1 Mask. When set to "1", the B1 Error Mask will be reset after one frame. A value of "0" will disable the automatic reset feature.

In configurations where STS1 = "1", the B1 Byte is calculated and placed in the Insert B1 Location. The calculation is Even Parity, independently performed, in parallel, over the eight bit positions of all bytes to be transmitted, after scrambling is performed. The value calculated for Frame n will be placed in the B1 Byte of Frame n+1 before scrambling is performed. The calculated value in the B1 Insert Location will be Exclusive-ORed with the Tx B1 Err Mask prior to insertion in the transmit B1 Byte position. TRERR controls the resetting of the mask as explained above.

Tx E1 Selection

E1 Byte selection is controlled by TRE1 (CR8; 1F8[H], Bit 5) and TXE1EXT (CR14; 1FE[H], Bit 5). The source selection is shown below *where*: **&** = the logical "AND", **+** = the logical "OR" function, and **=** represents a control state.

Tx Terminal Port	Insert Location	
	μPro	External
SPE-only Mode not selected & TRE1 = "0"	SPE-only Mode selected & TXE1EXT = "0" + TRE1 = "1" & TXE1EXT = "0"	SPE-only Mode selected & TXE1EXT = "1" + TRE1 = "1" & TXE1EXT = "1"

These selections are not available if the E1 Byte is used for in-band alarm communication. See the section "Tx E1 Alarm Insertion," (page 137).

Tx F1 Selection

Controls TXF1EXT (CR14; 1FE[H], Bit 4), TRF1(CR9; 1F9[H], Bit 7), and OA are used for F1 Selection. The source selection is shown below *where*: **&** = the logical "AND", **+** = the logical "OR" function, and **=** represents a control state.

Tx Terminal Port	Insert Location	
	μPro	External
SPE-only Mode not selected & TRF1 = "0"	SPE-only Mode selected & TXF1EXT = "0" + SPE-only Mode selected & OA = "1" + TRF1 = "1" & TXF1EXT = "0" + TRF1 = "1" & OA = "1"	SPE-only Mode selected & TXF1EXT = "1" & OA = "0" + TRF1 = "1" & TXF1EXT = "1" & OA = "0"

Tx D1-D3 Selection

D1-D3 Byte selection is controlled by TRSD (CR8; 1F8[H], Bit 7) and TXSDEXT (CR14; 1FE[H], Bit 3). The source selection is shown below *where*: **&** = the logical "AND", **+** = the logical "OR" function, and **=** represents a control state.

Tx Terminal Port	Insert Location	
	μPro	External
SPE-only Mode not selected **&** TRSD **=** "0"	SPE-only Mode selected **&** TXSDEXT **=** "0" + TRSD **=** "1" **&** TXSDEXT **=** "0"	SPE-only Mode selected **&** TXSDEXT **=** "1" + TRSD **=** "1" **&** TXSDEXT **=** "1"

In the OW/APS Application, the external source for the Bytes will be the Tx Section DCC Port. In the All TOH Application, the external source will be either the Tx Section DCC Port or the Tx TOH Port, as controlled by OA and SDCCEN (CR17; 1DD[H], Bit 7).

Tx H1-H3 Selection

The sources for the H1 and H2 Bytes may be either the Tx Terminal Port or the calculated values. The H3 Byte sources are either the Tx Terminal Port or the Insert Location. If transmit re-timing is disabled, the Tx Terminal Locations are used for H1, H2 and H3. When transmit re-timing is enabled, the calculated H1 and H2 values, and the H3 Insert Location value are used. The H3 value taken from the Insert Location will be overwritten by SPE data when a Pointer Decrement is performed. The source selection is shown below *where*: **&** = the logical "AND", **+** = the logical "OR" function, and **=** represents a control state.

Tx Terminal Port	Insert Location - Internal
SPE-only Mode not selected **&** C1J1EN **=** "0" **&** TXRTM **=** "0" **&** TCLK **=** "0"	SPE-only Mode selected + C1J1EN **=** "1" + TXRTM **=** "1" + TCLK **=** "1"

Tx B2 Selection

The B2 Byte is calculated and placed in the Insert B2 Location when DISTB2R (CR17; 1DD[H], Bit 1) = "0". The calculation is Even Parity, independently performed, in parallel, over the eight bit positions of all bytes except the nine Section Overhead Bytes. The value calculated for Frame n is placed in the B2 Byte of Frame n+1. If DISTB2R = "1" and if TCLK = "0", the B2 Byte Incoming at the Tx Terminal Port will be output at the Tx Line Port.

The B2 value output on the Tx Line will be Exclusive-ORed with the Tx B2 Err Mask (151[H]) prior to insertion. As has been discussed previously, TRERR controls the resetting of the mask.

Tx K1 and K2 Selection

K1 and K2 Byte Selection is controlled by TRAPS and EXAPS (CR8; 1F8[H], Bits 2 and 1). The source selection is shown below *where*: **&** = the logical "AND", **+** = the logical "OR" function, and **=** represents a control state.

Tx Terminal Port	Insert Location	
	µPro	**External**
SPE-only Mode not selected **&** TRAPS **=** "0"	SPE-only Mode selected **&** EXAPS **=** "0" + TRAPS **=** "1" **&** EXAPS **=** "0"	SPE-only Mode selected **&** EXAPS **=** "1" + TRAPS **=** "1" **&** EXAPS **=** "1"

Tx D4-D12 Selection

D4-D12 Byte selection is controlled by TRLD (CR8; 1F8[H], Bit 6) and TXLDEXT (CR15; 1DF[H], Bit 7). The source selection is shown below *where*: **&** = the logical "AND", **+** = the logical "OR" function, and **=** represents a control state.

Tx Terminal Port	Insert Location	
	µPro	**External**
SPE-only Mode not selected **&** TRLD **=** "0"	SPE-only Mode selected **&** TXLDEXT **=** "0" + TRLD **=** "1" **&** TXLDEXT **=** "0"	SPE-only Mode selected **&** TXLDEXT **=** "1" + TRLD **=** "1" **&** TXLDEXT **=** "1"

In the OW/APS Application, the external source for the Bytes will be the Tx Line DCC Port. In the All TOH Application, the external source will be either the Tx Line DCC Port or the Tx TOH Port, as controlled by OA and LDCCEN (CR17; 1DD[H], Bit 6).

Tx Z1 Selection

The controls TXZ1EXT (CR14; 1FE[H], Bit 2), TRZ1 (CR9; 1F9[H], Bit 5) and OA are used to control the Z1 Selection. The source selection is shown below *where*: **&** = the logical "AND", **+** = the logical "OR" function, and **=** represents a control state.

Tx Terminal Port	Insert Location	
	µPro	**External**
SPE-only Mode not selected **&** TRZ1 **=** "0"	SPE-only Mode selected **&** TXZ1EXT **=** "0" + SPE-only Mode selected **&** OA **=** "1" + TRZ1 **=** "1" **&** TXZ1EXT **=** "0" + TRZ1 **=** "1" **&** OA **=** "1"	SPE-only Mode selected **&** TXZ1EXT **=** "1" **&** OA **=** "0" + TRZ1 **=** "1" **&** TXZ1EXT **=** "1" **&** OA **=** "0"

Tx Z2 Selection

TXZ2EXT (CR14; 1FE[H], Bit 1), TRZ2 (CR9; 1F9[H], Bit 4) and OA are used to control the Selection of Z2. The source selection is shown below *where*: **&** = the logical "AND", **+** = the logical "OR" function, and **=** represents a control state.

Tx Terminal Port	Insert Location	
	µPro	**External**
SPE-only Mode not selected **&** TRZ2 **=** "0"	SPE-only Mode selected **&** TXZ2EXT **=** "0" + SPE-only Mode selected **&** OA **=** "1" + TRZ2 **=** "1" **&** TXZ2EXT **=** "0" + TRZ2 **=** "1" **&** OA **=** "1"	SPE-only Mode selected **&** TXZ2EXT **=** "1" **&** OA **=** "0" + TRZ2 **=** "1" **&** TXZ2EXT **=** "1" **&** OA **=** "0"

Tx E2 Selection

E2 Byte selection is controlled by TRE2 (CR8; 1F8[H], Bit 4) and TXE2EXT (CR14; 1FE[H], Bit 0). The source selection is shown below *where*: **&** = the logical "AND", **+** = the logical "OR" function, and **=** represents a control state.

Tx Terminal Port	Insert Location	
	µPro	**External**
SPE-only Mode not selected **&** TRE2 **=** "0"	SPE-only Mode selected **&** TXE2EXT **=** "0" + TRE2 **=** "1" **&** TXE2EXT **=** "0"	SPE-only Mode selected **&** TXE2EXT **=** "1" + TRE2 **=** "1" **&** TXE2EXT **=** "1"

Tx Line FEBE Insertion

FEBE-L insertion is enabled by the control bits TLFEBEEN. When enabled, the Line FEBE value ("0000" through "1000") overwrites Bits 5 through 8 of the Z2 Byte that has been selected. The FEBE-L Value is obtained from the received B2 Errors. An accumulation mechanism is used to account for differing transmit and receive rates.

Tx E1 Alarm Insertion

The E1 Byte sent to the Tx Line may optionally be used to communicate an in band AIS Indication. This is controlled by command TA2E (CR11; 1FB[H], Bit 0). When Enabled:

1. The Settings of TRE1 and TXE1EXT will be disregarded.
2. The normal state of the E1 Byte will be all "0".
3. The occurrence of certain anomalies will result in the E1 Byte being set to all "1".

If the conditions are such that an E1 Alarm will be inserted (if enabled by TA2E), it will be indicated by the setting of TPAISC or TLAISC (SR8; 1F6[H], Bits 1 and 0). When E1 Alarm insertion is disabled the functioning of TRE1 and TXE1EXT is enabled.

Tx Path AIS Insertion

Path AIS (AIS-P) insertion consists of setting the H1, H2 and H3 Bytes and all SPE Bytes to "1". This function is enabled if TRAIS (CR9; 1F9[H], Bit 3) = "1" and either LTE (CR1; 0F9[H], Bit 2) or PTE (CR9; 1F9[H], Bit 2) = "1". AIS-P insertion is directly controlled by the µPro via the command STPAIS (CR11; 1FB[H], Bit 5). Path AIS insertion will also occur on Transmit FIFO underflow or overflow, if the automatic FIFO recovery option is set. In addition, AIS-P may, as an option, be automatically inserted upon certain Tx Terminal Port alarms and when the Alarm Port Input is active (Pin $\overline{TAIS}$ is Low). Use of the Tx Terminal E1 Alarm is enabled by TTEAIS (CR15; 1DF[H], Bit 5). The insertion of PAIS will terminate with the sending of a valid pointer with the NDF Bits active ("1001") for one frame. Subsequent pointer values will be transmitted with an inactive NDF ("0110") indication. If the conditions are such that a PAIS will be inserted (if enabled by TRAIS), it will be indicated by the setting of TPAISC.

Tx Line RDI Insertion

RDI-L is transmitted by setting Bits 6, 7 and 8 of the K2 Byte to "110". LRDI may be inserted upon command from the µPro and, if so enabled, autonomously upon certain Receive Side anomalies. The µPro command is STLRDI (CR15; 1DF[H], Bit 1). Automatic Line RDI insertion is enabled by the control TRLRDI (CR2; 0FA[H], Bit 4). The Inclusion of B2EBER as a condition for automatic insertion is enabled by the control B2ELRDI (CR15; 1DF[H], Bit 0). The Inclusion of J0MIS as a condition for automatic insertion is enabled by the control J0MLRDI (CR18; 1DC[H], Bit 6).

Tx Line AIS Insertion

Line AIS (AIS-L) insertion consists of setting all bytes of the Line Level Signal to "1". It is enabled if TRAIS = "1" and LTE and PTE = "0". AIS-L insertion is directly controlled by the µPro via the command STLAIS (CR17; 1DD[H], Bit 5). In addition, AIS-L will be inserted if the Alarm Port input is active (Pin $\overline{TAIS}$ = "0") and TRAIS = "1". If the conditions are such that an AIS-L will be inserted (if enabled by TRAIS), it will be indicated by the setting of TLAISC. The insertion of AIS-L will terminate with the sending of a valid pointer with the NDF Bits active ("1001") for one frame. Subsequent pointer values will be transmitted with an inactive NDF ("0110") indication.

LOOPBACKS

Three Loopbacks are available: Line Loopback, Tx-Rx Line Loopback, and Rx-Tx Terminal Loopback. These are indicated in the Block Diagram (Figure 14) and as the shaded multiplexers in Figure 46, where TRLOOP, LPAISEN, LPAISSEL, LINLOOP and RTLOOP are control bits.

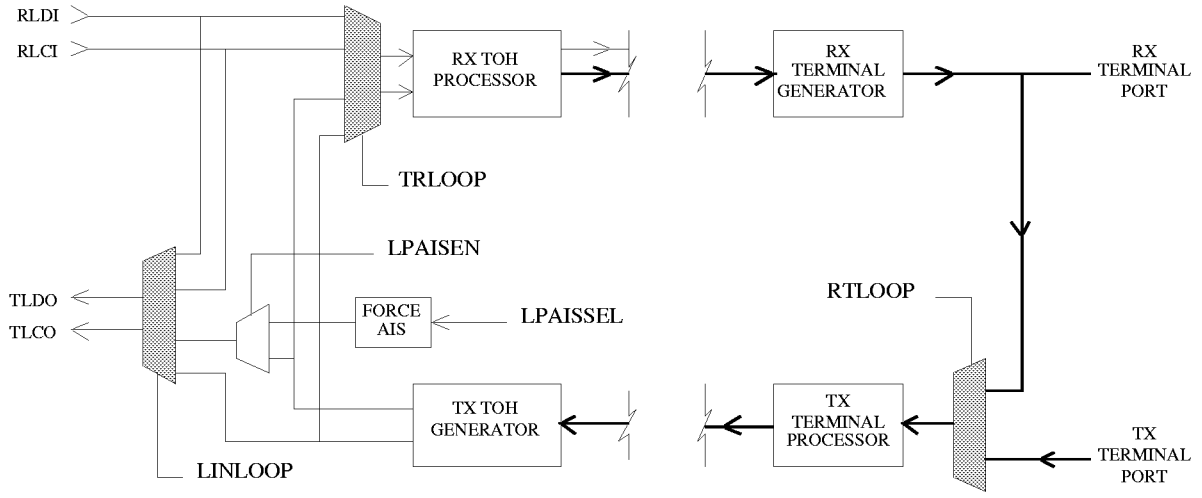


Figure 46. Loopbacks

Line Loopback

Line Loopback consists of open circuiting the Clock and Data Outputs from the Tx OH Generator and substituting the information incoming on RLCI and RLDI. This is controlled by LINLOOP (CR17; 1DD[H], Bit 2).

Tx-Rx Line Loopback

Tx-Rx Line Loopback consists of open circuiting the RLDI and RLCI Inputs and substituting the Tx OH Generator Clock and Data outputs. When Tx-Rx Line Loopback is initiated $\overline{\text{RFRI}}$ is disregarded. This Loopback is controlled by TRLOOP (CR0; 0F8[H], Bit 0).

When a Tx-Rx Line Loopback is enabled the signal exiting on TLDO may be either the information that is looped back, i.e., the information input at the Tx Terminal Port, or it may be a forced AIS signal. This is controlled by LPAISEN (CR12; 1FC[H], Bit 4). When the Forced AIS option is selected LPAISSEL (CR12; 1FC[H], Bit 3) determines if AIS-L or AIS-P is output. Termination of AIS Insertion by removing the loopback or changing the state of LPAISEN will not cause an NDF to be transmitted. AIS termination with an NDF indication can be achieved by performing the following sequence of actions:

1. forcing the Tx OH Generator to Insert the appropriate AIS
2. removing the loopback or changing LPAISEN
3. Terminating the AIS Insertion at the Tx OH Generator.

Activation of Tx-Rx Line Loopback will inhibit RLFRI from creating interrupts or downstream alarms. The RLOC and RLOS Detectors will monitor the looped signal.

Rx-Tx Terminal Loopback

Rx-Tx Terminal Loopback consists of open circuiting the path between the Tx Terminal Port and the Tx Terminal Processor and substituting the Rx Terminal Generator output for the Tx Terminal Port Input. Rx-Tx Terminal Loopback is controlled by RTLOOP (CR8; 1F8[H], Bit 0). When Rx-Tx Terminal Loopback is enabled the signal at the Rx Terminal Port is unaffected. Activation of Rx-Tx Terminal Loopback will inhibit TLOC and TLOS from creating interrupts or upstream alarms. The looped data is not processed by the Tx Terminal Framer but rather has a frame indicator sent with it to the Tx Terminal Processor from the Rx side.

RESETS

The SOT-1 has four reset mechanisms: Hardware Reset, Software Chip Reset, Software Receive Side Reset, and Software Transmit Side Reset.

Hardware Reset is accomplished with the pin RST, which is active High. This is a level sensitive input. The device remains in the reset condition until RST is returned to the Low Level. When activated, the reset process will:

1. Reset all Counters
2. Reset all Control Registers
3. Clear All Status Bits
4. Re-center the FIFOs
5. Set INT (SR1; 0F2/3/5[H], Bit 7)

A Software Chip Reset is initiated by CHPRES (CR18; 1DC[H], Bit 0). It is similar to a Hardware Reset except that step 2, listed above, is not performed. A Receive Software Reset is initiated by RSWRES (CR3; 0FB[H], Bit 1). A Transmit Software Reset is Controlled by TSWRES (CR15; 1DF[H], Bit 6). A Transmit or Receive Software Reset consists of resetting the Counters and Status Bits associated with the Transmit or Receive Sides. A Software Reset is initiated by setting the appropriate control bit to "1". The reset state will remain in effect until the control bit is returned to the "0" logic level.

MICROPROCESSOR INTERFACE

The µPro Interface is the means by which the SOT-1 is queried and controlled by the microprocessor and is a multiplexed Data/Address type.

Software Operations

All Memory Locations are Read and Write except for: 000[H] - 004[H], Clear on Read Status Registers, and Unlatched Status Registers, all of which are Read only. Some control register bits are marked as Reserved or Unused and these should all be written to "0". Failure to do so may jeopardize software compatibility in future device revisions. The Control RAMTSTEN (CR6; 0FE[H], Bit 6) is provided to allow memory testing. When set to "1", RAM access by all internal operations is inhibited. Two controls, TEST1 and TEST2 (CR17; 1DD[H], Bits 4 and 3), are used for Internal TranSwitch tests. These must be set to "0" for normal operation.

All counters clear on Read. Writing to a 16 Bit Counter is accomplished by first writing the HIBYTE Location (1FF[H]) then writing to the Lower Order Register. Reading is accomplished by reading the lower order register then reading HIBYTE. Registers 0F6[H] and 1F6[H] are non-latching registers used for Receive Side and Transmit Side counter overflows, respectively. One bit is provided for each counter, except for the Pointer Increment and Decrement Counters. The Rx Pointer Increment and Decrement Counters use the same bit to indicate overflow. Similarly, the Tx Pointer Increment and Decrement Counters are combined into a single bit. There are no overflow indication bits for the Tx B1, B2 and B3 counters.

Alarm reporting is accomplished with seven sets of three Status Registers (SR0 - SR6), which are composed of 2 latching and 1 non-latching location, and three single Status Registers (SR7 - SR9), which provide only unlatched values. In either case, the alarm is indicated by the appropriate bit being set to "1". In SR0 - SR6, each alarm occupies the same bit position in each of the three registers. The First Register of the set provides latched values that clear (reset to "0") when the register is read. The Second Register contains latched values that are cleared, on a per bit basis, by writing a "1" to the bit that is to be cleared (multiple bit positions may be simultaneously cleared). It must be noted that the clearing of either latched register is reflected in the contents of the other register. For example reading the First Register clears all alarms in both the First and Second Register. Similarly, Writing a "1" to a bit in the Second Register clears that alarm bit in both the First and Second Registers. For test purposes, writing a "1" to any bit(s) with the address of the Third register of SR0 - SR6 will set a "1" in the corresponding bit(s) in the First and Second registers. The Third register of the set and the three single register SR7 - SR9 contain unlatched values that provide a real time indication of the alarm status. Bits in these locations will be at a logical "1" for the duration of the causative event.

Interrupt Structure

In general, interrupts are created on alarms or counter overflows. Alarm related interrupts may occur on the positive edge (event start) or positive and negative edges (event start and end) of the causative incident. Counter overflow interrupts are initiated only on the detection of the overflow condition. Clearing the counter does not create an interrupt. The creation of an interrupt is reported as INT. Any time that an interrupt is created this bit will be set to "1".

To simplify interrupt handling an unlatched Polling Register (0F7) is provided. It is used to indicate the condition of six Status Registers and the two Counter Overflow Registers. Each of the eight registers is assigned a bit in this register. One or more bits set in a Status or Counter overflow register will cause the appropriate Polling Register bit to be set.

There are six controls that manage the creation of interrupts. They are:

1. HWINE (CR2; 0FA[H], Bit 5)
2. INVINT (CR5; 0FD[H], Bit 0)
3. -VE (CR2; 0FA[H], Bit 0)
4. TIEN (CR2; 0FA[H], Bit 2)
5. PIEN (CR2; 0FA[H], Bit 1)
6. DIEN (CR5; 0FD[H], Bit 7)

HWINE is the master interrupt enable. When set to "1", the interrupt output to the µPro (INT) is enabled. A value of "0" disables the creation of interrupts. INVINT is used to logically invert the pin INT. Setting this bit to "1" causes the signal to become $\overline{INT}$. -VE is the edge control for alarm generated interrupts. A value of "0" creates the interrupts on the positive edge only. When set to "1", interrupts will be created on both the positive and negative edges. -VE has no effect on the generation of interrupts by counters that overflow. TIEN, PIEN, and DIEN enable categories of events for interrupt creation. These three controls are discussed below.

Transport Layer Interrupts

Interrupt enabling for Transport Layer events is controlled by TIEN. TIEN = "0" will disable interrupts. When set to "1", the creation of interrupts is enabled. Transport Layer Events are defined in Table 22.

Table 22. Transport Layer Events

Event	Source	-VE Control
RLOS	Rx Line Interface	Yes
RFE	Rx Framer	Yes
RSEF	Rx Framer	Yes
RLOF	Rx Framer	Yes
RAIS-L	Rx TOH Processor	Yes
RLE1	Rx TOH Processor	Yes
RRDI-L	Rx TOH Processor	Yes
B2EBER	Rx TOH Processor	Yes
RTNEW	Rx TOH Processor	No
RAPS	Rx TOH Processor	Yes
RAIS-P	Rx Pointer Tracking	Yes
RLOP	Rx Pointer Tracking	Yes
RB1COF	Rx TOH Processor	No
RB2COF	Rx TOH Processor	No
RLFEBEOF	Rx TOH Processor	No
Rx Inc OF	Rx Pointer Tracking	No
Rx Dec OF	Rx Pointer Tracking	No
RPJOF	Rx Pointer Tracking	No
RNPTR	Rx Pointer Tracking	No
RCPTR	Rx Pointer Tracking	Yes
LPJOF	Rx Pointer Generation	No
TLOS	Tx Terminal Port	Yes
TFE	Tx Terminal Framer	Yes
TSEF	Tx Terminal Framer	Yes
TLOF	Tx Terminal Framer	Yes
TAIS-L	Tx Terminal Processor	Yes
TTE1	Tx Terminal Processor	Yes
TAIS-P	Tx Terminal Pointer Tracking	Yes
TLOP	Tx Terminal Pointer Tracking	Yes
Tx Inc OF	Tx Terminal Pointer Tracking	No
Tx Dec OF	Tx Terminal Pointer Tracking	No
TCPTR	Tx Terminal Pointer Tracking	Yes
TNPTR	Tx Terminal Pointer Tracking	No

Path Layer Interrupts

Interrupt enabling for Path Layer events is controlled by PIEN. PIEN = "0" will disable interrupts. When set to "1", the creation of interrupts is enabled. Path Layer Events are defined in Table 23.

Table 23. Path Layer Events

Event	Source	-VE Control
RRDI-P	Rx POH Processor	Yes
B3EBER	Rx POH Processor	Yes
C2MIS	Rx POH Processor	Yes
C2UNEQ	Rx POH Processor	Yes
RLOM	Rx POH Processor	Yes
RPNEW	Rx POH Processor	No
RB3COF	Rx POH Processor	No
RPFEBEOF	Rx POH Processor	No

Device Layer Interrupts

Interrupt enabling for Device Layer events is controlled by DIEN. DIEN = "0" will disable interrupts. When set to "1", the creation of interrupts is enabled. Device Layer Events are defined in Table 24.

Table 24. Device Layer Events

Event	Source	-VE Control
RLOC	Rx Line Interface	Yes
RLFRI	Rx Line Interface	Yes
RRCOFA	Terminal Timing Generation	No
RFIFOE	Rx Re-timing FIFO	No
TAISV	Alarm Port	Yes
TLOC	Tx Terminal Port	Yes
LOTR	Line Timing Generation	Yes
TRCOFA	Line Timing Generation	No
TFIFOE	Tx Re-timing FIFO	No

TEST AND DIAGNOSTICS

For testing and diagnostic purposes the SOT-1 provides Loopbacks (previously discussed), and Output Tri-state capability.

Output Disable

The pin $\overline{\text{TEST}}$ is a control that when taken Low, with RST held High, will force all output pins, and bidirectional pins acting as outputs, to a high impedance state. $\overline{\text{TEST}}$ at the Low Level by itself invokes a TXC Device Test Mode. For normal operation $\overline{\text{TEST}}$ must be at the "1" Logic Level.

PACKAGE INFORMATION

The SOT-1 is packaged in an 84-pin plastic leaded chip carrier suitable for socket or surface mounting, as shown in Figure 47. All dimensions are in inches and are nominal unless otherwise noted.

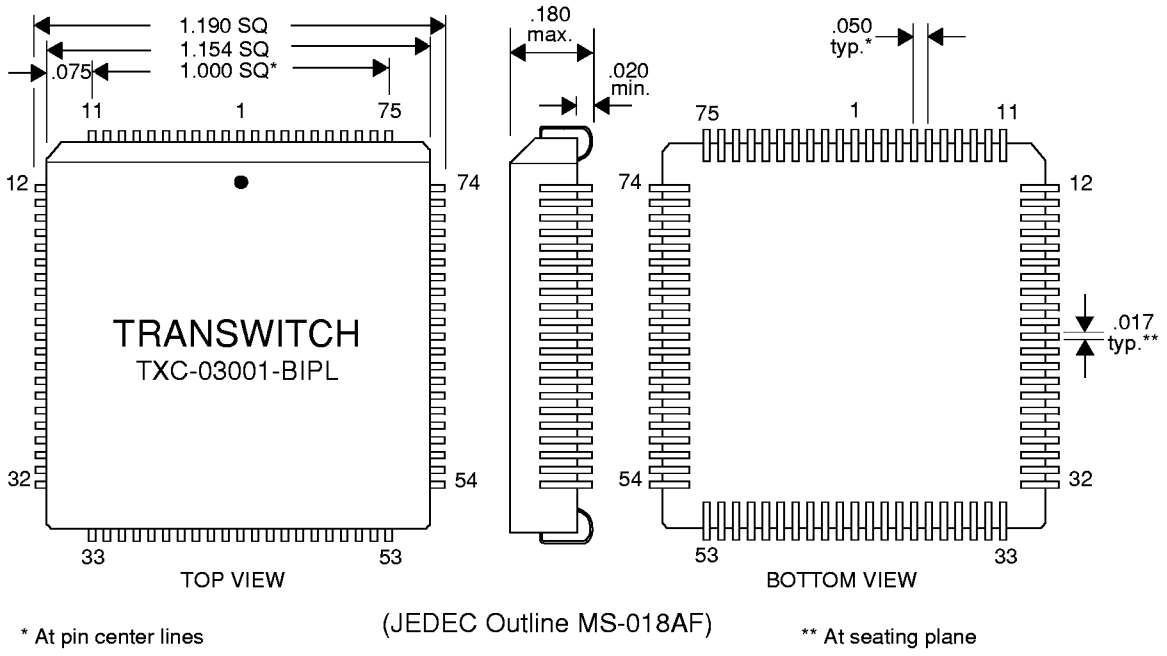


Figure 47. SOT-1 TXC-03001B 84-Pin Plastic Leaded Chip Carrier

ORDERING INFORMATION

Part Number: TXC-03001-BIPL	84-pin Plastic Leaded Chip Carrier

RELATED PRODUCTS

TXC-02020, ART VLSI Device (Advanced STS-1/DS3 Receiver/Transmitter) - ART performs the transmit and receive line interface functions for interfacing STS-1 (51.84 Mb/s) and DS3 (44.736 Mb/s) signals at a coaxial interface.

TXC-02021, ARTE VLSI Device (Advanced STS-1/DS3 Receiver/Transmitter) - ARTE performs the same functions as ART with expanded features.

TXC-03452B, L3M VLSI Device (Level 3 Mapper/De-synchronizer) - L3M maps a DS3 or E3 signal into an SDH/SONET signal formatted for STM-n (VC-3 via TU-3) or STS-n (via STS-1 SPE).

TXC-04001B, ADMA-T1 VLSI Device (Dual DS1 to VT1.5 Async, Mapper/De-synchronizer) - ADMA-T1 maps two asynchronous DS1 signals into any two VT1.5s of a SONET STS-1 SPE.

TXC-04011, ADMA-T1P VLSI Device (Dual DS1 to VT1.5 Async, Mapper/De-synchronizer) - ADMA-T1P performs the same functions as ADMA-T1 with support of Add Bus Timing Mode. It is packaged in a 120 pin PQFP.

TXC-04251, QT1M VLSI Device (Quad DS1 to TU-11/VT1.5 Async, Mapper/De-synchronizer) - QT1M maps four asynchronous DS1 signals into SDH (TU-11 via TUG-2 and TUG-3) or SONET (VT1.5 via VTG and STS-1 SPE).

TXC-04252, QE1M VLSI Device (Quad E1 to TU-12/VT2 Async, Mapper/De-synchronizer) - QE1M maps four asynchronous E1 signals into SDH (TU-12 via TUG-2 and TUG-3) or SONET (VT2 via VTG and STS-1 SPE).

TXC-05150, CDB VLSI Device (Cell Delineation Block) - CDB provides cell delineation for ATM cells carried in a physical line at rates of 1.544 Mb/s to 155.52 Mb/s.

TXC-06125, XBERT VLSI Device (Bit Error Rate Generator/Receiver) - XBERT is a programmable multi-rate test pattern generator and checker with serial, nibble, or byte interface capabilities.

STANDARDS DOCUMENTATION SOURCES

Telecommunication technical standards and reference documentation may be obtained from the following organizations:

ANSI (U.S.A.):

American National Standards Institute (ANSI)
11 West 42nd Street
New York, New York 10036

Tel: 212-642-4900
Fax: 212-302-1286

The ATM Forum:

ATM Forum World Headquarters
303 Vintage Park Drive
Foster City, CA 94404-1138

Tel: 415-578-6860
Fax: 415-525-0182

ATM Forum European Office
14 Place Marie - Jeanne Bassot
Levallois Perret Cedex
92593 Paris France

Tel: 33 1 46 39 56 26
Fax: 33 1 46 39 56 99

Bellcore (U.S.A.):

Bellcore
Attention - Customer Service
8 Corporate Place
Piscataway, NJ 08854

Tel: 800-521-CORE (In U.S.A.)
Tel: 908-699-5800
Fax: 908-336-2559

EIA - Electronic Industries Association (U.S.A.):

Global Engineering Documents
Suite 407
7730 Carondelet Avenue
Clayton, MO 63105

Tel: 800-854-7179 (In U.S.A.)
Fax: 314-726-6418

ITU-TSS (International):

Publication Services of International Telecommunication Union (ITU)
Telecommunication Standardization Sector (TSS)
Place des Nations
CH 1211
Geneve 20, Switzerland

Tel: 41-22-730-5285
Fax: 41-22-730-5991

MIL-STD Military Standard (U.S.A.):

Standardization Documents Order Desk
700 Robbins Avenue
Building 4D
Philadelphia, PA 19111-5094

Tel: 212-697-1187
Fax: 215-697-2978

TTC (Japan):

TTC Standard Publishing Group of the
Telecommunications Technology Committee
2nd Floor, Hamamatsucho - Suzuki Building,
1 2-11, Hamamatsu-cho, Minato-ku, Tokyo

Tel: 81-3-3432-1551
Fax: 81-3-3432-1553

LIST OF DATA SHEET CHANGES

This change list identifies those areas within this updated SOT-1 (TXC-03001B) Data Sheet that have significant differences relative to the previous and now superseded SOT-1 (TXC-03001B) Data Sheet:

Updated SOT-1 Data Sheet: Edition 2, February 1998

Superseded SOT-1 Data Sheet: *PRODUCT PREVIEW* Edition 1, May 1996

The page numbers indicated below of this updated data sheet include changes relative to the superseded data sheet.

Page Number of Updated Data Sheet	Summary of the Change
All	Changed edition number and date.
All	Deleted *PRODUCT PREVIEW* document status markings, and associated explanatory text from pages 1 and 153.
Where Applicable	Deleted all references to Datacom Mode. Changed pin symbols TSPEI/O to TSPEI, TSYNI/O to TSYNI, TTCI/O to TTCI and TPCI/O to TPCI. Changed Tx TOH Generator to Tx OH Generator. Changed Physical Layer to Physical Medium Layer. Deleted Memory Map bits with symbols DATACOM, ENDCMPOH, DISPCKG, TB3COF, TB2COF, TB1COF, TDDLY. Changed TranSwitch street address in Shelton, CT.
2	Updated Table of Contents and added a note to the bottom.
3-4	Updated List of Figures, List of Tables and List of Equations.
11	Clarified TOH is Transport Overhead for the first sentence of the first paragraph.
13	Modified the last sentence of the first paragraph.
15	Made changes to the Z2 definition.
19	Made changes to Figure 14.
20	Modified Transmit Side section.
22	Moved notes from page 27 to this page. Deleted the last sentence from the Name/Function column of TLCI.
23	Made changes to Name/Function column for TLCO, RTDO, TPCO, TPDO(0-7), RSPE and RSYN. Added Note 1 and references thereto.
24	Modified TTCI and TPCI. Made changes to Name/Function column for TTDI and TPDI(0-7).
25	Made changes to Name/Function column for SPFR, LRFR, $\overline{\text{RAP}}$/$\overline{\text{RTS}}$, OTDI, STFR, LTFR and $\overline{\text{TAP}}$/$\overline{\text{TTS}}$.
26	Made changes to Name/Function column for SRDO, LRDO, STDI and LTDI.

Page Number of Updated Data Sheet	Summary of the Change
27	Made changes to Name/Function column for AD(0-7), $\overline{WR}$, $\overline{RD}$, RDY, INT and $\overline{SEL}$.
28	Made changes to all three tables.
30	Modified the first paragraph. Changed Parameter and Max columns for t_F and t_R. Changed Parameter, Min and Max columns for t_{PWH} and t_{PWL}.
31	Clarified the Terminal Timing in Parallel Modes section.
32	Changed Parameter and Max columns for t_F and t_R. Clarified Parameter column for t_{PWH} and t_{PWL}.
33	Clarified Parameter column for t_{FO}, t_{PWHO}, t_{PWLO} and t_{RO}.
34	Clarified Parameter column for t_F, t_{PWH}, t_{PWL} and t_R.
35	Added Max to t_{CYC}. Changed Max column for t_F. Clarified Parameter column for t_F, t_{PWH}, t_{PWL} and t_R.
36	Clarified Parameter column for t_F, t_{PWH}, t_{PWL} and t_R of both tables.
37	Changed Max column for t_F and t_R of both tables. Clarified Parameter column for t_F, t_{PWH}, t_{PWL} and t_R of both tables. Added Note 1 to both tables.
38	Modified Figure title. Clarified Parameter column for t_{FO}, t_{RO}, t_{PWHO} and t_{PWLO}.
39	Clarified Parameter column for t_{FO}, t_{RO}, t_{PWHO} and t_{PWLO}. Changed Min, Typ and Max columns for t_{PWL}. Deleted t_{PWL1}.
40	Clarified Parameter column for t_{FO}, t_{RO}, t_{PWHO} and t_{PWLO}. Changed Notes column for t_{D1} and t_{D2} and t_{PWHO}. Modified Note 5.
41	Clarified Parameter column for t_F, t_{PWH}, t_{PWL} and t_R. Changed Max column for t_F and t_R. Changed Min and Max columns for t_{PWH} and t_{PWL}. Deleted figure for Serial DATACOM Input Timing.
42	Clarified Parameter column for t_F, t_{PWH}, t_{PWL} and t_R. Changed Min column for t_{PWH} and t_{PWL}. Deleted figure for Parallel DATACOM Input Timing.
43-45	Made changes to the waveform diagrams, tables and notes.
46	Modified the paragraphs. Added Not Equipped to Usage column of Figure 34.
48	Made changes to Description column for Address 01B.
50	Made changes to Control Bits and Description columns for Address 040.
53	Made changes to Control Bits and Description columns for Addresses 0C2 and 0D2.

Page Number of Updated Data Sheet	Summary of the Change
55	Added notes to Bits 4 and 0 of Address 0FB, Bits 2-1 of Address 0FD, and Bit 7 of Address 0FF. Changed Bits 6-4 of Address 0FD to Unused. Modified Note 1 and added Note 5.
56	Added Status Bit to Addresses 119-11F. Made minor changes to Description column for Addresses 125-127.
57	Made minor changes to Description column for Addresses 128-130, 136 & 137, 138, 139, 13A, 13B and 13C.
58	Made changes to Description column for Addresses 13D, 13E & 13F, 146 and 147.
59	Added J1SYNCEN to Control Bits column for Addresses 180 - 1BF. Made changes to Description column for Address 1CA.
60	Deleted Status Bits and made changes to Description column for Address 1D4.
61	Added note(s) to Bits 2 and 1 of Address 1DC, Bits 1 and 0 of Address 1DE, Bit 4 of Address 1FB, Bits 1 and 0 of Address 1FC and Bits 7-4, 2-0 of Address 1FD. Changed Bits 7-5 of Address 1F6. Modified Note 1 and added Note 5.
62	Clarified Enter column for RNPTR. Made changes to Exit column for RAIS-P.
63	Made changes to Enter column for RTNEW.
64-65	Made changes to Conditions column for TLOC and TLOS. Made changes to Enter column for TNPTR. Made changes to Exit column for TAIS-P.
65-66	Made changes to Comments column for RLFRI, RFE, B2EBER, B3EBER, RCPTR, C2MIS, C2UNEQ and RLOM. Changed C2 Reg. 01 from 01 to 00 for C2MIS.
67	Deleted Comments from RRCOFA and TAISV. Made changes to Comments column for LORR and RLE1. Made changes to Enter and Comments columns for RFIFOE.
68	Made changes to Comments column for TFE, TCPTR, TTE1. Made changes to Enter and Comments columns for TRCOFA and TFIFOE. Made changes to Enter column and deleted Comments for LOTR.
69	Made changes to Comments column for RRDI-PSD, RRDI-PCD, RRDI-PPD, RPDI-P and J0MIS.
71	Changed Bits 7-5 to Reserved.
72	Made changes to Enter column for REG2, REG4 and REG5.
75	Made changes to Rx Terminal AIS-P Insertion section.
78	Added Note 2 to Comments column for Bits 4 and 0.

Page Number of Updated Data Sheet	Summary of the Change
79	Deleted notes from the table.
80	Changed Bits 6-4 to Unused. Made changes to Conditions column for Bits 3 and 0. Modified the notes.
81	Deleted Conditions column for Reserved. Modified Comments column and the notes.
82	Made changes to Comments column for TIDL. Made changes to Conditions and Comments columns for TPFEBEEN.
83	Deleted Comments for TPRDIEN, C2MPRDI and C2UPRDI. Changed Comments for Reserved. Modified Note 1 and deleted Note 5.
86	Made changes to Conditions column for TRAIS.
87	Made changes to Comments for RRB2. Modified the notes. Added Note 8 to Comments column for NWFTREN.
88	Deleted Note 8 from Comments column for RTDSEL. Modified the notes.
89	Changed Bit 5 of Address 1FB. Added Note 1 to Bit 4 (Unused).
90	Made changes to Conditions column for RA2E.
92	Modified Comments column and the notes. Changed Bit 0 to Unused.
93	Made changes to Conditions column for TXH4INS. Added Note 1.
94	Deleted Note 3.
95-96	Modified Comments and the notes for both tables. Made changes to Conditions column for TTEAIS.
97	Deleted Comments from LINLOOP, DISTB2R and TPRDI2O. Modified Note 2.
98	Made changes to Comments for Bits 5, 4, 3, 2 and 1. Modified the notes.
99	Deleted Conditions column for Bits 7 and 6. Made changes to Comments column. Modified the notes.
100-101	Made changes to Primary Operating Modes section.
101-102	Made changes to Line Timing Generator section.
103-104	Made changes to Tx Side and Rx Line Port Format section.
105	Made changes to the first paragraph.
106	Deleted Serial Datacom and Parallel Datacom sections.

Page Number of Updated Data Sheet	Summary of the Change
113	Rx B2 Processing: Changed Locations for B2SCV and B2CCV. Table 6: Changed the last column.
113-114	Added last two paragraphs and Table 7.
114	Made changes to Rx Line FEBE Processing section.
117	Rx B3 Processing: Changed Locations for B3SCV and B3CCV. Changed value of B3CCV to 1. Added Table 12.
118	Made changes to Rx Path FEBE Processing section.
122	Added note to Table 15.
124	Made changes to Tx Terminal Inputs and Input Frame Delineation sections.
125	Made changes to Input B1 Processing and Input B2 Processing sections.
126	Added note to Table 17. Made changes to Input B3 Processing section.
128-129	Made changes to Transmit POH Assembly section.
130	Made changes to the second paragraph of Tx Idle Insertion section.
131	Added note to Table 20.
134	Tx H1-H3 Selection: added TCLK to the table.
137	Made changes to the first sentence of Tx Line FEBE Insertion section. Made changes to Tx Path AIS Insertion, Tx Line RDI Insertion and Tx Line AIS Insertion sections.
138	Made changes to the first paragraph of Loopbacks section. Made changes to the second paragraph of Tx-Rx Line Loopback section.
139	Added the last sentence to Rx-Tx Terminal Loopback section.
139-142	Made changes to Resets and Microprocessor Interface sections.
143	Made changes to Test and Diagnostics section.
145	Changed Product Number for L3M to TXC-03452B.
146-147	Added EIA and MIL-STD to Standards Documentation Sources section.
148-152	Added List of Data Sheet Changes.

- NOTES -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