FUJITSU

# 8-CHANNEL 8-BIT A/D CONVERTER

# MB4056

April 1988
Edition 2.0

## 8-CHANNEL 8-BIT A/D CONVERTER

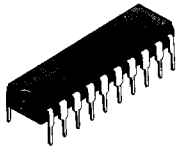
The Fujitsu MB4056 is an analog-to-digital converter (ADC) for general purpose which features eight channels of analog inputs and 8-bit data length of digital output.

Analog input signal is converted to serial 8-bit digital data by the successive-approximation technique which provides high-speed conversion, i.e. many analog data can be converted within a short time.

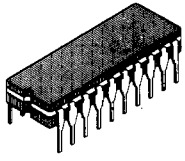
Additionally, the MB4056 has dual range conversion capability, which provides sequentially one data of both range, standard and contracted modes, to chose better data between them and to delete the range change time.

All digital I/O signals including control inputs are TTL level compatible so as to provide wide application such as in microprocessor-controlled system and so on.

- Single Power Supply: +4.75 V to +18 V
- Multiplex 8-Channel Analog Inputs:
- Resolution: 8 bits
- Linearity Error: ±0.19% Max.
- Analog Input Voltage Ranges:
  Automatic Range Change/Dual Range Conversion: 0 to 5 V Standard mode
  0 to 1.25 V Contracted mode
- Successive-Approximation Conversion: 100 μs/ch Max. at $f_{CLK}$ = 100 kHz, S/D = 1
  200 μs/ch Max. at $f_{CLK}$ = 100 kHz, S/D = 0
- Ratio-metric Conversion by Reference Voltage $V_{REF}$
- Analog Input Bias Current: 250 nA Max.
- TTL/CMOS Compatible Digital I/O
- Power Consumption: 160 mW Typ. at $V_{CC}$ = 8V
- Standard 20-pin Plastic Package: Suffix: -P
  Standard 20-Pin Ceramic Package: Suffix: -Z

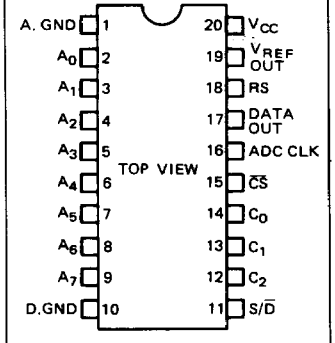


PLASTIC PACKAGE
DIP-20P-M01



PLASTIC PACKAGE
DIP-20C-C03

**PIN ASSIGNMENT**




**ABSOLUTE MAXIMUM RATINGS (See NOTE)**

| Rating | | Symbol | Value | Unit |
|---|---|---|---|---|
| Power Supply Voltage | | $V_{CC}$ | +20 | V |
| Digital Input Voltage | | $V_{IH}$ | +20 | V |
| Digital Output Voltage (Off-State) | | $V_{OH}$ | +20 | V |
| Analog Input Voltage | | $V_{IA}$ | +20 | V |
| Storage Temperature | Ceramic | $T_{STG}$ | −55 to +150 | °C |
| | Plastic | $T_{STG}$ | −40 to +125 | °C |

**NOTE:** Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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Fig. 1 – MB4056 BLOCK DIAGRAM

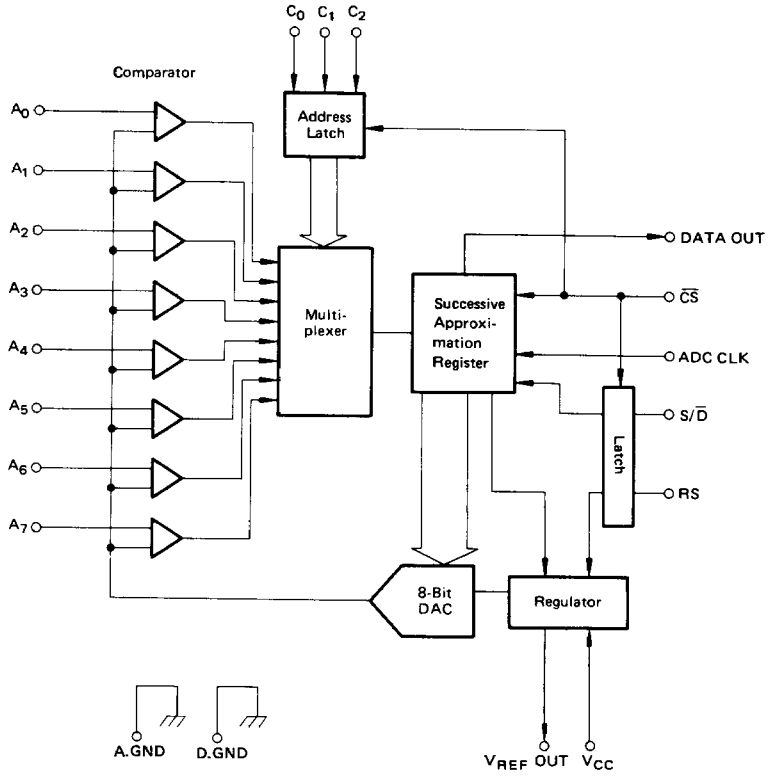


**TABLE 1: CONVERSION MODES**

| S/D | RS | 1st Conversion | 2nd Conversion |
|---|---|---|---|
| L | L | Contracted Range | Standard Range |
| L | H | Standard Range | Contracted Range |
| H | L | Contracted Range | – |
| H | H | Standard Range | – |

**TABLE 2: CHANNEL SELECTIONS**

| $C_2$ | $C_1$ | $C_0$ | Channel |
|---|---|---|---|
| 0 | 0 | 0 | $A_0$ |
| 0 | 0 | 1 | $A_1$ |
| 0 | 1 | 0 | $A_2$ |
| 0 | 1 | 1 | $A_3$ |
| 1 | 0 | 0 | $A_4$ |
| 1 | 0 | 1 | $A_5$ |
| 1 | 1 | 0 | $A_6$ |
| 1 | 1 | 1 | $A_7$ |

# PIN DESCRIPTIONS

| Pin Name | Pin No. | Descriptions |
|---|---|---|
| $A_0$ to $A_7$ | 2 to 9 | **Analog Inputs**<br>These inputs are provided to receive eight channels of analog inputs. One of them is selected by a combination of $C_0$ to $C_2$. |
| S/$\overline{D}$ | 11 | **Conversion Mode Select Input**<br>This control input is provided to select a conversion sequence with RS input as shown in Table 1. When low, analog input voltage is converted in both ranges, and when high, in one range only. This input is latched at the falling edge of $\overline{CS}$. |
| $C_2$ to $C_0$ | 12 to 14 | **Channel Select Inputs**<br>These inputs are used to select one of eight analog input as shown in Table 2. This inputs are latched at the falling edge of $\overline{CS}$. |
| $\overline{CS}$ | 15 | **Chip Select Input**<br>This control input is used to start analog to digital conversion and to terminate it. When $\overline{CS}$ goes low, the A/D conversion starts and the DATA OUTPUT is enabled. When the A/D conversion is completed or termination of the conversion is required, $\overline{CS}$ is made high. |
| ADC CLK | 16 | **A/D Conversion Clock**<br>This clock signal is used for A/D conversion. The conversion speed is determined by this clock rate. But precise stability of the clock rate is no required. |
| DATA OUT | 17 | **Data Outputs**<br>This output is provided to output the A/D conversion results as digital signals. The converted digital data are serially output in the order of start-bit, MSB (Most Significant Bit), 2SB (Second Significant Bit), . . . , 7SB, LSB (Least Significant Bit) and stop-bit in synchronous with the ADC CLK. |
| RS | 18 | **Range Select Input**<br>This control input is provided to select an analog input voltage as shown in Table 1. This input is latched at the falling edge of $\overline{CS}$. |
| $V_{REF}$ | 19 | **Reference Voltage Output**<br>This output provides the regulated 5V when $V_{CC}$ is between 8V and 18V. About 10mA current of the output is supplyed externally. |
| A. GND<br>D. GND | 1<br>10 | Analog Ground<br>Digital Ground |
| $V_{CC}$ | 20 | Power Supply Voltage, 4.75V to 18V. |

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## RECOMMENDED OPERATING CONDITIONS

| Parameter | Symbol | Value | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| Power Supply Voltage | $V_{CC}$ | 4.75 | 12 | 18 | V |
| Digital output Low Current | $I_{OL}$ | | | 8 | mA |
| Ambient Operating Temperature | $T_A$ | -40 | | +85 | °C |

## ANALOG CIRCUIT CHARACTERISTICS

($V_{CC}$ = 4.75 to 18V, $T_A$ = -40 to 85°C)

| Parameter | | Symbol | Condition | Value | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Max | Typ | Max | |
| Resolution | | | | | | 8 | bit |
| Linearity Error | | | | | | ±0.5 | LSB |
| Differential Linearity Error | | | | | | ±0.9 | LSB |
| Zero Transition Voltage | | $V_{ZS}$ | Standard Conversion Mode $8V \leq V_{CC} \leq 18V$ | | 20 | | mV |
| Full Scale Transition Voltage | | $V_{FS}$ | | | 4980 | | mV |
| Zero Transition Voltage | | $V_{ZC}$ | Contracted Conversion Mode $4.75V \leq V_{CC} \leq 18V$ | | 5 | | mV |
| Full Scale Transition Voltage | | $V_{FC}$ | | | 1245 | | mV |
| Comparator Input Current | | $I_{COP}$ | | | | -250 | nA |
| Regulator | Output Voltage | | $8V \leq V_{CC} \leq 18V$ | 4.5 | 5.0 | 5.5 | V |
| | Line Regulation | | $8V \leq V_{CC} \leq 18V$ | | 4.0 | | mV/V |
| | Load Regulation | | $V_{CC}$ = 12V $-10mA \leq I_{OUT} \leq 0mA$ | | 0.5 | | mV/mA |
| | Output Voltage Change with Temperature | | $V_{CC}$ = 12V | | 50 | | PPm/°C |
| Conversion Time | | $t_{CYC1}$ | $f_{CLK}$ = 100kHz, S/D = "1" | | | 100 | µs/CH |
| | | $t_{CYC0}$ | $f_{CLK}$ = 100kHz, S/D = "0" | | | 200 | µs/CH |

## DIGITAL CIRCUIT DC CHARACTERISTICS

($V_{CC}$ = 4.75 to 18V, $T_A$ = –40 to 85°C)

| Parameter | Symbol | Condition | | Value | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | |
| Input High Voltage | $V_{IH}$ | | | 2.0 | | | V |
| Input Low Voltage | $V_{IL}$ | | | | | 0.8 | V |
| Input Clamp Voltage | $V_{IC}$ | $I_{IL}$ = –18mA | | | | –1.5 | V |
| Output High Current | $I_{OH}$ | $V_{IH}$ = 2V, $V_{IL}$ = 0.8V<br>$V_{OH}$ = 20V | | | | 100 | μA |
| Output Low Voltage | $V_{OL}$ | $V_{IH}$ = 2V<br>$V_{IL}$ = 0.8V | $I_{OL}$ = 4mA | | | 0.4 | V |
| | | | $I_{OL}$ = 8mA | | | 0.5 | V |
| Input High Current | $I_{IH}$ | $V_{IH}$ = 2.7V | | | | 20 | μA |
| | | $V_{IH}$ = 20V | | | | 100 | μA |
| Input Low Current | $I_{IL}$ | $V_{IL}$ = 0.4V | | | –20 | –100 | μA |
| Power Supply Current | $I_{CC}$ | $V_{CC}$ = 20V | | | 20 | 38 | mA |

## DIGITAL CIRCUIT AC CHARACTERISTICS

($V_{CC}$ = 4.75 to 18V, $T_A$ = –40 to 85°C)

| Parameter | Symbol | Value | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| ADC CLK Cycle Time | $t_{CY}$ | 10 | | | μs |
| ADC CLK H level Pulse Width | $t_{WAC}{}^{+}$ | 2.5 | | | μs |
| ADC CLK L level Pulse Width | $t_{WAC}{}^{-}$ | 2.5 | | | μs |
| $\overline{CS}$ H level Pulse Width | $t_{WCS}{}^{+}$ | 1.5 | | | μs |
| $\overline{CS}$ Set-up Time | $t_{SCS}$ | 1 | | | μs |
| $\overline{CS}$ Hold Time | $t_{HCS}$ | 1 | | | μs |
| Channel Set-up Time | $t_{SCH}$ | 0 | | | μs |
| Channel Hold Time | $t_{HCH}$ | 1.5 | | | μs |
| Propagation Delay Time | $t_{PLH}$ | | 0.8 | 2 | μs |
| | $t_{PHL}$ | | 0.8 | 2 | μs |

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Fig. 2 – AC MEASUREMENT CIRCUIT

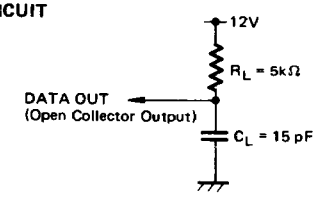


Fig. 3 – AC TIMING DIAGRAM

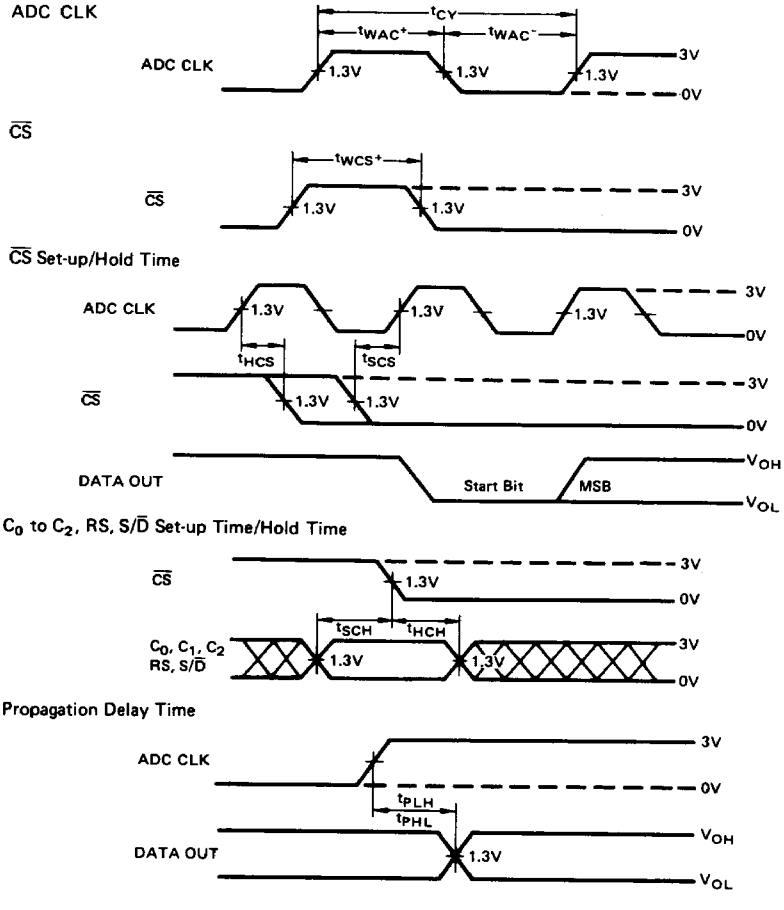


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Fig. 4 – TIMING DIAGRAM (S/$\overline{D}$ = "0")

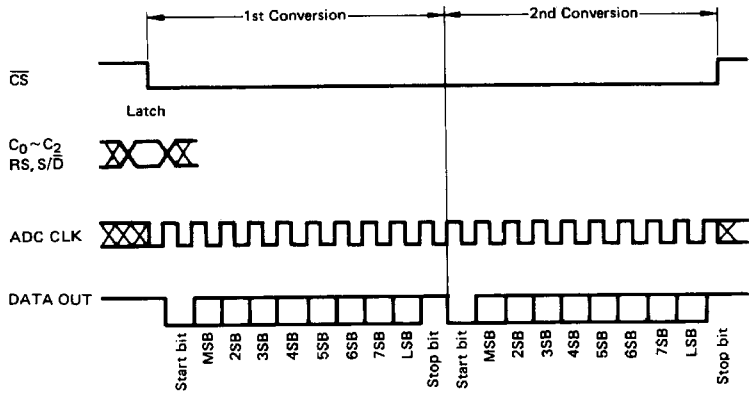
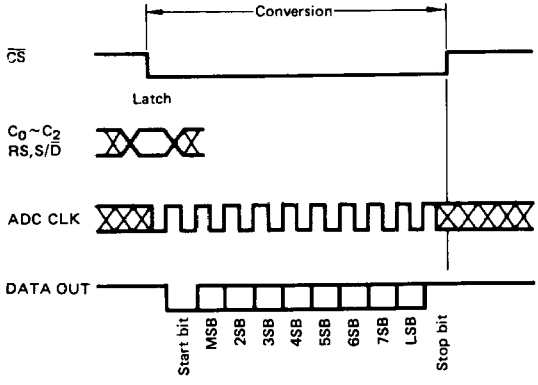



Fig. 5 – TIMING DIAGRAM (S/$\overline{D}$ = "1")

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# TYPICAL CHARACTERISTICS CURVES

Fig. 6 – ALLOWABLE $V_{REF}$ OUT PIN OUTPUT CURRENT vs. POWER SUPPLY VOLTAGE

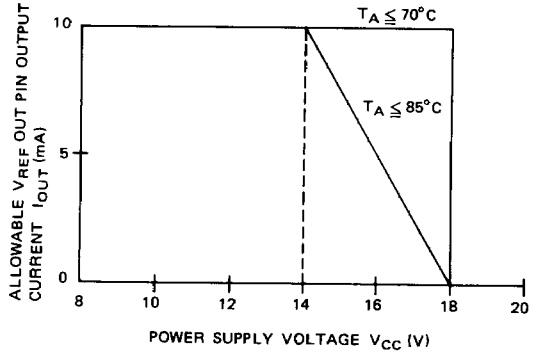
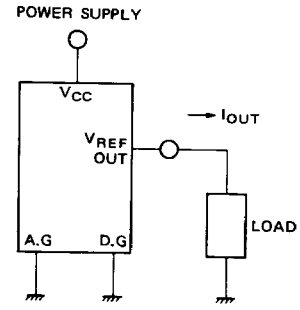



Fig. 7 – MEASUREMENT CIRCUIT

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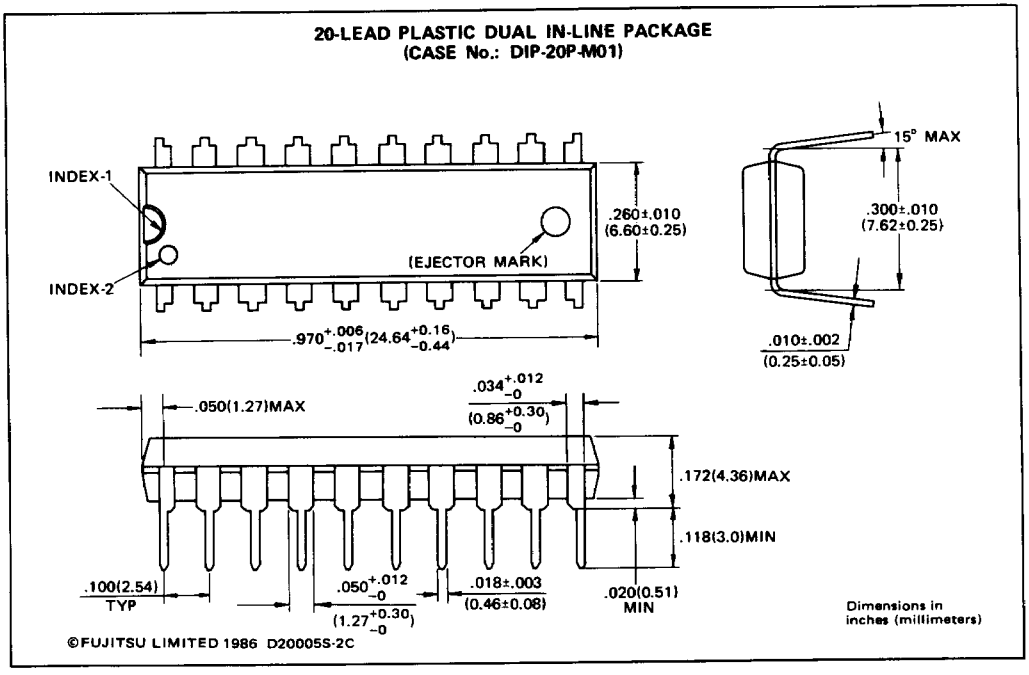
# PACKAGE DIMENSIONS

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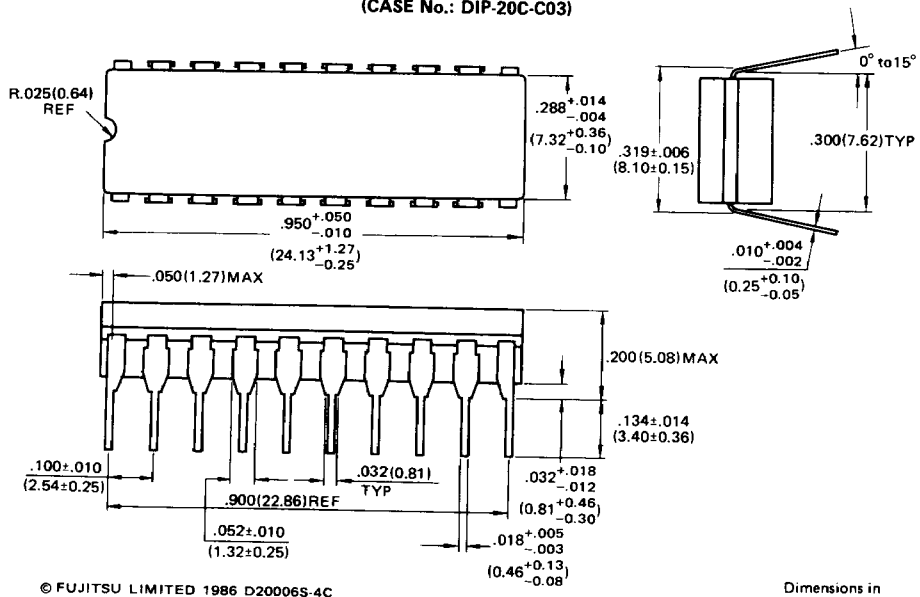
## PACKAGE DIMENSIONS (continued)

20-LEAD CERAMIC (CERDIP) DUAL IN-LINE PACKAGE
(CASE No.: DIP-20C-C03)






Dimensions in
inches (millimeters)

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