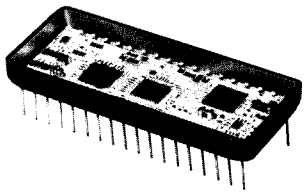
DDC
ILC DATA DEVICE CORPORATION

SDC-14520 MONOBRID® SERIES

16 BIT MONOLITHIC HYBRID S/D AND R/D TRACKING CONVERTERS



DESCRIPTION

The SDC-14520 Monobrid® Series* is a complete 16 bit synchro-to-digital or resolver-to-digital converter contained in a single hybrid module. Most of its circuitry has been incorporated into a custom designed monolithic chip, thereby greatly reducing parts count inside the hybrid. The Monobrid™ combination of monolithic and hybrid technologies allows a more sophisticated design with better performance and additional features to fit inside a standard 36 pin DDIP hybrid package. Power consumption is reduced, reliability is increased, and costs are lower.

New features found in the SDC-14520 Series are 3-state output in two bytes; ± 1.3 minute accuracy; transparent latch, which allows continuous tracking while an inhibit is applied; and control transformer capability. Included are other innovative features, found in recent DDC Synchro Converters, such as analog velocity output, error voltage output, solid state signal and reference isolation, broadband input and capability to accommodate non-standard line-to-line voltage levels.

The SDC-14520 Series is available in accuracy grades of ±1.3, ±2.6 and ±5.3 minutes. The accuracy is not affected by carrier amplitude variation because the conversion is ratiometric. Phase sensitive detection in the error loop rejects quadrature and noise. Adjustments and calibration are never required.

The SDC-14520 Series accepts broadband inputs: 360 to 1000 Hz or 47 to 1000 Hz. The input signal isolation is solid state and the internal differential solid state input has high common mode rejection.

Output angle is natural binary code, parallel positive logic, and TTL/CMOS compatible. Synchronization to a computer is via a Converter Busy output and an Inhibit input.

Only one main power supply is required. Its +15V DC nominal level can range from +11 to +16.5 volts with no degradation in performance. The SDC-14520 is also connected to the external logic power supply. Internal logic is CMOS, and all logic inputs and outputs are buffered to the external logic level. TTL or any external CMOS logic level between +4.5V and the +15V supply level can be accommodated.

APPLICATIONS

With three-state output and an Inhibit that does not stop the tracking process, SDC-14520 Series converters are especially suited for bus multiplexing and interfacing with microprocessors. These converters are ideal for remotely located and hard to access equipment where low power requirements, small size, and high MTBF are critical. All units are processed to MIL-STD-883. They are well suited to the most stringent and severe industrial or military and avionics applications. In conjunction with other devices, they are easily adapted for closed loop control.

Designed for printed circuit board mounting by standard techniques, the SDC-14520 Series can be readily incorporated into other equipment by the OEM user. Because of their low cost, they are competitive with discrete S/D converters in many applications.

FEATURES

- *LOW POWER: 100 mW TYPICAL*
- *ACCURACY: ±1.3 MINUTES*
- *3-STATE LATCHED OUTPUTS FOR MICROPROCESSOR DATA*
- *USEABLE AS CONTROL TRANSFORMER (CT)*
- *INHIBIT DOES NOT INTERRUPT TRACKING*
- *LOGIC: TTL AND CMOS COMPATIBLE 16 BIT PARALLEL BINARY ANGLE*

*Patented

Note: Monobrid® is a registered trademark of ILC Data Device Corporation.

SPECIFICATIONS

Over reference amplitude, temperature and power supply ranges; 10% signal amplitude variation; and up to 10% harmonic distortion in the reference.

PARAMETER	VALUE
RESOLUTION	16 bits
ACCURACY:	
–XX3 Accuracy Options	±5.3 minutes max.
–XX4 (see Ordering	±2.6 minutes max.
–XX5 Information)	±1.3 minutes max.
REFERENCE INPUT	
Carrier Frequency Ranges	
Nominal 400 Hz Units	360-1000 Hz
Nominal 60 Hz Units	47-1000 Hz
Reference Input Characteristics	
Voltage Range	4-130V rms
Input Impedance	250 KΩ min. single ended 500 KΩ min. differential
Common Mode Range	DC common mode plus recurrent AC peak = 210V max.

SYNCHRO/RESOLVER SIGNAL INPUTS

SOLID STATE BUFFER INPUT

Minimum Input Impedance (Balanced)

	Z_{IN} Line to Line	Z_{IN} Each Line to GND
Synchro		
90V L-L	130 KΩ	85 KΩ
11.8V L-L	17.5 KΩ	11.5 KΩ

	Z_{IN} Single Ended	Z_{IN} Differential	Z_{IN} Each Line to GND
Resolver			
90V L-L	175 KΩ	350 KΩ	175 KΩ
26V L-L	50 KΩ	100 KΩ	50 KΩ
11.8V L-L	23 KΩ	46 KΩ	23 KΩ

Common Mode Ranges	
For 90V L-L Input	182V max.
For 26 V L-L Input	60V max.
For 11.8V L-L Input	60V max.

DC Common mode plus recurrent AC peak

PARAMETER	VALUE
DIGITAL INPUT/OUTPUT	
Logic Type	TTL/CMOS compatible, depending on logic supply voltage
Outputs:	
16 Parallel Data Bits	Natural binary angle positive logic
Converter Busy (CB)	0.5-2.0 µs positive pulse, leading edge initiates counter update
Drive Capability	1 standard TTL load (1.6 mA at 0.4V max)
Inputs:	$Z_{IN} \geq 25K\Omega$ pull up resistor to V_L
Inhibit Input (INH)	INH – Logic 0 inhibits
Enable, Bits 1 to 8 ($\overline{EN\ MSB}$)	$\overline{EN\ MSB}$ and $\overline{EN\ LSB}$ – Logic 0 enables
Enable, Bits 9 to 16 ($\overline{EN\ LSB}$)	Logic 1 high impedance
$\overline{S}$	Logic 0 for use as CT

PARAMETER	VALUE
VOLTAGE FOLLOWER BUFFER INPUT (DIRECT)	
Input Signal Type	Sin and cos resolver signals referenced to converter internal ground V (not to external GND)
Sin/Cos Voltage Range	1V nominal, 1.15V max
Max. Voltage Without Damage	15V rms continuous. 100V peak transient
Input Impedance	$Z_{IN} > 10$ MΩ (transient protected voltage follower)
ANALOG OUTPUTS	
Internal Analog GND (V)	+15 VDC/2 ≅ 7V nominal
Unfiltered DC Error Voltage (D)	–14.5 mV DC average per LSB of error
DC Velocity Voltage ($\dot{\theta}$)	+1 VDC per +0.26 rps at 400 Hz +1 VDC per +0.068 rps at 60 Hz
DYNAMIC CHARACTERISTICS	
Input Rate	
At 400 Hz	0 to 1.25 rps min.
At 60 Hz	0 to .31 rps min.
Velocity Constant	$K_V = \infty$ (No limitation with Type II servo loop)
Acceleration Constant	
At 400 Hz	$K_a = 12{,}000\ sec^{-2}$ nominal
At 60 Hz	$K_a = 750\ sec^{-2}$ nominal
Settling Time	
For 179 Step Change	
At 400 Hz	500 ms max typ to 1 LSB 550 ms max to final value
At 60 Hz	1500 ms typ to 1 LSB 1600 ms max to final value
TEMPERATURE RANGES	
Operating	
–1 option	–55°C to +125°C
–3 option	0°C to +70°C
Storage	–55°C to +135°C

POWER SUPPLIES	+15 VDC	Logic Supply
Nominal Voltage		
Voltage Range	+11 to +16.5V	+4.5V to +15 Supply
Absolute Max Voltage	+18V	+18V
Current or Impedance	10 mA max.	Z_{IN} = 5 KΩ min.

PARAMETER	VALUE
PHYSICAL CHARACTERISTICS	
Type	36 pin double DIP
Size	0.78 x 1.9 x 0.21 inch (19.8 x 48.3 x 5.3 mm)
Weight	1 oz. max (28g)

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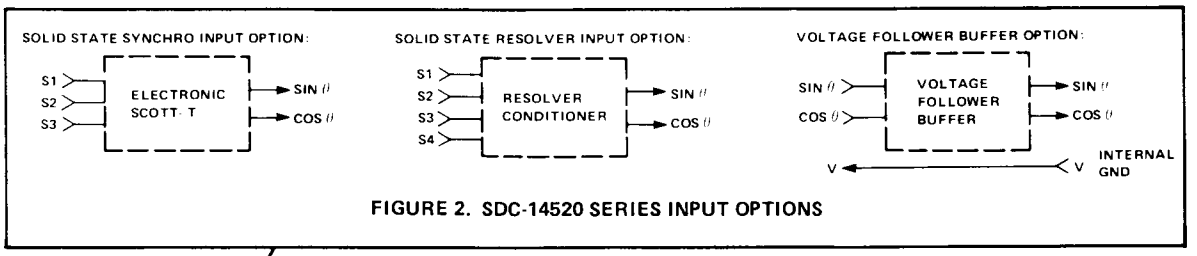


FIGURE 2. SDC-14520 SERIES INPUT OPTIONS

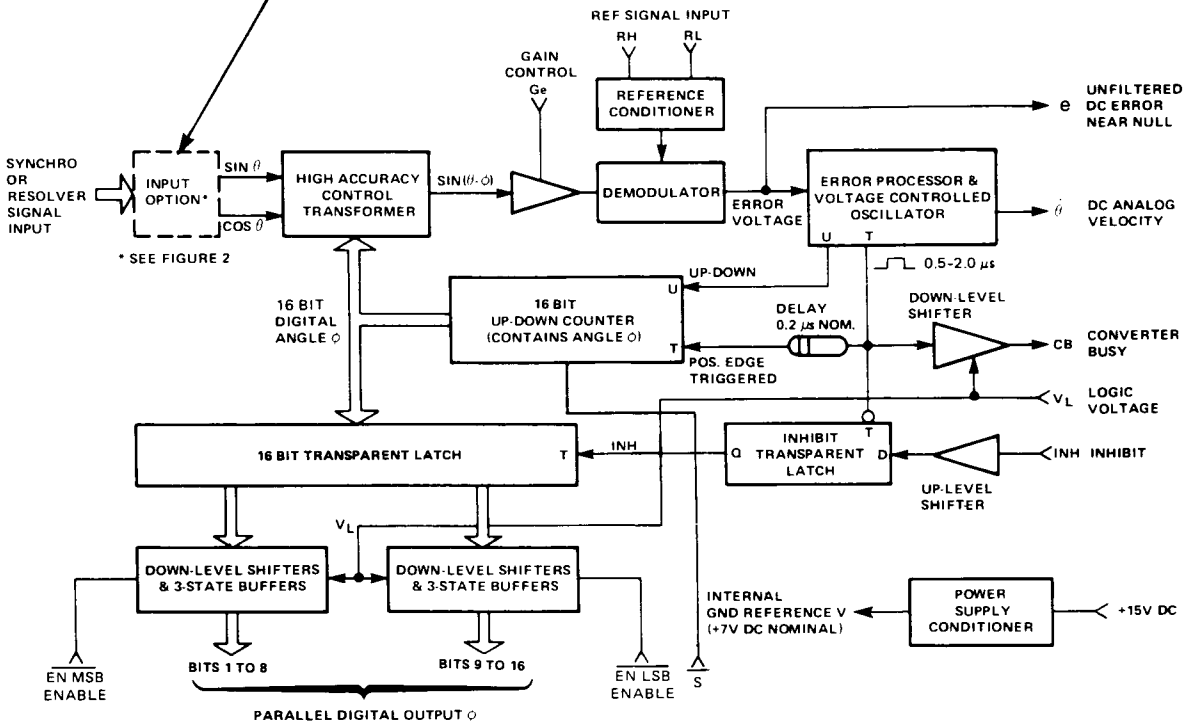


FIGURE 1. SDC-14520 SERIES BLOCK DIAGRAM

TECHNICAL INFORMATION

INTRODUCTION

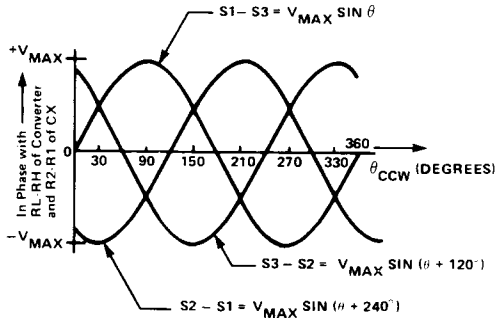
The circuit shown in the SDC-14520 block diagram, Figure 1, consists of three main parts: the signal input option; a feedback loop whose elements are the control transformer, demodulator, error processor, and up-down counter; and digital interface circuitry including various latches and buffers.

The input options accept a synchro or resolver input and produce a resolver type output for the control transformer. The first two options, called solid state synchro and resolver input (see Figure 2), accept synchro and resolver signal inputs directly, and provide signal isolation internally. The third option was designed for direct input, it is a voltage follower buffer and requires an external signal conditioner such as a transformer. Both options, the solid state input and the external transformer isolated buffer, are available for the following standard inputs:

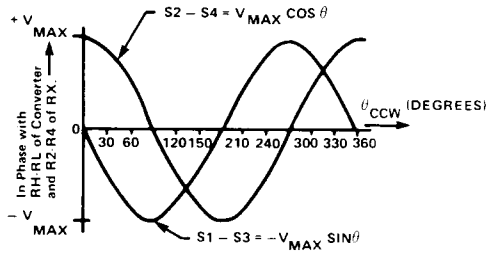
All input options are DC coupled with broadband characteristics up to 1000 Hz. SDC-14520 Series converters are useable to 10 KHz with slight degradation in accuracy-consult factory for further information.

In a synchro or resolver, shaft angle data is transmitted as the ratio of carrier amplitudes across the terminals. The internal converter operates with signals in resolver format, $\sin\theta \cos\omega t$ and $\cos\theta \cos\omega t$. Synchro signals are of the form $\sin\theta \cos\omega t$, $\sin(\theta + 120^\circ)\cos\omega t$, and $\sin(\theta + 240^\circ)\cos\omega t$. Diagrams on the following page show synchro and resolver signals as a function of the angle θ.

The feedback loop produces a 16 bit digital angle Φ which tracks the analog input angle θ to within the specified



Standard Synchro Control Transmitter (CX) Outputs as a Function of CCW Rotation From Electrical Zero (EZ).



Standard Resolver Control Transmitter (RX) Outputs as a Function of CCW Rotation From Electrical Zero (EZ) With R2-R4 Excited.

SYNCHRO AND RESOLVER SIGNALS

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accuracy of the converter. The control transformer performs the following trigonometric computation:

$$\sin(\theta - \Phi) = \sin\theta \cos\Phi - \cos\theta \sin\Phi$$

where θ is the angle representing the synchro or resolver shaft position, and Φ is the digital angle contained in the up-down counter in the converter. The tracking process consists of continually adjusting Φ to make $(\theta - \Phi) \rightarrow 0$, so that Φ will represent the shaft position θ.

The output of the demodulator is an analog DC level proportional to sin $(\theta - \Phi)$. The error processor integrates this sin $(\theta - \Phi)$ error signal, and the output of the integrator is used to control the frequency of a voltage controlled oscillator. This oscillator produces "clock" pulses which are accumulated by the up-down counter. The up-down counter is functionally an incremental integrator. Therefore there are two stages of integration, making the converter a Type II tracking servo. In a Type II servo, the voltage controlled oscillator always settles to a counting rate which makes $d\Phi/dt$ equal to $d\theta/dt$ without lag. The output data will always be fresh and available so long as the maximum tracking rate of the converter is not exceeded.

The digital interface circuitry has three main functions: to latch the output bits during an Inhibit command so that stable data can be read out, to furnish 16 bit parallel data in 3-state format, and to act as a buffer between the internal CMOS logic and the external logic level.

Applying an Inhibit command will lock the data in the 16 bit transparent latch without interfering with the continuous tracking of the feedback loop. This is a new feature, since S/D and R/D converters usually lock the up-down counter while an Inhibit is applied. In the SDC-14520 Series Monobrids, therefore, the digital angle Φ is always updated and the Inhibit can be applied for an arbitrary amount of time. The Inhibit transparent latch and the 0.2 μs delay are also parts of the Inhibit circuitry, whose detailed operation is described in the Logic Output/Input Section.

When testing or evaluating the converter, it is advisable to limit the power supply currents as follows:

+15V Supply Limit at 20 mA.
Logic Supply V_L at 2 mA + Digital Load at Logic 1.

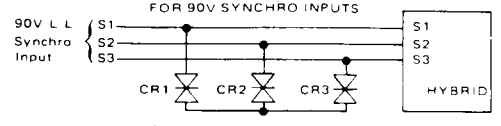
Analog circuits inside the SDC-14520 module are referenced to an internal reference ground level V which rides at +7V nominal with respect to the external ground (GND). V should not be connected to the external ground.

SOLID STATE BUFFER INPUTS

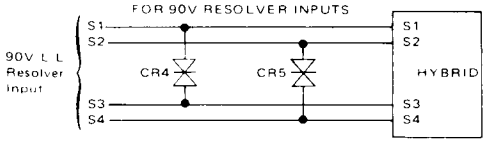
The solid state signal and reference inputs are true differential inputs with high AC and DC common mode rejection, so most applications will not require units with isolation transformers. Input impedance is maintained with power off. The recurrent AC peak + DC common mode voltage should not exceed the following values:

Input	Common Mode Maximum	Max Transient Peak Voltage
11.8V L-L	60V Peak	150V
26 V L-L	60V Peak	150V
90 V L-L	182V Peak	500V
Reference	210V Peak	1000V

90V line-to-line systems may have voltage transients which exceed the 500V specification listed above. These transients can destroy the thin film input resistor network in the hybrid. Therefore, 90V L-L solid state input modules may be protected by installing voltage suppressors as shown. Voltage transients are likely to occur whenever synchro or resolver voltages are switched on or off. For instance, a 1000V transient can be generated when the primary of a CX or TX driving a synchro or resolver input is opened.



CR1, CR2 and CR3 are SA85C, 100V bi-polarity transient voltage suppressors or equivalent.



CR 4 and CR5 are 1N6137, 200V bi-polarity transient voltage suppressors or equivalent.

CONNECTIONS FOR VOLTAGE TRANSIENT SUPPRESSORS

Non-standard synchro and resolver voltage levels can be accommodated with no degradation in the specifications. A unit should be selected whose voltage level 11.8V, 26V, or 90V is the next higher standard level above that of the non-standard signal. To correct the error gradient, a resistor R of the following value in ohms must be added between pins Ge and V:

$$R = \frac{1000}{A\text{-}1} \text{ where } A = \frac{\text{Standard Signal Voltage}}{\text{Non-Standard Signal Voltage}}$$

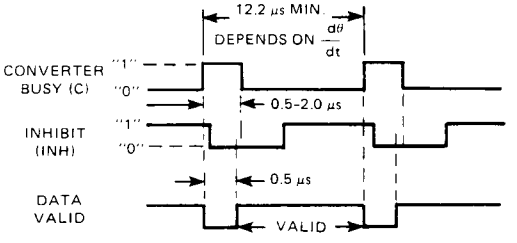
VOLTAGE FOLLOWER BUFFER INPUT

Voltage follower buffer units require a signal isolation transformer or a similar signal conditioner that provides a 1.0V rms nominal resolver type signal referenced to the internal converter ground V. This input option may be preferred in applications where the signal conditioner can be integrated with other components, as in many multiplexed systems.

LOGIC OUTPUTS AND INPUTS

CAUTION:	Appropriate handling procedures should be used to prevent damages to CMOS circuits.

Logic outputs consist of 16 parallel data bits and a Converter Busy (CB). All logic outputs are short-circuit proof to ground and to positive voltages as high as V_L. The CB output is a positive 0.5–2.0 μs pulse, and data changes about 0.2 μs after the leading edge of the pulse because of an internal delay (see Figure 1). Data is valid 0.5 μs after the leading edge of a CB.



TIMING DIAGRAM

The parallel digital outputs are gated to provide two 8 line bytes for microprocessor bus interfacing. When the Enables for the gates are at logic 0, the gate outputs are at normal logic 1 or 0, depending on the bit state. When the Enables are at logic 1, the gate outputs are high impedance and the microprocessor sees an essentially open line. Outputs are valid 0.5 μs after an Enable is driven to logic 0. For 16 bit parallel output operation when the 3-state feature is not used, the Enable lines should be tied to logic 0.

The inhibit (INH) logic input locks the 16 bit transparent latch so that the bits will remain stable while data is being transferred (see Figure 1). The output is stable 0.5 μs after the Inhibit is driven to logic 0. A logic 0 at the T input locks the 16 bit latch, and a logic 1 allows the bits to change. The purpose of the INH transparent latch is to prevent the transmission of invalid data when there is an overlap between the CB and INH. While the counter is not being updated the CB is at logic 0 and the INH latch is transparent. When the CB goes to logic 1 the INH latch is locked. If a CB occurs after an INH has been applied, the 16 bit latch will remain locked and its data cannot change until the CB returns to logic 0. If an INH is applied during a CB pulse, the 16 bit latch will remain locked and its data cannot change until the CB returns to logic 0. If an INH is applied during a CB pulse, the 16 bit latch will not lock until the CB pulse is over. The purpose of the 0.2 μs delay is to prevent a race condition between the CB and the INH in which the up-down counter begins to change just as an INH is applied.

TIMING

Whenever an input angle change occurs, the converter changes the digital angle in 1 LSB steps, and generates a converter busy pulse. The output data change is initiated by the leading edge of the CB pulse, delayed by the 0.2 μs (nominal) delay. The output becomes stable in less than 0.5 μs even though the CB pulse may last longer. Inhibit commands do not affect the updating of the converter no matter how long they are applied. A simple method of interfacing to a computer is to (a) apply the Inhibit, (b) wait 0.5 μs, (c) transfer the data, and (d) release the Inhibit.

ANALOG OUTPUTS

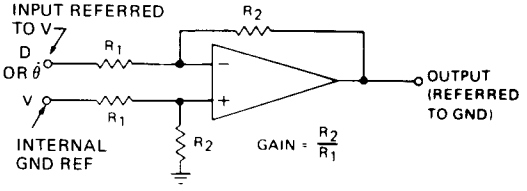
The analog outputs are V, D and $\dot{\theta}$. V is an internal analog ground, +7 VDC nominal. The outputs D, and θ ride on the ground reference voltage V, and should be measured with respect to V. Outputs can swing ±5V when the voltage level of the +15V power supply is +15V. The output swing changes proportionally if the level is not at +15V.

Output D is the unfiltered DC error voltage sin $(\theta - \Phi)$ near the null point. Its average amplitude at nominal input voltage for +1 LSB of error (equivalent to $(\theta - \Phi) = 0.022^\circ$) is −14.5 mV average.

$\dot{\theta}$ is a DC voltage proportional to the angular velocity $d\theta/dt = d\Phi/dt$. A +1 VDC output corresponds to +0.26 rps for 400 Hz units, and +0.068 rps for 60 Hz units.

Maximum loading for each analog output is 0.5 mA. Outputs D and $\dot{\theta}$ are not required for normal operation of the converter; V is used as reference ground with the voltage follower buffer option.

The figure shows a difference circuit which may be used to reference the analog outputs with respect to normal ground instead of the internal reference ground V.



DIFFERENCE CIRCUIT FOR ANALOG OUTPUTS

The outputs D and $\dot{\theta}$ are not closely controlled or characterized. Consult factory for further information.

USE AS A CT

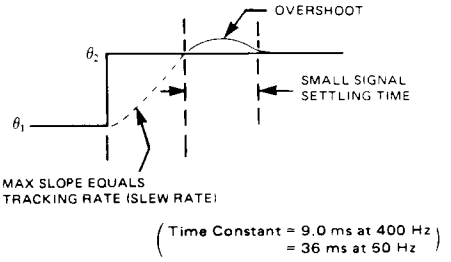
The new SDC-14520 Series S/D's can be used as solid state control transformers (CT). The procedure to accomplish this function is to disable the up-down counter by setting pin 30 ($\overline{S}$) to logic "0" and use the digital output lines, which are bidirectional, (pins 5 through 18, 21 and 22) as digital inputs. By operating the unit as described the error output is scaled to −14.5 mV avg/LSB of error and appears on pin 27 as full wave, demodulated, unfiltered D.C.

If an AC error output is desired, connect RH (pin 19) to + 15V power supply (pin 32 and RL (pin 20) to GND (pin 29). The resulting AC error output with a scaling of 16 mV rms/LSB of error is available on pin 27. The dynamic range of the SDC-14520 Series, error output is ±200 LSB, min.

DYNAMIC PERFORMANCE

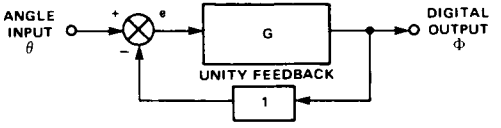
A type II servo loop ($K_V = \infty$) and very high acceleration constants give the SDC-14520 Series superior dynamic performance, as listed in the specifications.

If a step input occurs, as is likely when the power is initially turned on, the response will be critically damped. The response to a step input is shown below. After initial slewing at the maximum tracking rate of the converter, there is one overshoot which is inherent to a Type II servo. The overshoot settling to final value is a function of the small signal settling time.



RESPONSE TO A STEP INPUT

The loop dynamics of the tracking converter is shown in the diagram. The closed transient response is nominally critically damped. All loop dynamics can be determined from the diagram and formulas listed.



For 60 Hz

$$G = \frac{28^2\left(\frac{S}{13}+1\right)}{S^2\left(\frac{S}{130}+1\right)\left(\frac{S}{260}+1\right)}$$

For 400 Hz

$$G = \frac{110^2\left(\frac{S}{50}+1\right)}{S^2\left(\frac{S}{500}+1\right)\left(\frac{S}{1000}+1\right)}$$

CONVERTER LOOP DYNAMICS

RELIABILITY

MTBF values are very high because the use of custom monolithics greatly decreases the number of active components, because thin film resistor networks are used, and because of careful thermal design. Summaries of MTBF calculations are available on request.

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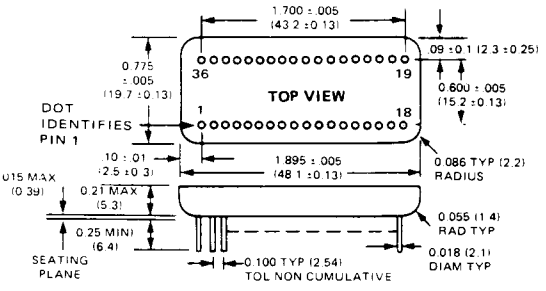
ORDERING INFORMATION

SDC-1452X – X X X

- Accuracy:
  - 3 = ±5.3′
  - 4 = ±2.6′
  - 5 = ±1.3′
- Reliability Grade
  - 0 = Standard DDC procedures
  - 1 = Fully compliant with MIL-STD 883
  - 2 = Screened to MIL-STD-883 but without QCI testing
- Temperature (operating):
  - 1 = −55°C to +125°C
  - 3 = 0°C to +70°C
- Input:
  - 0 = 11.8V, 400 Hz, Synchro
  - 1 = 90V, 400 Hz, Synchro
  - 2 = 90V, 60 Hz, Synchro
  - 4 = 26V, 400Hz, Resolver
  - 5 = 11.8V, 400 Hz, Resolver
  - 6 = 90V, 400 Hz, Resolver
  - 7 = 1V, 400 Hz, Resolver (Direct)
  - 8 = 1V, 60 Hz, Resolver (Direct)
- Family Code
- Input Type:
  - SDC = Synchro
  - RDC = Resolver
  - XDC = Direct Input (1V)

MECHANICAL OUTLINE
36 PIN DOUBLE DIP



NOTES

1. Dimensions shown are in inches. (millimeters)
2. Lead identification numbers are for reference only.
3. Lead cluster shall be centered within ±0.10 of outline dimensions. Lead spacing dimensions apply only at seating plane.
4. Pin material meets solderability requirements of MIL-STD-202E, Method 208C.
5. Package is Kovar with electroless nickel plating.
6. Case is electrically floating.

D

PIN CONNECTION TABLE

PIN	FUNCTION		
	Solid St. Resolver	Solid St. Synchro	Volt. Fol. Buffer
1	S1	S1	NC
2	S2	S2	COS
3	S3	S3	SIN
4	S4	NC	NC
5	Bit 1 MSB		
6	Bit 2		
7	Bit 3		
8	Bit 4		
9	Bit 5		
10	Bit 6		
11	Bit 7		
12	Bit 8		
13	Bit 9		
14	Bit 10		
15	Bit 11		
16	Bit 12		
17	Bit 13		
18	Bit 14		
19	RH (Ref High)		
20	RL (Ref Low)		
21	Bit 15		
22	Bit 16 LSB		
23	$\dot{\theta}$ (Analog Velocity Out)		
24	CB (Converter Busy)		
25	$\overline{\text{EN LSB}}$ (Enable, Bits 9 to 16)		
26	$\overline{\text{EN MSB}}$ (Enable, Bits 1 to 8)		
27	D (Unfiltered DC Error Out)		
28	V_L (Logic Voltage Input)		
29	GND		
30	$\overline{S}$		
31	Ge (Gain Control)		
32	+15V (Power Supply In)		
33	INH (Inhibit)		
34	V (Internal Analog GND)		
35	BC (Buffered Cos)		
36	BS (Buffered Sin)		

NOTES:
BS and BC pins are used in other applications