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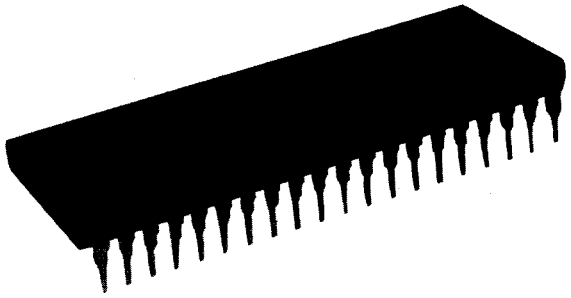
LS7240 | 6 DECADE, 7 LEVEL COMPARATOR WITH MEMORY

Revised January 1986

FEATURES:

- Direct Interface with CMOS CD4510 Presettable Up/Down Counter
- Direct Interface with LS7040 Dual 3 Decade Counter
- Multiplexed BCD/HEX Data I/O
- DC to 60KHz Scan Frequency at 5V
- Cascadable
- 7 Levels of 24 Bit Comparators
- Thumbwheel Switch Interface for 7 Level Storage Data
- CMOS Type Noise Immunity
- Single Power Supply Operation +4.75 to +15 Volts
- CMOS Compatibility
- Power-On-Reset
- All Inputs Protected
- High Input Impedance
- Low Power Dissipation



DESCRIPTION:

The LS7240 is a monolithic, ion implanted MOS 7-Level 6 digit (BCD or HEX) memory/comparator. It includes seven 6 decade comparators and memory, a comparator output, a 4 bit data I/O Bus, 7 synchronizing strobes for thumbwheel and display drive and 24 parallel data input lines. Data written in each of the 7 levels of memory is compared with the data placed in the 24 bit parallel inputs and the result is indicated by the Multiplexed comparator output. The 4 bit I/O serves as either the inputs for writing into any of the 7 memories or outputs for displaying either the 24 bit parallel data or any one of the memories.

DESCRIPTION OF OPERATION:

SCAN OSCILLATOR AND DIGIT SELECT STROBES:

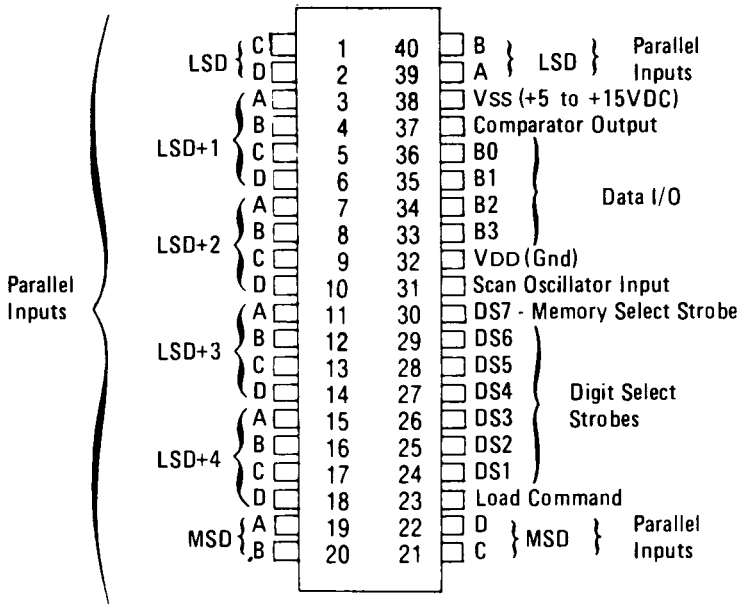
The SELECT STROBE GENERATOR is driven by an internal oscillator whose frequency is determined by an external RC network (as shown in Fig. 4). Table I indicates several frequencies and their associated resistor-capacitor networks.

The SELECT STROBES scan from DS1 to DS7. DS7 selects the particular comparator memory to be selected and DS1 through DS6 selects the LSD to MSD digit to be loaded. Maximum scan frequency is 60KHz at 5V, 40KHz at 10V and 20KHz at 15V. All I/O timings are synchronized by the DS strobes as explained in each I/O section.

PARALLEL INPUT DATA AND COMPARATOR OUTPUT:

BCD data applied from the counter to the 24 bit parallel inputs is compared with the 7-level memory. All 24 bits of each memory are compared in parallel and 7 internal comparisons are performed. These comparisons result in a logical "1" if the memory level and input data are equal or a logical "0" if not equal. The internal comparisons are multiplexed with the strobe outputs, i.e. MEMORY 1 is muxed with DS1,

LS7240 CONNECTION DIAGRAM:



TOP VIEW

FIGURE 1

MEMORY 2 is muxed with DS2, etc. (See Figure 4). A single output comparator line is demuxed externally. The positive edges of the DIGIT STROBES are used to strobe the comparator output line into their respective latches as shown in figures 2 and 5. The positive edge of DS1 is used to demux comparator 1 from the common comparator output, positive edge of DS2 demuxes comparator 2 etc.
The data provided by the counter is BCD data. However, HEX data, binary data or any other format of data may also be used as inputs. All that would be required is that the internal memory is correspondingly loaded.

DATA I/O AND LOAD COMMAND

The 4 bit data I/O acts as inputs when the DS strobes are active (high) and as outputs in between strobes. The in between strobe time is typically 5 μs. In the input mode, the data applied selects the memory to be addressed as well as the 6 digit number to be loaded. Figure 5 indicates how a set of 7 thumbwheel switches is used to load the memory. The LS7240 has internal pull down resistors on its I/O lines. Data applied during DS7 serves as the memory address, while data applied during the succeeding DS1 through DS6 loads LSD through MSD respectively into the selected memory. Data is loaded into the memory at the trailing edges of the DS strobes. In between strobes, when the I/O bus is in the output mode, the selected 6 digit memory is multiplexed out. The MSD is applied to the output during the DS1 and DS2 inter-strobe delay. The LSD+4 output occurs between DS2 and DS3, LSD+3 between DS3 and DS4, LSD+2 between DS4 and DS5, LSD+1 between DS5 and DS6, and LSD between DS6 and DS7.
The load command output can be used as a strobe for storing the output data into external latches for display or control functions.
A number of LOAD/DISPLAY combinations for data I/O is possible as explained in Table II. The data in this truth table refers to the input data applied to the I/O bus during active DS7.

The display is shown in figure 5. The LOAD COMMAND is used to load the BCD DATA into a CD4511 or equivalent. The DIGIT SELECT STROBES are used to enable the LED's as shown. DS2 is used to display the MSD, DS3 displays LSD+4, DS4 displays LSD+3, DS5 displays LSD+2, DS6 displays LSD+1 and DS7 displays LSD.
The LS7240 is equipped with an ANTI-BOUNCE feature. Input data must be stable at the input to the I/O bus for a minimum of 700 scan cycles before it can be loaded into the memory. Typical Anti-Bounce times as a function of scan frequency is indicated in Table III. Similarly, removal of data must be stable for 700 clock cycles before it is recognized as a complete removal.

POWER-ON-RESET:

An internal POWER-ON-RESET is provided to reset all memories to "0" and sets DS7 (Pin 30) to logic "1" upon application of power.

POWER SUPPLIES:

The circuit will operate over the range of +4.75 to +15 volts.

TABLE I

Voltage	Resistor	Capacitor	Typical Frequency
	220KΩ	50pf	60KHz
5V	680KΩ	50pf	30KHz
	1.5MΩ	50pf	15KHz
	470KΩ	50pf	40KHz
10V	1MΩ	50pf	20KHz
	2MΩ	50pf	10KHz
	1MΩ	50pf	20KHz
15V	2MΩ	50pf	10KHz
	4.7MΩ	50pf	5KHz

TABLE II

Truth Table for Load/Display Combination

B3	B2	B1	B0	
0	0	0	1	Display Memory 1
0	0	1	0	Display Memory 2
0	0	1	1	Display Memory 3
0	1	0	0	Display Memory 4
0	1	0	1	Display Memory 5
0	1	1	0	Display Memory 6
0	1	1	1	Display Memory 7
1	0	0	1	Load & Display Memory 1
1	0	1	0	Load & Display Memory 2
1	0	1	1	Load & Dispaly Memory 3
1	1	0	0	Load & Display Memory 4
1	1	0	1	Load & Display Memory 5
1	1	1	0	Load & Display Memory 6
1	1	1	1	Load & Display Memory 7
0	0	0	0	Displays 24 Bit Input Data
1	0	0	0	Resets All Memories and Displays Memory 1.

TABLE III

Scan Frequency (KHz)	Anti-Bounce (milliseconds)
60	12
40	17.5
20	35

TECHNICAL DATA:

INPUTS/OUTPUTS – All inputs and outputs are CMOS compatible over entire range of power supply voltage limits.
LOGIC – Positive True.
PACKAGE – 40 Pin Dual-In-Line plastic.

MAXIMUM R

Parameter

DC Supply Vol
Operating Tem
Storage Tempe

All inputs con
charges. Care s
outside the spe

DC ELECTR

(V_{DD}=0V, V_{SS}

OUTPUT SPEC

SOURCE CUR

$V_{OH}=V_{SS}-.5$V

$V_{OH}=V_{SS}-1$V

$V_{OH}=V_{SS}-2$V

SINK CURREN

$V_{OL}=V_{DD}+.4$V

L

SOURCE CUR

$V_{OH}=V_{SS}-.5$V

$V_{OH}=V_{SS}-1$V

$V_{OH}=V_{SS}-2$

SINK CURREN

$V_{OL}=V_{DD}+.4$

BCD I/O

SOURCE CURI
$V_{OH}=V_{SS}-.5$V

$V_{OH}=V_{SS}-1$V

$V_{OH}=V_{SS}-2$V

S: (Voltages referenced to V_{DD})

	Symbol	Value	Units
e	V_{SS}	+4.75 to +15	Vdc
Range	T_A	−25 to +70	°C
nge	T_S, T_G	−65 to +150	°C

ection circuitry to prevent damage due to high static exercised to prevent unnecessary application of Voltage ge.

IARACTERISTICS:

:o +15V, −25°C≤ T_A ≤+70°C unless otherwise specified).

INS:

DIGIT SELECT STROBES

H	V_{SS}	Min.	Typ.	Max.	Units
	5Vdc	0.4	1.0	–	mA
	10Vdc	1.0	1.6	–	
	15Vdc	1.2	2.0	–	
	5Vdc	1.4	2.0	–	mA
	10Vdc	2.7	4.0	–	
	15Vdc	3.5	5.0	–	
	5Vdc	2.3	3.0	–	mA
	10Vdc	6.0	9.0	–	
	15Vdc	7.4	9.6	–	
	5Vdc	16.0	27.0	–	μA
	10Vdc	13.0	19.0	–	
	15Vdc	9.0	15.0	–	

MMAND AND COMPARATOR OUTPUT

H	V_{SS}	Min	Typ.	Max.	Units
	5Vdc	0.1	0.3	–	mA
	10Vdc	0.3	0.6	–	
	15Vdc	0.5	1.0	–	
	5Vdc	0.2	0.4	–	mA
	10Vdc	1.0	1.5	–	
	15Vdc	1.5	2.5	–	
	5Vdc	0.5	0.9	–	mA
	10Vdc	2.2	3.2	–	
	15Vdc	3.4	5.0	–	
	5Vdc	19.0	30.0	–	μA
	10Vdc	16.0	23.0	–	
	15Vdc	13.0	17.0		

H	V_{SS}	Min.	Typ.	Max.	Units
	5Vdc	0.1	0.3	–	mA
	10Vdc	0.3	0.6	–	
	15Vdc	0.5	1.0	–	
	5Vdc	0.5	0.9	–	mA
	10Vdc	1.0	1.5	–	
	15Vdc	1.5	2.5	–	
	5Vdc	0.5	0.9	–	mA
	10Vdc	2.2	3.2	–	
	15Vdc	3.0	5.0	–	

SINK CURRENT, I_{OL}	V_{SS}	Min.	Typ.	Max.	Units
	5Vdc	7.0	10.0	–	μA
V_{OL}=V_{DD}+.4V	10Vdc	5.0	7.0	–	
	15Vdc	3.0	5.0	–	

QUIESCENT SUPPLY CURRENT

(All Inputs Pins Tied to V_{SS}) (All Output Pins Left Open)

Symbol	V_{SS}	Max.	Units
I_{DD}	5V	12.0	mA
	10V	15.0	
	15V	18.0	

INPUT VOLTAGE SPECIFICATIONS: (All Inputs Except Scan)

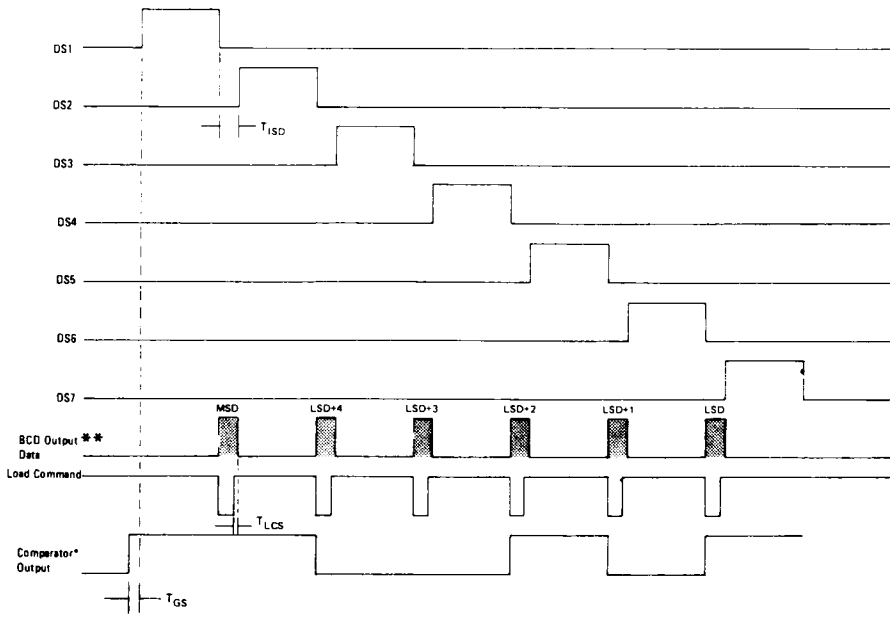
Parameter	Symbol	V_{SS}	Min.	Max.	Units
Input Voltage "0" Level	V_{IL}	5Vdc	0	1.5	Vdc
		10Vdc	0	3.0	
		15Vdc	0	4.5	
Input Voltage "1" Level	V_{IH}	5Vdc	3.5	V_{SS}	Vdc
		10Vdc	7.0	V_{SS}	
		15Vdc	10.5	V_{SS}	

DYNAMIC ELECTRICAL CHARACTERISTICS:

(V_{DD}=0, V_{SS}= +4.75 to +15V, −25°C≤ T_A ≤+70°C unless otherwise specified).

Parameter	Symbol	Min.	Max.	Units
Scan Input Frequency				
V_{SS}=5V	f_{SC}	–	60.0	KHz
V_{SS}=10V	f_{SC}	–	40.0	KHz
V_{SS}=15V	f_{SC}	–	20.0	KHz
Inter-strobe delay	t_{ISD} †	1.5	12.0	μs
Load Command Set-Up Time	t_{LCS} †	0.2	2.5	μs
Comparator Output Set-Up Time	t_{CS} †	1.5	10.0	μs

†See Figure 2.



* 4 Comparisons are shown. In normal operation, usually only 1 comparison will occur at a time

**Shaded areas indicate valid output data.

FIGURE 2

BLOCK DIAGRAM OF PROGRAMMABLE COUNTER CONTROLLER

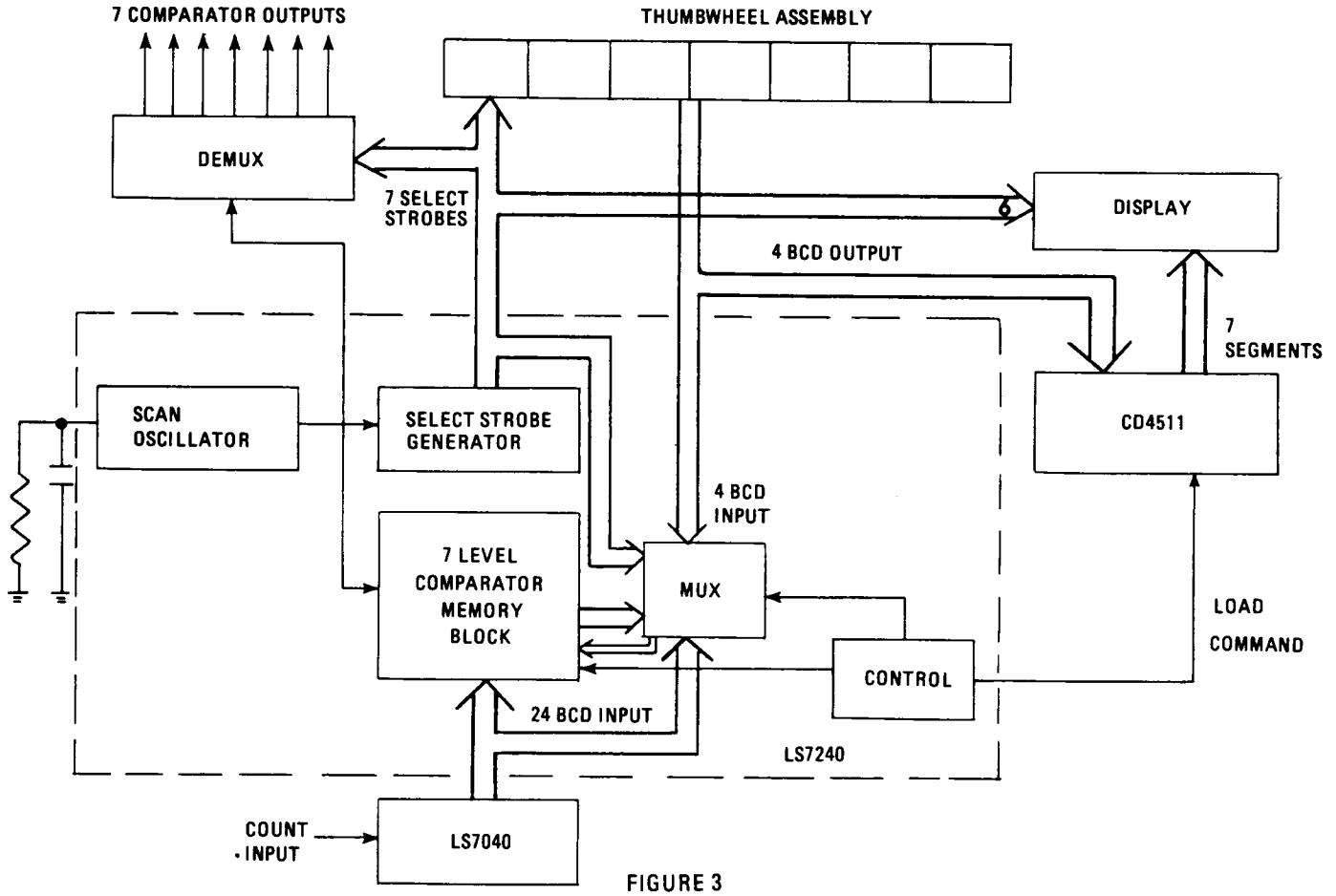
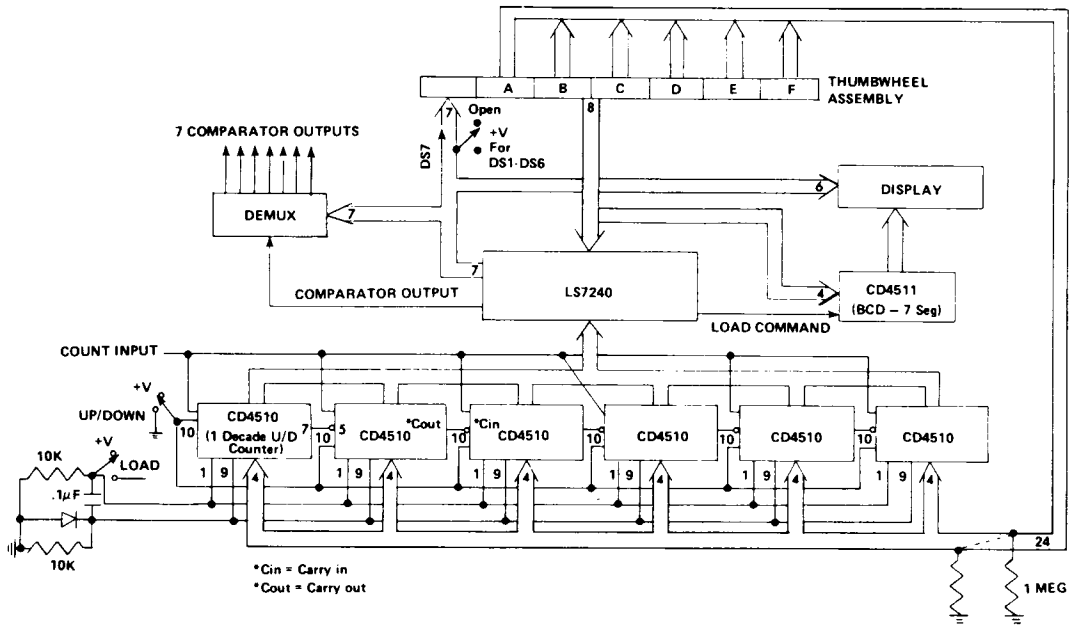


FIGURE 3

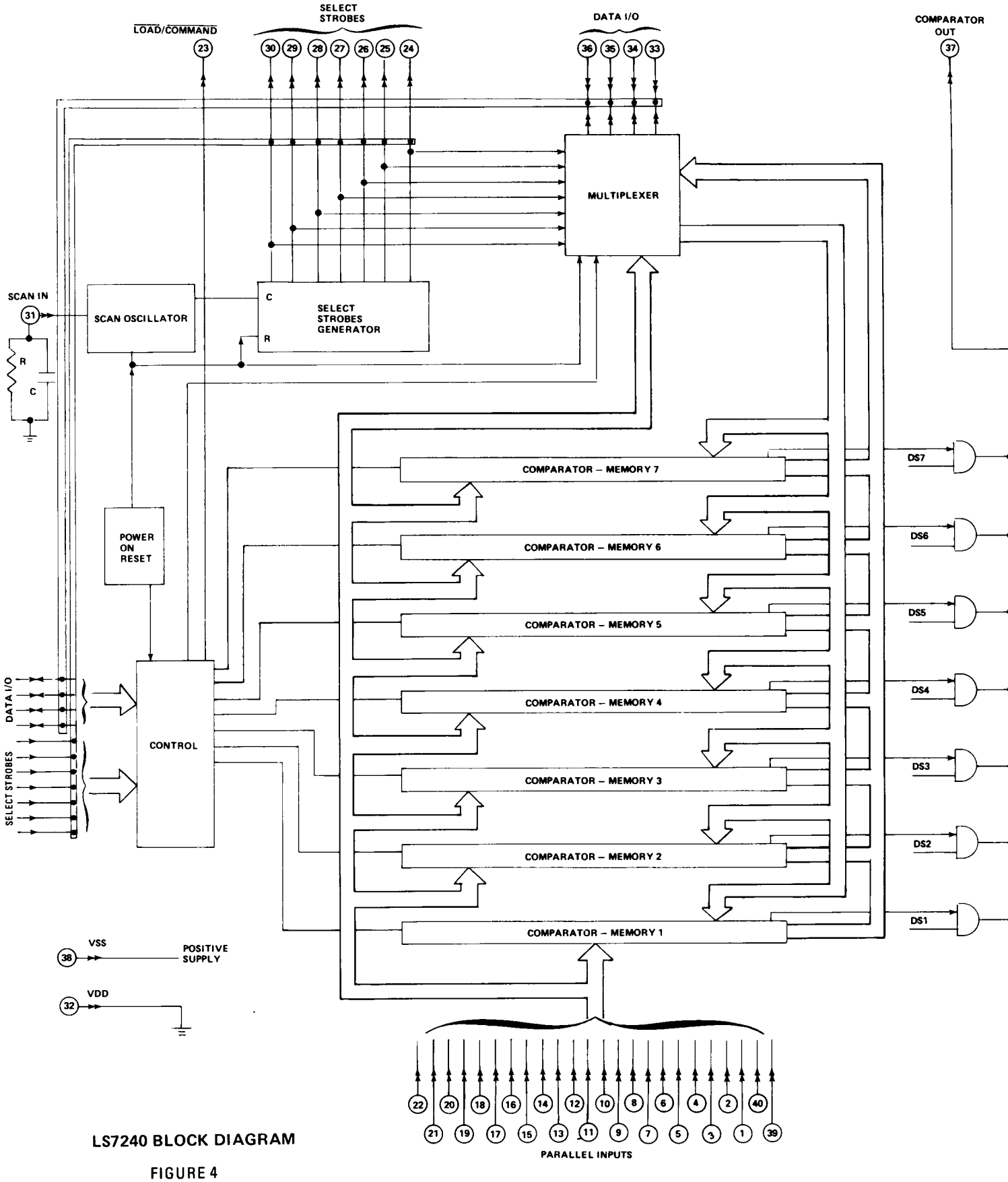
SYSTEM INTERCONNECTION USING PRESETTABLE UP/DOWN COUNTERS



The thumbwheel assembly is used to load the LS7240 as well as the synchronous six decade up/down counter. To preset the CD4510's, the inputs to the thumbwheels A.through F are connected to the positive supply and the BCD outputs are applied to their respective CD4510 inputs. External 1 Meg resistors are used at the thumbwheel outputs. The Load Command is used to reset and then preset the counter to the number selected.

FIGURE 5

FIGURE A



LS7240 BLOCK DIAGRAM

FIGURE 4

INTERCONNECT DIAGRAM OF TYPICAL COUNTER CONTROLLER

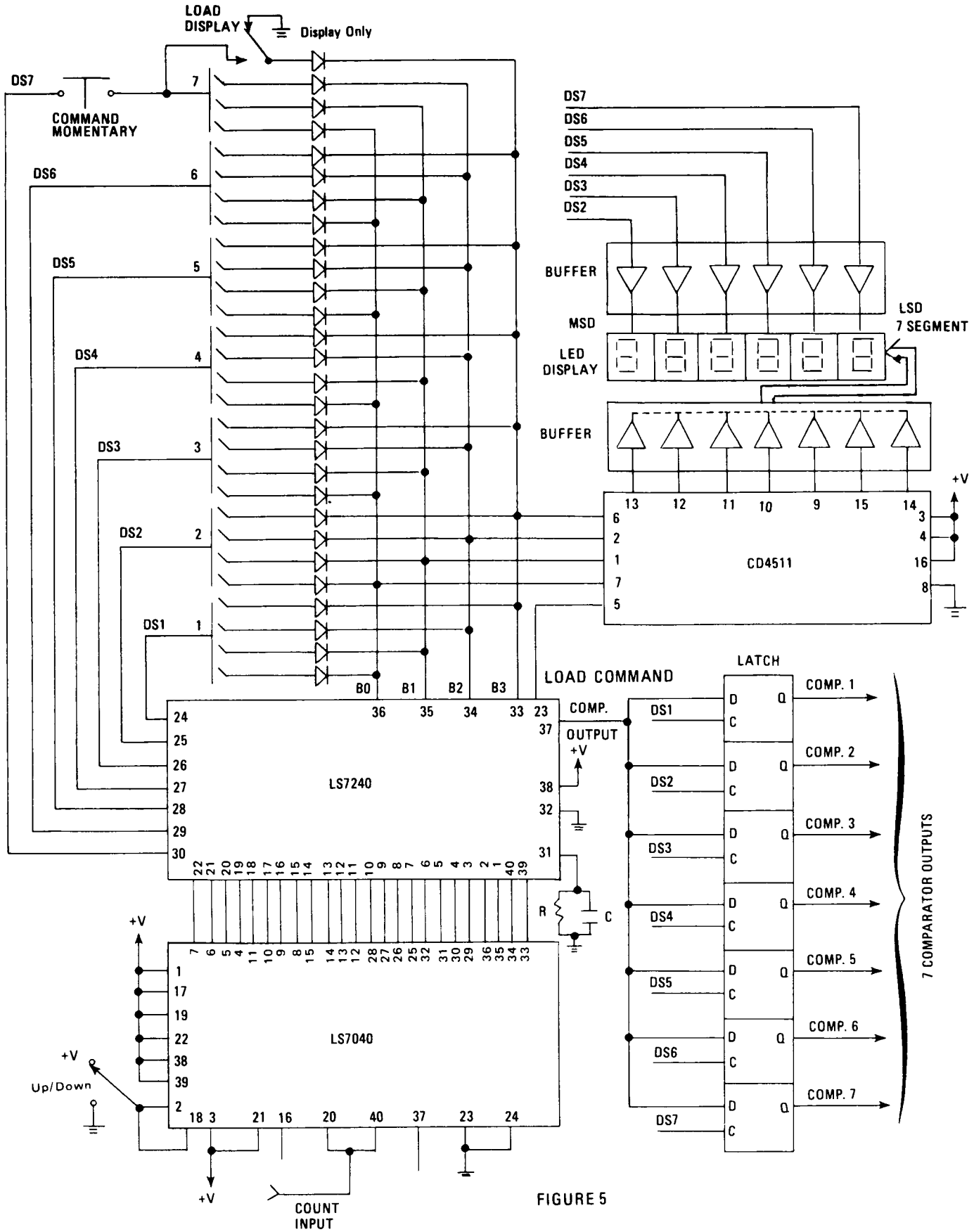


FIGURE 5

The System Interconnection of an LS7240 with an LS7040 and support circuitry is as shown. Thumbwheel 7 selects the memory. Thumbwheel 6 through 1 selects MSD through LSD. If the "Load and Display/Display Only" toggle switch is in the Load and Display position, the data is loaded into the LS7240, and displayed on the LED display when the "COMMAND MOMENTARY" is depressed. The BCD output data of the LS7240 is converted to 7 segment data by the CD4511. As long as the Momentary is held down, the display presents the data just loaded. If the Momentary is released, the display presents the BCD input data from the LS7040. If memory 0 is selected and the toggle switch is in the LOAD AND DISPLAY position, all memories are reset when the momentary is depressed. If the toggle switch is in the "Display Only" position then depressing the momentary will enable the 7 segment display to present what was previously loaded into the memory.