

**Description**

The Voltage Controlled Solidtron™ (VCS) features high peak current capability and a low on-state voltage drop common to SCR thyristors. Additionally it features extremely high turn-on di/dt capability and virtually no turn-on delay jitter making it ideally suited for a variety of capacitor discharge applications.

The 4-pin F-Pak SM package offers a rugged low inductance interface and allows for installation using automated handling equipment. The package consists of an epoxy filled 4 contact FR4 substrate.

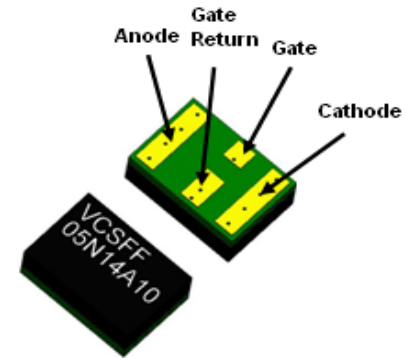
**Features**

- 1400V Peak Off-State Voltage
- 3.0kA Repetitive Peak Anode Current
- 120kA/uSec di/dt Capability
- 18nSec Turn-On Delay
- Low Loss
- MOS Gate Control

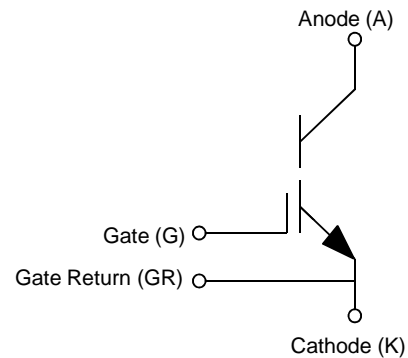
**Applications**

ESA / EFI

**F-Pak**



**Schematic Symbol**



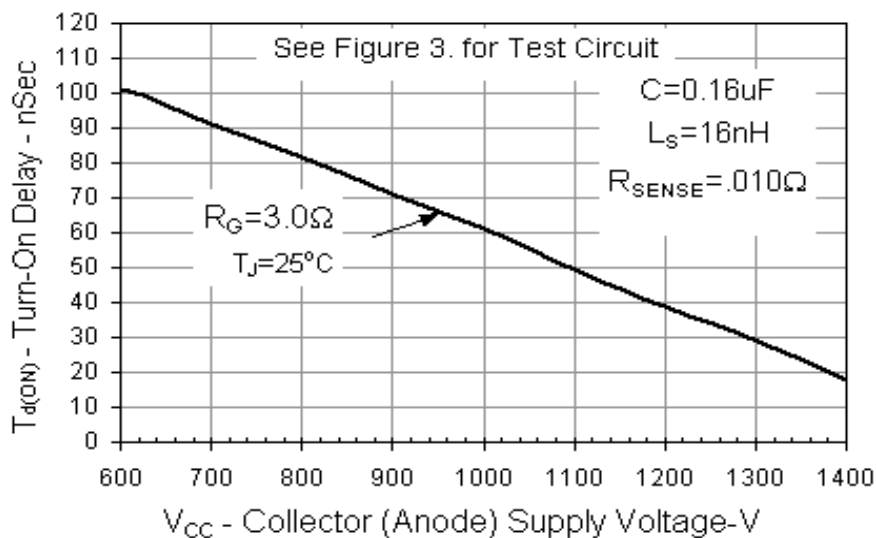
**Limiting Characteristics and Ratings**

	SYMBOL	VALUE	UNITS
Peak Off-State Voltage	$V_{DRM}$	1400	V
Peak Reverse Voltage	$V_{RRM}$	-30	V
Off-State Rate of Change of Voltage Immunity ( $V_D=1400V$ )	dv/dt	5000	V/uSec
Non-repetitive Peak Anode Current (Sinusoid Pulse Duration=250nSec)	$I_{ASM}$	4800	A
Repetitive Peak Anode Current (Sinusoid Pulse Duration=250nSec)	$I_{ASM}$	3000	A
Rate of Change of Current	di/dt	120	kA/uSec
Continuous Gate-Cathode Voltage	$V_{GKS}$	+/-20	V
Peak Gate-Cathode Voltage	$V_{GKM}$	+/-25	V
Minimum Gate-Cathode Voltage Required for Guaranteed Off-State	$V_{GK(OFF-MIN)}$	0	V
Maximum Junction Temperature	$T_{JM}$	125	°C
Maximum Soldering Temperature (Installation)		260	°C

**Performance Characteristics**

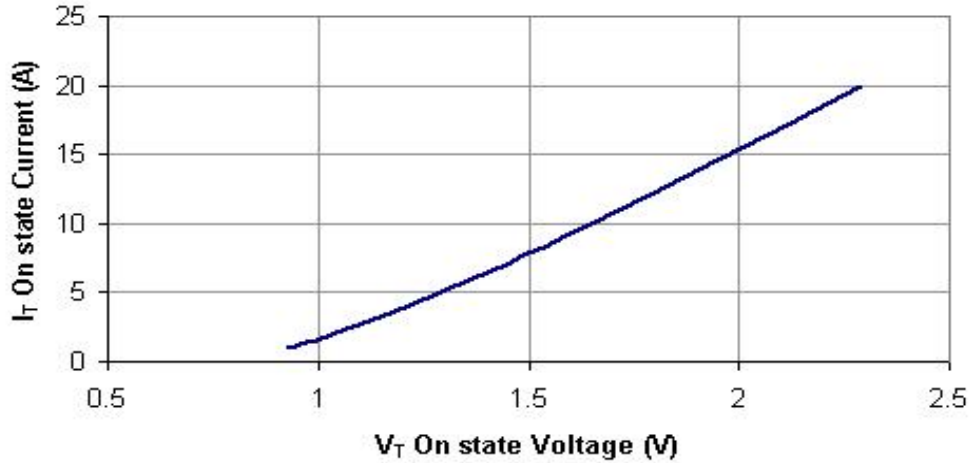
T <sub>J</sub> =25°C unless otherwise specified				Measurements			
Parameters	Symbol	Test Conditions		Min.	Typ.	Max.	Units
Anode to Cathode Breakdown Voltage	V <sub>(BR)</sub>	V <sub>GK</sub> =-5, I <sub>A</sub> =1mA		1400			V
Anode-Cathode Off-State Current	I <sub>D</sub>	V <sub>GE</sub> =-5V, V <sub>AK</sub> =1400V	T <sub>C</sub> =25°C			1	uA
			T <sub>C</sub> =50°C			3	uA
			T <sub>C</sub> =125°C			5	uA
Gate-Cathode Leakage Current	I <sub>GK(lkg)</sub>	V <sub>GK</sub> =+/-15V	T <sub>C</sub> =25°C		4	10	nA
			T <sub>C</sub> =50°C		4	10	nA
			T <sub>C</sub> =125°C		5	10	nA
Anode-Cathode On-State Voltage	V <sub>T</sub>	I <sub>T</sub> = 5A, V <sub>GK</sub> = 5V	T <sub>C</sub> =25°C		1.3		V
Gate-Cathode Turn-On Threshold Voltage	V <sub>GK(TH)</sub>	V <sub>AK</sub> =V <sub>GK</sub> , I <sub>AK</sub> =1mA			0.8		V
Input Capacitance	C <sub>ISS</sub>	Bias=6V, Freq.=120Hz			1.55		nF
Turn-on Delay Time	t <sub>D(ON)</sub>	0.16uF Capacitor Discharge			90		nS
Rate of Change of Current	di/dt	T <sub>J</sub> =25°C, V <sub>GK</sub> = -5V to +5V			26		kA/uSec
Peak Anode Current	I <sub>P</sub>	V <sub>AK</sub> =700V, R <sub>G</sub> =3.0Ω, L <sub>S</sub> =16nH			1660		A
Rate of Change of Current	di/dt	0.15uF Capacitor Discharge			120		kA/uSec
Peak Anode Current	I <sub>P</sub>	T <sub>J</sub> =25°C, V <sub>GK</sub> = -5V to +5V			6700		A
		V <sub>AK</sub> =1200V, R <sub>G</sub> =3.0Ω, L <sub>S</sub> =6nH					

**Typical Performance Curves** T<sub>J</sub>=25°C unless otherwise specified



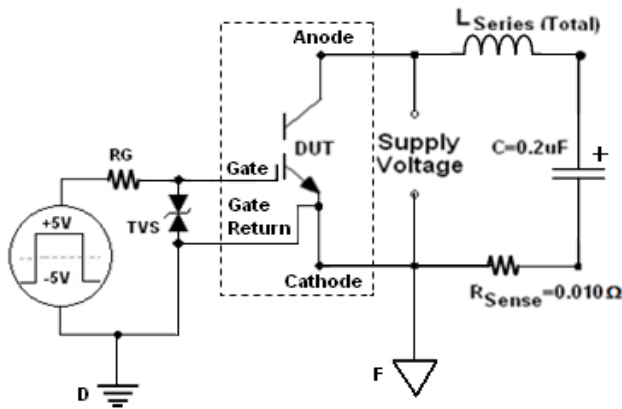
**Figure 1.** Turn-On Delay Characteristics  
 R<sub>G</sub>=3.0Ω, T<sub>J</sub>=25°C

**Typical Performance Curves (Continued)**



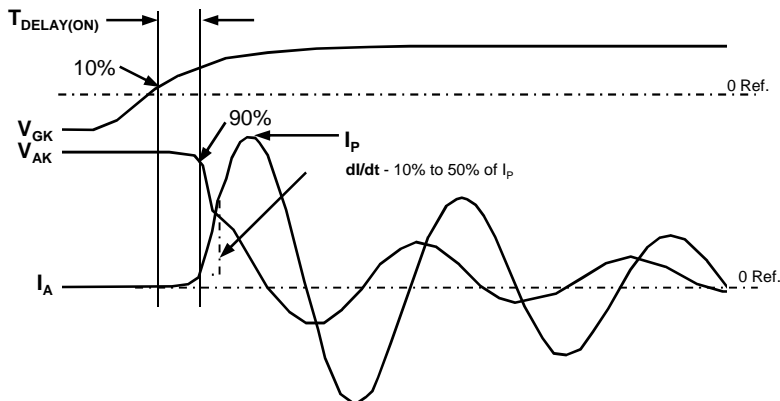
**Figure 2** On state characteristics

**Test Circuit and Waveforms**



**Figure 3.** 0.16uF Pulsed Discharge Circuit Schematic

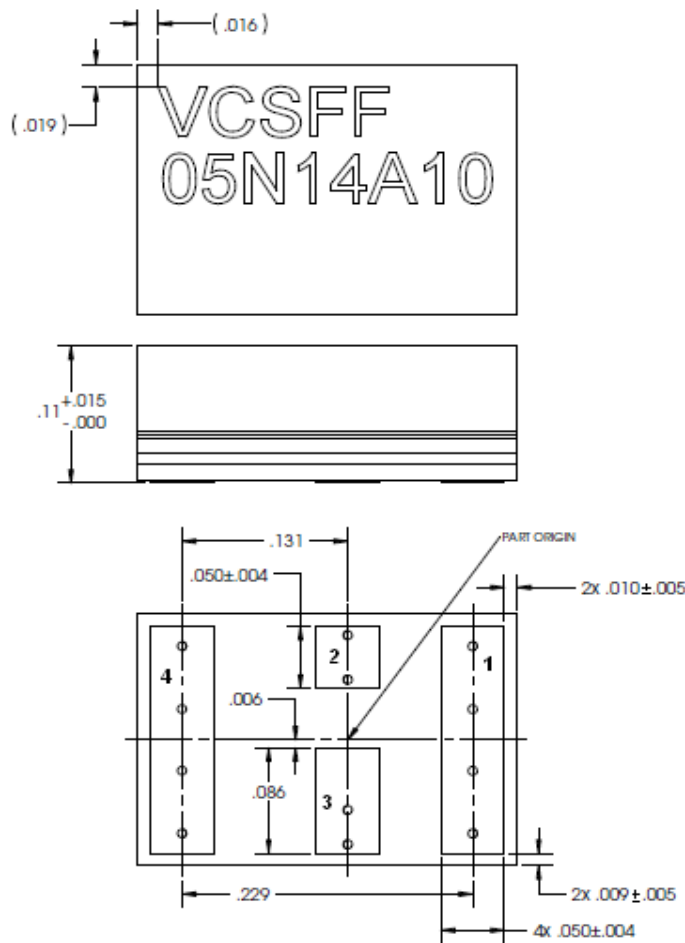
- $L_{SERIES(TOTAL)}$  is calculated using  $1 / (f 2\pi)^2 C$  where  $f$  = frequency of  $I_A$  (See Figure 4)
- $R_{SENSE}$  is a calibrated Current Viewing Resistor (CVR)
- TVS - Fairchild SMBJ9V0CA
- Gate driver circuit ground connected to GR (Gate Return) . Donot connect gate circuit ground to cathode external to the device.



- The waveform shown is representative of one produced using a very low inductance circuit (<10nH).
- $V_{GK}$  is held positive until  $I_A$  oscillations have ended ( $I_A=0$ ).

**Figure 4.** 0.16uF Pulsed Discharge Circuit Waveforms

**Package Dimensions**



- Pins
1. Cathode
  2. Gate
  3. Gate Return
  4. Anode

All Dimensions are in inches

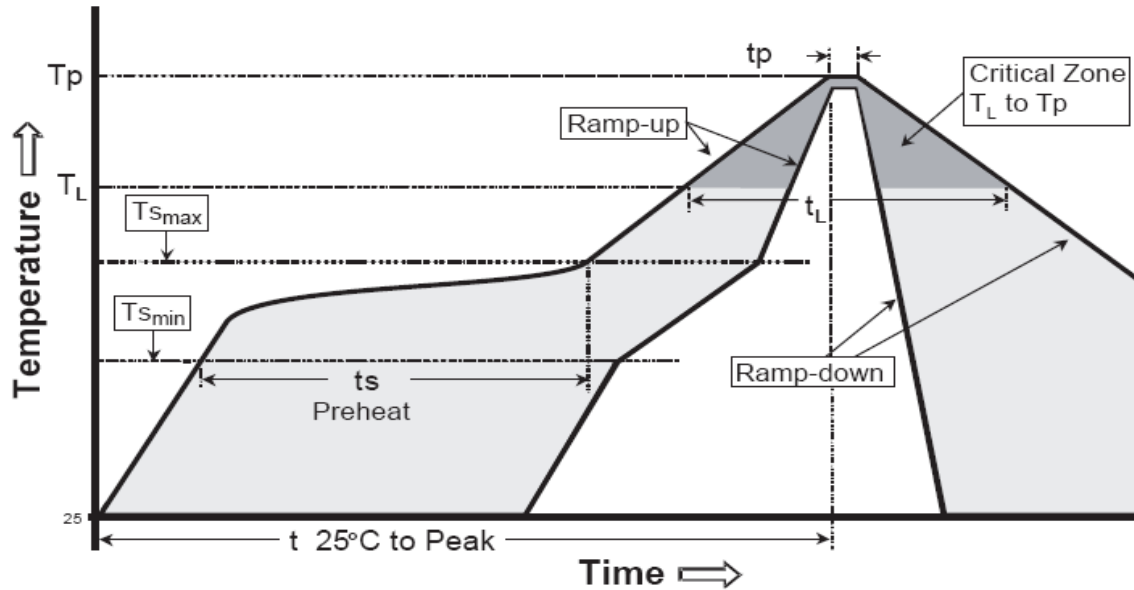
**Figure 5.** Critical Package Dimensions and Pin Assignment

**Application Note:**

**Use of Gate Return Bond Area.**

The MCT was designed for high di/dt applications. An independent cathode connection or "Gate Return Bond Area" was provided to minimize the effects of rapidly changing Anode-Cathode current on the Gate control voltage, ( $V=L*di/dt$ ). It is therefore, critical that the user utilize the Gate Return Bond Area as the point at which the gate driver reference (return) is attached to the VCS device.

**Recommended Reflow Profile:**



IPC-020c-5-1

	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Average Ramp-Up Rate (tsmax to tp)	3°C/second max.	3°C/second max.
Preheat		
Temperature Min (tsmin)	100°C	150°C
Temperature Max (tsmax)	150°C	200°C
Time (tsmin to tsmax)	60-120 seconds	60-180 seconds
Time maintained above:		
Temperature (tL)	183°C	217°C
Time (tL)	60-150 seconds	60-150 seconds
Peak/Classification Temperature (tp)	240 +0/-5°C	260 +0°C
Temperature (tp)	10-30 seconds	20-40 seconds
Ramp-Down Rate	6°C/second max.	6°C/second max.
Time 25°C to Peak Temperature	6 minutes max.	8 minutes max.

**General Handling Precautions**

1. Installation reflow temperature should not exceed 260°C or internal package degradation may result.
2. As with all MOS gated devices, proper handling procedures must be observed to prevent electrostatic discharge which may result in permanent damage to the gate of the device

'ATTENTION OBSERVE PRECAUTIONS FOR HANDLING ELECTROSTATIC DISCHARGE SENSITIVE DEVICES IN ALL ASSEMBLY AND TEST AREAS'





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**VCSFF05N14A10**

**Solidtron™**

N-MOS VCS, F-Pak  
Data Sheet (Rev 6 - 06/17/11)

**Revision History**

Rev	Date	EA #	Nature of Change
3	05-04-2009	04242009-NB-0005	Initial Issue
4	07-09-2010		
5	05-20-2011		Use of Gate Return Bond Area note added.
6	06-17-2011		Updated drawing