SLDS035 – D2984, JANUARY 1987 – REVISED NOVEMBER 1989

- **Each Device Drives 32 Lines**
- **–120-V PNP Open-Collector Parallel Outputs**
- **High-Speed Serially Shifted Data Inputs**
- **CMOS-Compatible Inputs**
- **Strobe and Sustain Inputs Provided**
- **Serial Data Output for Cascade Operation**

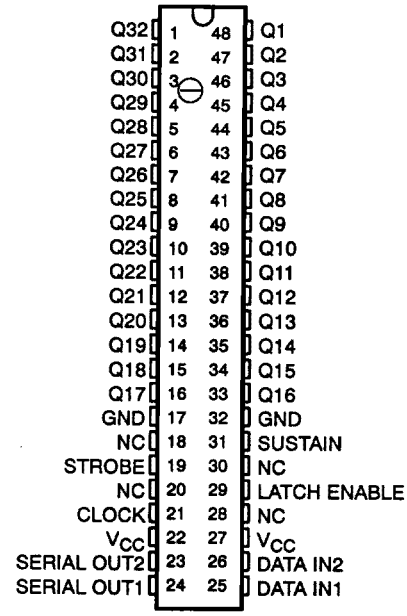
description

The SN751508 and SN751518 are monolithic integrated circuits designed to drive the data lines of a dc plasma panel display. The SN751518 pin sequence is reversed from the SN751508 for ease in printed-circuit-board layout.

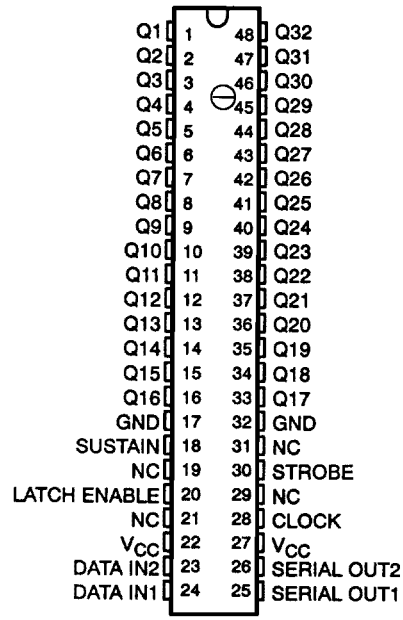
Each device consists of two 16-bit shift registers, 32 latches, 32 OR gates, and 32 pnp open-collector output AND gates. Typically, a 32-bit data string is split into two 16-bit data strings externally and then entered in parallel into the shift registers on the high-to-low transition of the clock signal. A high LATCH ENABLE transfers the data from the shift registers to the inputs of 32 OR gates through the latches. Data present in the latch during the high-to-low transition of LATCH ENABLE is stored. When STROBE is high, the latch is masked and a high is placed on the data input of the output AND gates. When STROBE is low and SUSTAIN is high, data from the latches is reflected at the outputs. When low, SUSTAIN forces all outputs to their off state. Drivers can be cascaded via the serial data outputs of the static shift registers. These outputs are not affected by LATCH ENABLE, STROBE, or SUSTAIN.

The SN751508 and the SN751518 are characterized from 0°C to 70°C.

SN751508 . . . FT PACKAGE
(TOP VIEW)

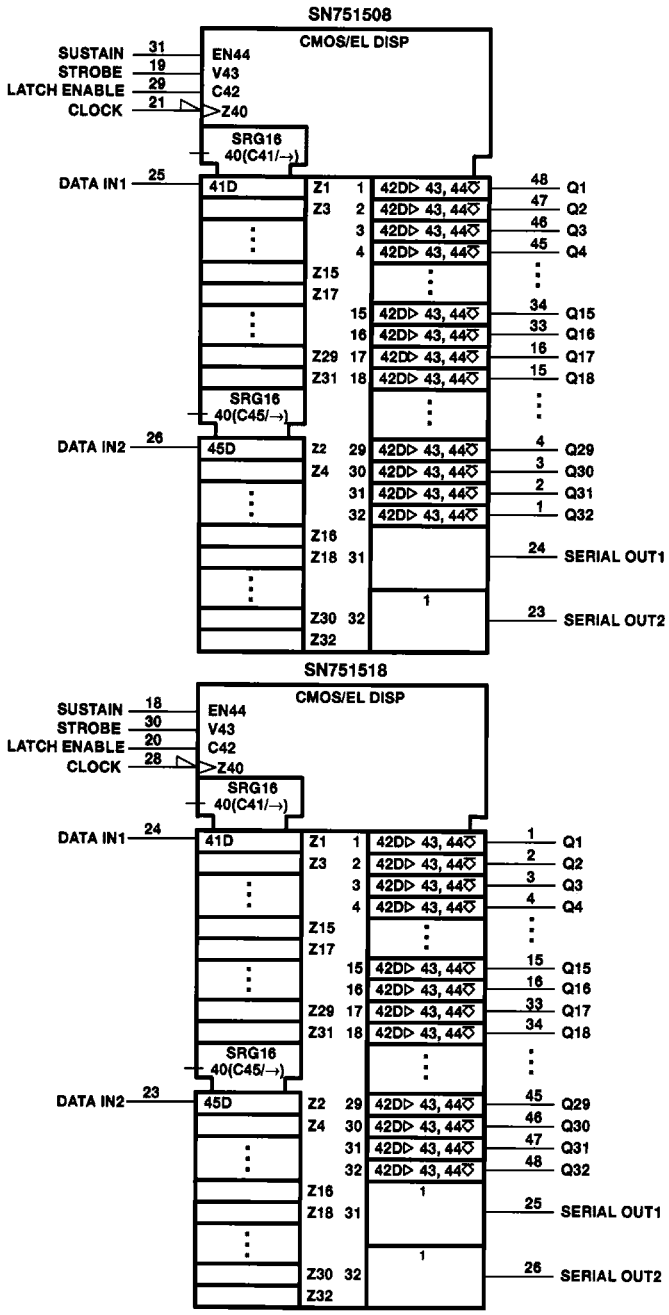


SN751518 . . . FT PACKAGE
(TOP VIEW)



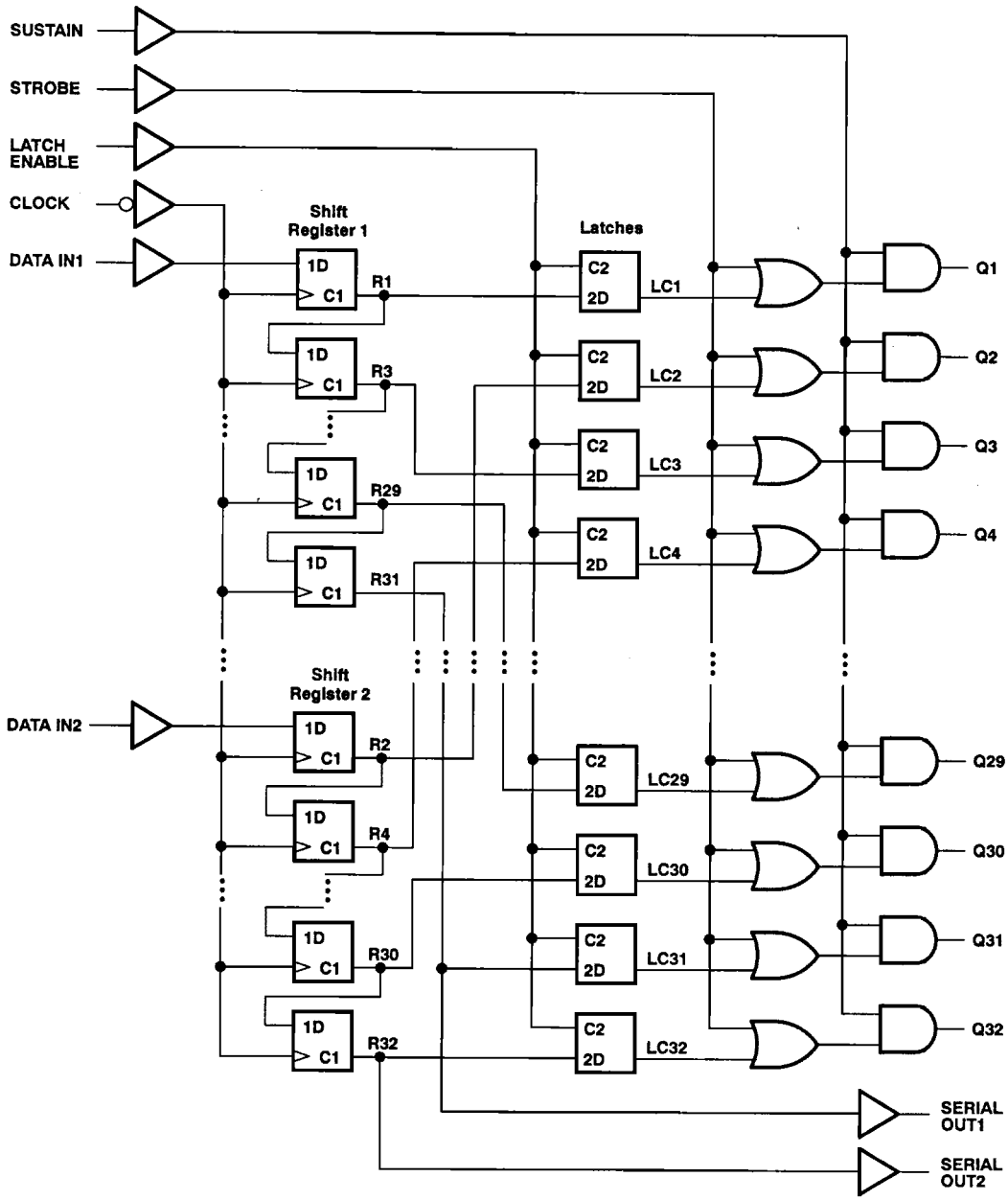
NC – No internal connection

logic symbols†



† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



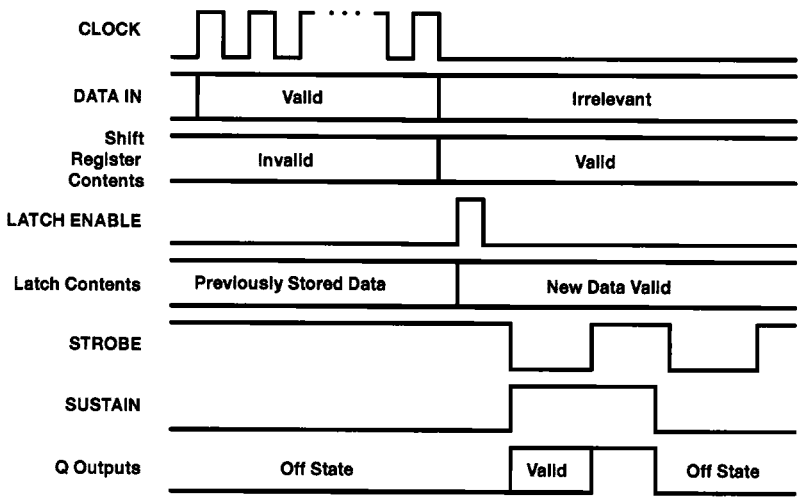
FUNCTION	CONTROL INPUTS				SHIFT REGISTERS R1 THRU R32	LATCHES LC1 THRU LC32	OUTPUTS		
	CLOCK	LATCH ENABLE	STROBE	SUSTAIN			SERIAL		Q1 THRU Q32
							S01	S02	
Load	↓ No ↓	X X	X X	X X	Load and shift† No change	Determined by LATCH ENABLE‡	R31	R32	Determined by SUSTAIN and STROBE
Latch Enable	X X	L H	X X	X X	As determined above	Stored data New data	R31	R32	Determined by SUSTAIN and STROBE
Strobe	X X	X X	L H	H H	As determined above	Determined by LATCH ENABLE‡	R31	R32	LC1 thru LC32 All on (high)
Sustain	X	X	X	L	As determined above	Determined by LATCH ENABLE‡	R31	R32	All off

H = high level, L = low level, X = irrelevant, ↓ = high-to-low transition

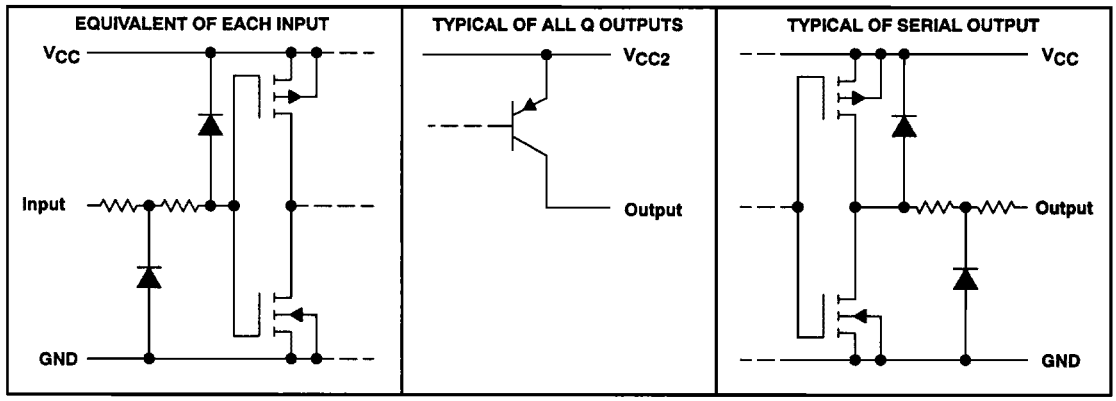
† Each even-numbered shift register stage takes on the state of the next-lower even-numbered stage, and likewise each odd-numbered shift register stage takes on the state of the next-lower odd-numbered stage; i.e., R32 takes on the state of R30, R30 takes on the state of R28, ... R4 takes on the state of R2, R2 takes on the state of DATA IN2, R31 takes on the state of R29, R29 takes on the state of R27, ... R3 takes on the state of R1, and R1 takes on the state on DATA IN1.

‡ New data enters the latches while LATCH ENABLE is high. This data is stored while LATCH ENABLE is low.

typical operating sequence



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V_{CC} (see Note 1) ..... −0.4 to 7 V
On-state Q output voltage range, V_O ..... −120 V to V_{CC} + 0.4 V
Input voltage range, V_I ..... −0.4 V to V_{CC} + 0.4 V
Serial output voltage range ..... −0.4 V to V_{CC} + 0.4 V
Continuous total power dissipation at (or below) 25°C free-air temperature (see Note 2) ..... 1025 mW
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

NOTES: 1. Voltages values are with respect to GND.
2. For operation above 25°C free-air temperature, derate linearly to 656 mW at 70°C at the rate of 8.2 mW/°C.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.5	5	5.5	V
Output voltage, V_O				−75	V
High-level input voltage, V_{IH}	V_{CC} = 4.5 V	3.6			V
	V_{CC} = 5.5 V	4.4			
Low-level input voltage, V_{IL}	V_{CC} = 4.5 V			0.9	V
	V_{CC} = 5.5 V			1	
Output current, I_O (T_A = 25°C)				−1.2	mA
Clock frequency, f_{clock}				5	MHz
Pulse duration, t_w (see Figure 1)	CLOCK	75			ns
	DATA IN	160			
	LATCH ENABLE	90			
	STROBE	2			µs
	SUSTAIN	2			
Setup time, t_{su} (see Figure 1)	DATA IN before CLOCK↓	20			ns
	CLOCK low before LATCH ENABLE↑	50			
	LATCH ENABLE low before CLOCK↓	0			
	LATCH ENABLE high before STROBE↓	0			
	LATCH ENABLE high before SUSTAIN↑	0			
Hold time, DATA IN after CLOCK↓, t_h (see Figure 1)		50			µs
Operating free-air temperature, T_A		0		70	°C

electrical characteristics over operating free-air temperature range, V_{CC} = 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	Q outputs	I_{OH} = −0.5 mA		4	4.5		V
		SERIAL OUT 1, 2	V_{CC} = 5.5 V	I_{OH} = −100 µA	4.3	4.6		
				I_{OH} = −20 µA	4.4			
			V_{CC} = 4.5 V	I_{OH} = −100 µA	3.4	3.6		
				I_{OH} = −20 µA	3.6			
V_{OL}	Low-level output voltage	SERIAL OUT 1, 2	V_{CC} = 5.5 V	I_{OL} = 100 µA		0.9	1.2	V
				I_{OL} = 20 µA			1.1	
			V_{CC} = 4.5 V	I_{OL} = 100 µA		0.9	1.1	
				I_{OL} = 20 µA			0.9	
I_{OH}	High-level Q output current		T_A= 25°C,	V_O = 3 V	−1.2			mA
I_{OL}	Low-level Q output current		T_A= 25°C,	V_O = −75 V			−500	µA
I_{IH}	High-level input current		T_A= 25°C,	V_I = V_{CC}			1	µA
I_{IL}	Low-level input current		T_A= 25°C,	V_I = 0			−1	µA
I_{CC}	Supply current		All Q outputs high,	V_{CC} = 5.5 V		17	25	mA
			All Q outputs low				3	
C_i	Input capacitance						15	pF

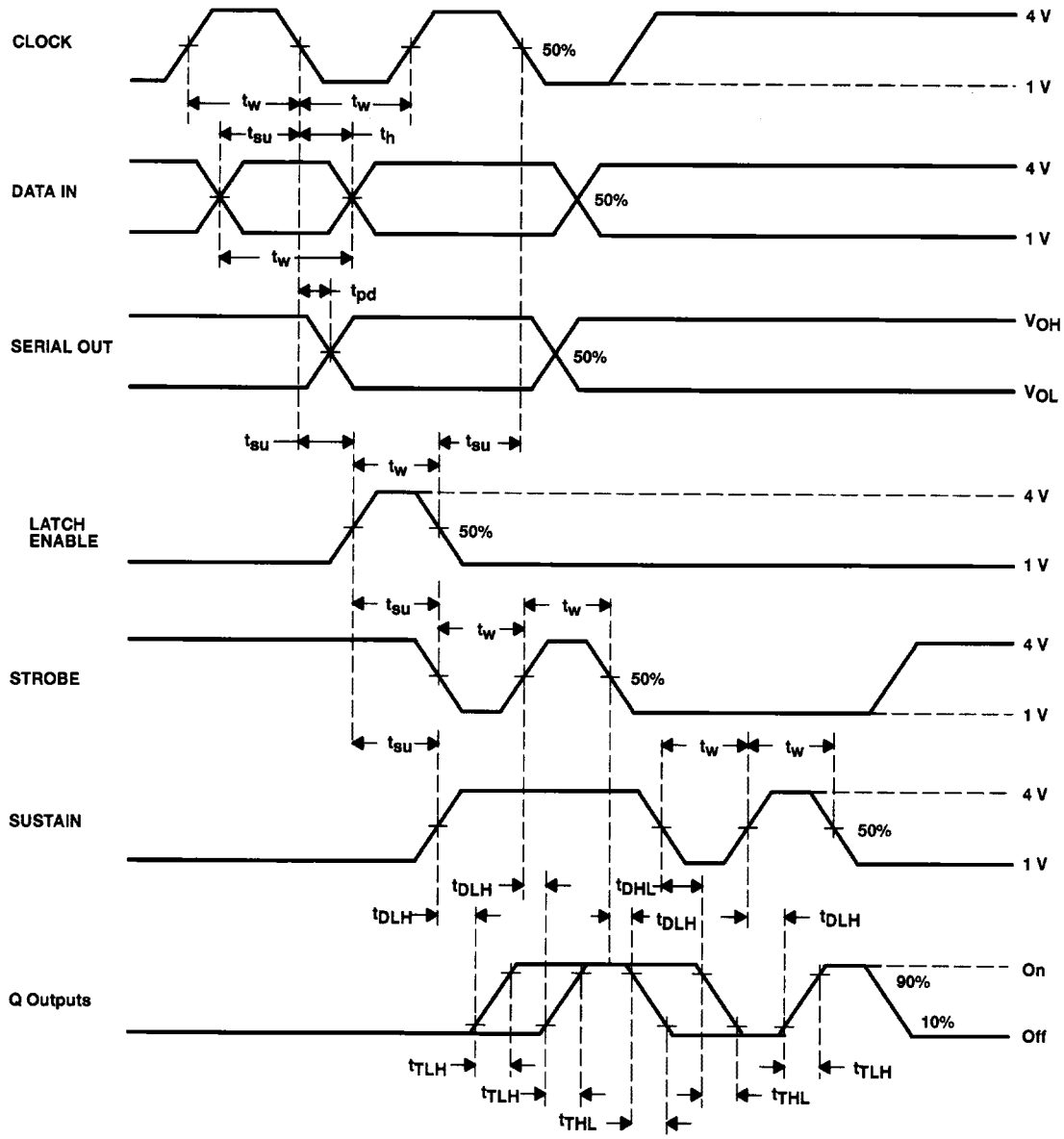
† All typical values are at T_A = 25°C.

switching characteristics, V_{CC} = 5 V, C_L = 15 pF, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd}	Propagation delay time, CLOCK to SERIAL OUT			100	150	ns
t_{DLH}	Delay time, low-to-high-level Q output from SUSTAIN or STROBE	R_L = 91 kΩ, See Figures 1 and 2		0.3‡	1	μs
t_{DHL}	Delay time, high-to-low-level Q output from SUSTAIN or STROBE			1‡	2.5	μs
t_{TLH}	Transition time, low-to-high-level Q output			2	5	μs
t_{THL}	Transition time, high-to-low-level Q output			11	18	μs

‡ Typical values for delay times are measured from SUSTAIN.

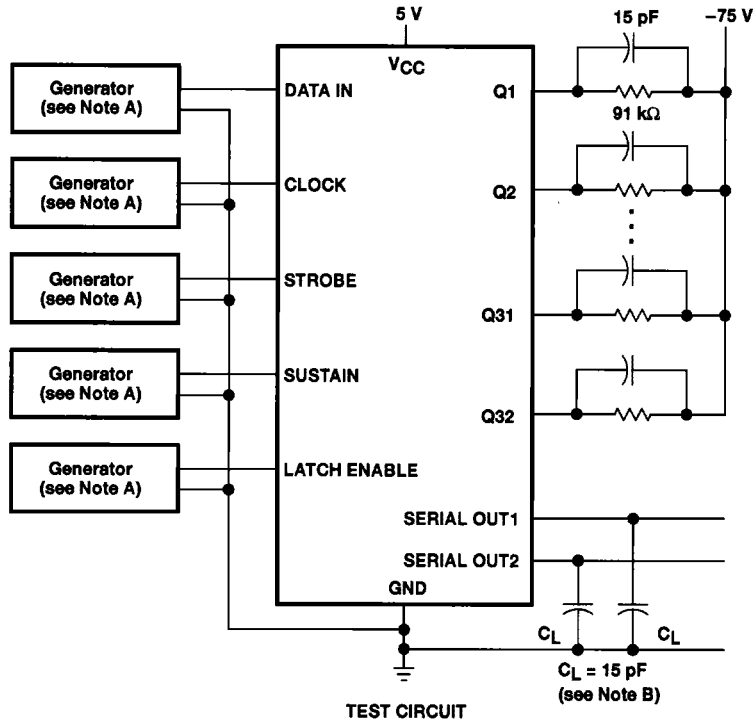
PARAMETER MEASUREMENT INFORMATION



NOTE: Input t_r and t_f are less than or equal to 10 ns.

Figure 1. Input Timing and Switching Time Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



NOTES: A. Input pulses are supplied by generators having the following characteristics: t_W = 100 ns, PRR ≤ 5 MHz, t_r ≤ 10 ns, t_f ≤ 10 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

Figure 2. Test Circuit

TYPICAL CHARACTERISTICS

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

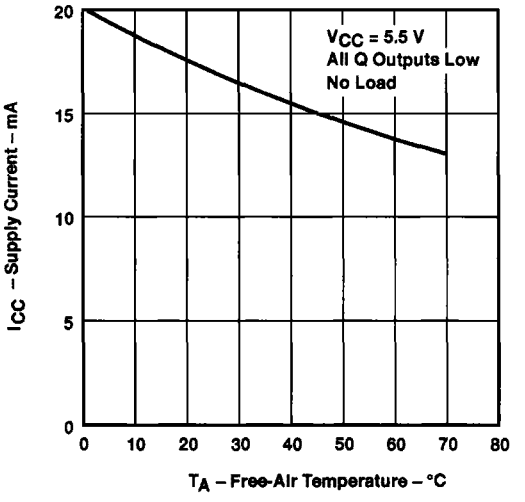


Figure 3

PROPAGATION DELAY TIME,
CLOCK TO SERIAL OUT
vs
FREE-AIR TEMPERATURE

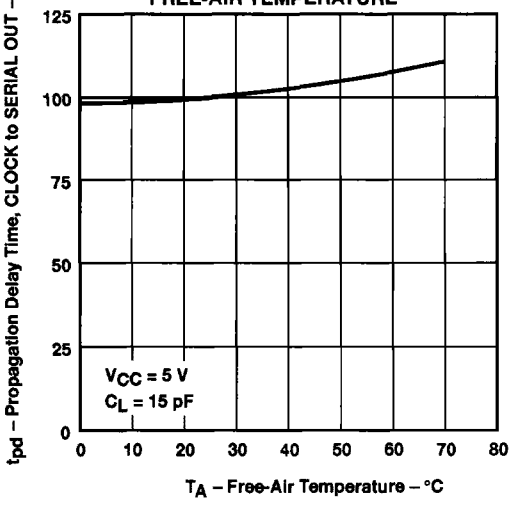


Figure 4

DELAY TIME, SUSTAIN INPUT TO Q OUTPUT
LOW TO HIGH
vs
FREE-AIR TEMPERATURE

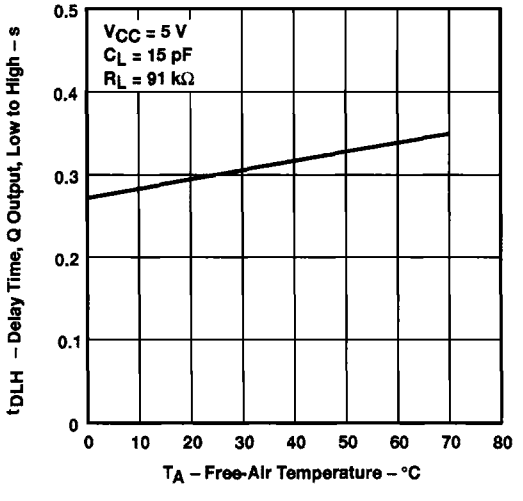


Figure 5

DELAY TIME, SUSTAIN INPUT TO Q OUTPUT
HIGH TO LOW
vs
FREE-AIR TEMPERATURE

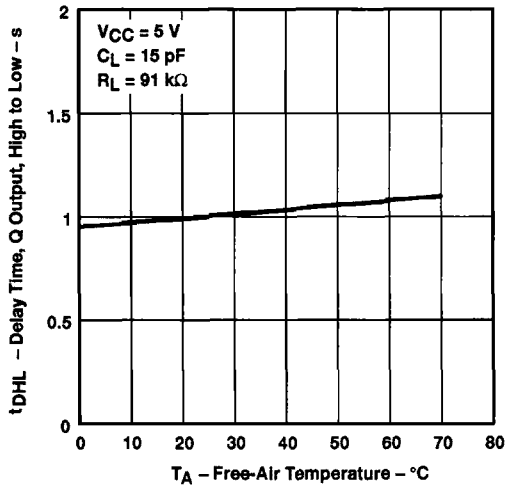


Figure 6

TYPICAL CHARACTERISTICS

TRANSITION TIME, Q OUTPUT, LOW TO HIGH vs FREE-AIR TEMPERATURE

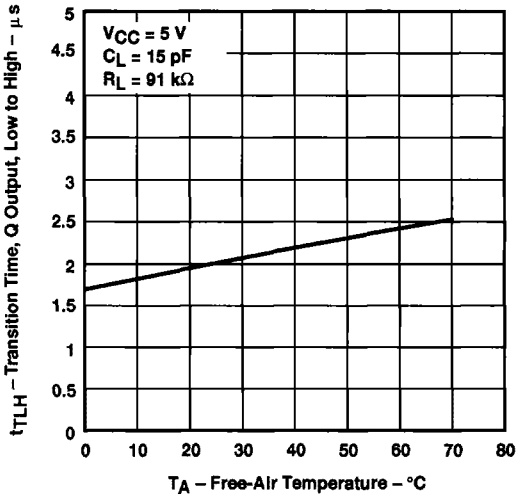


Figure 7

TRANSITION TIME, Q OUTPUT, HIGH TO LOW vs FREE-AIR TEMPERATURE

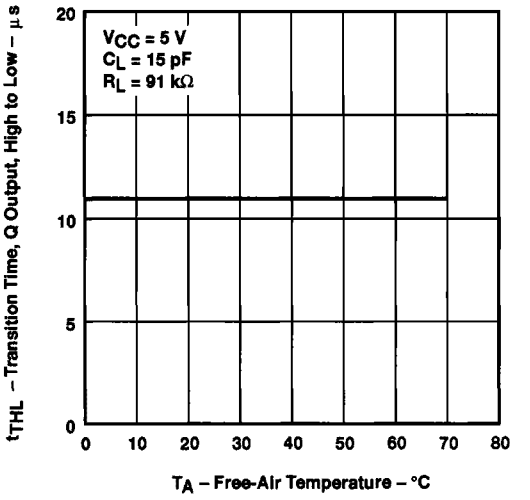


Figure 8