FEATURES

- 168-pin industry standard 8-byte Dual-in-line memory module
- JEDEC compliant: 21-C, Fig. 4-13 A,B,C,D,H (Release 5)
  No. 95 MO-161
- $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$ and Address lines are buffered
- High performance, CMOS
- Single 3.3 ± 0.3V power supply
- LVTTL-compatible inputs and outputs
- Extended Data Out access cycle
- Refresh modes: $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$, HIDDEN
- Refresh: 8192 refresh cycles every 64 ms
- Dimensions: 5.25" (length) x 1.25" (height) x 0.354" (max thickness)

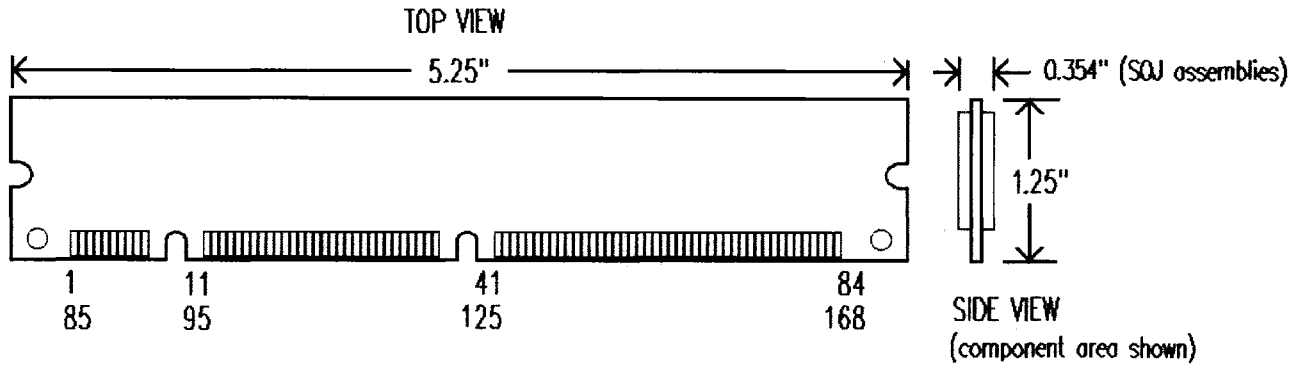
PERFORMANCE RANGE

SYMBOL	PARAMETER	Rating	
		60 ns	70 ns
t_{RAC}	$\overline{RAS}$ Access Time	60 ns (max)	70 ns (max)
t_{CAC}	$\overline{CAS}$ Access Time	15 ns (max)	20 ns (max)
t_{AA}	Access Time from Column Address	30 ns (max)	35 ns (max)
t_{RC}	Random Read or Write Cycle Time	104 ns (min)	124 ns (min)
t_{HPC}	EDO Mode Cycle Time	25 ns (min)	30 ns (min)

ORDERING INFORMATION

DESCRIPTION	PART NUMBER	ENGINEERING DESCRIPTOR
16M x 64, 60 ns, Gold Tabs, SOJ, Normal Refresh	20620C	CL001M16645CB0K-60
16M x 64, 70 ns, Gold Tabs, SOJ, Normal Refresh	20621C	CL001M16645CB0K-70
16M x 64, 60 ns, Gold Tabs, SOJ, Self Refresh	20622C	CL001M16645CC0K-60
16M x 64, 70 ns, Gold Tabs, SOJ, Self Refresh	20623C	CL001M16645CC0K-70
16M x 64, 60 ns, Gold Tabs, TSOP, Normal Refresh	20624C	CL001M16645CB0U-60
16M x 64, 70 ns, Gold Tabs, TSOP, Normal Refresh	20625C	CL001M16645CB0U-70
16M x 64, 60 ns, Gold Tabs, TSOP, Self Refresh	20626C	CL001M16645CC0U-60
16M x 64, 70 ns, Gold Tabs, TSOP, Self Refresh	20627C	CL001M16645CC0U-70

CARD OUTLINE



GENERAL DESCRIPTION

The 16M x 64 DIMM uses dynamic RAM devices and is designed for use as a general-purpose 8-byte wide memory assembly with 8 data bits per byte. The DIMM is populated with sixteen 16M x 4 DRAMs and two buffers.

All inputs are buffered except for $\overline{RAS}$ and data. Buffering serves to improve the signal quality of the inputs. The timings specified herein include buffer delays. $\overline{RAS}$ are not buffered in order to preserve the DRAM access specification.

Presence Detect (PD) and Identification (ID) bits provide information about DIMM density, addressing, performance and features. PD bits can be activated using the PD enable ($\overline{PDE}$) input signal. PD bits are also buffered.

During Read or Write Cycles, each byte may be uniquely addressed via 24 address bits, with the first 13 bits (A0~A12) latched on $\overline{RAS}$ and the latter 11 bits (A0~A10) latched on $\overline{CAS}$. READ or WRITE cycles are selected with the $\overline{WE}$ input, with a logic low indicating a WRITE cycle and a logic HIGH indicating a READ cycle. During a WRITE cycle, data-in is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last.

EXTENDED DATA OUT (EDO) operation allows for faster READs or WRITEs within a row-address-defined page boundary. EDO MODE is an enhanced FAST PAGE MODE method of operation. An EDO MODE cycle is initiated with $\overline{RAS}$ followed by $\overline{CAS}$, then strobing $\overline{CAS}$ to latch different column addresses while holding $\overline{RAS}$ LOW.

Returning $\overline{RAS}$ and $\overline{CAS}$ high terminates a memory cycle and returns the DRAMs to a reduced-current STANDBY state.

Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE) or $\overline{RAS}$ refresh cycle ($\overline{RAS}$-ONLY, CBR, or HIDDEN) so that all 8192 combinations of $\overline{RAS}$ addresses (A0~A12) are executed at least every 64 ms. The CBR refresh and HIDDEN refresh cycles will invoke the on-chip refresh address counters for automatic $\overline{RAS}$ addressing.

PIN DESCRIPTION

$\overline{RAS0}$,$\overline{RAS2}$	Row Address Strobe
$\overline{CAS0}$~$\overline{CAS7}$	Column Address Strobe(Buffered)
$\overline{WE0}$,$\overline{WE2}$	Write Enable (Buffered)
$\overline{OE0}$,$\overline{OE2}$	Output Enable (Buffered)
A0, B0, A1 ~ A12	Address Input (Buffered)
DQx	Data Input/Output
VCC	Power (+3.3V)
VSS	Ground
NC	No Connect
PD1 ~ PD8	Presence Detects (Buffered)
$\overline{PDE}$	Presence Detect Enable
ID0 ~ ID1	ID Bits

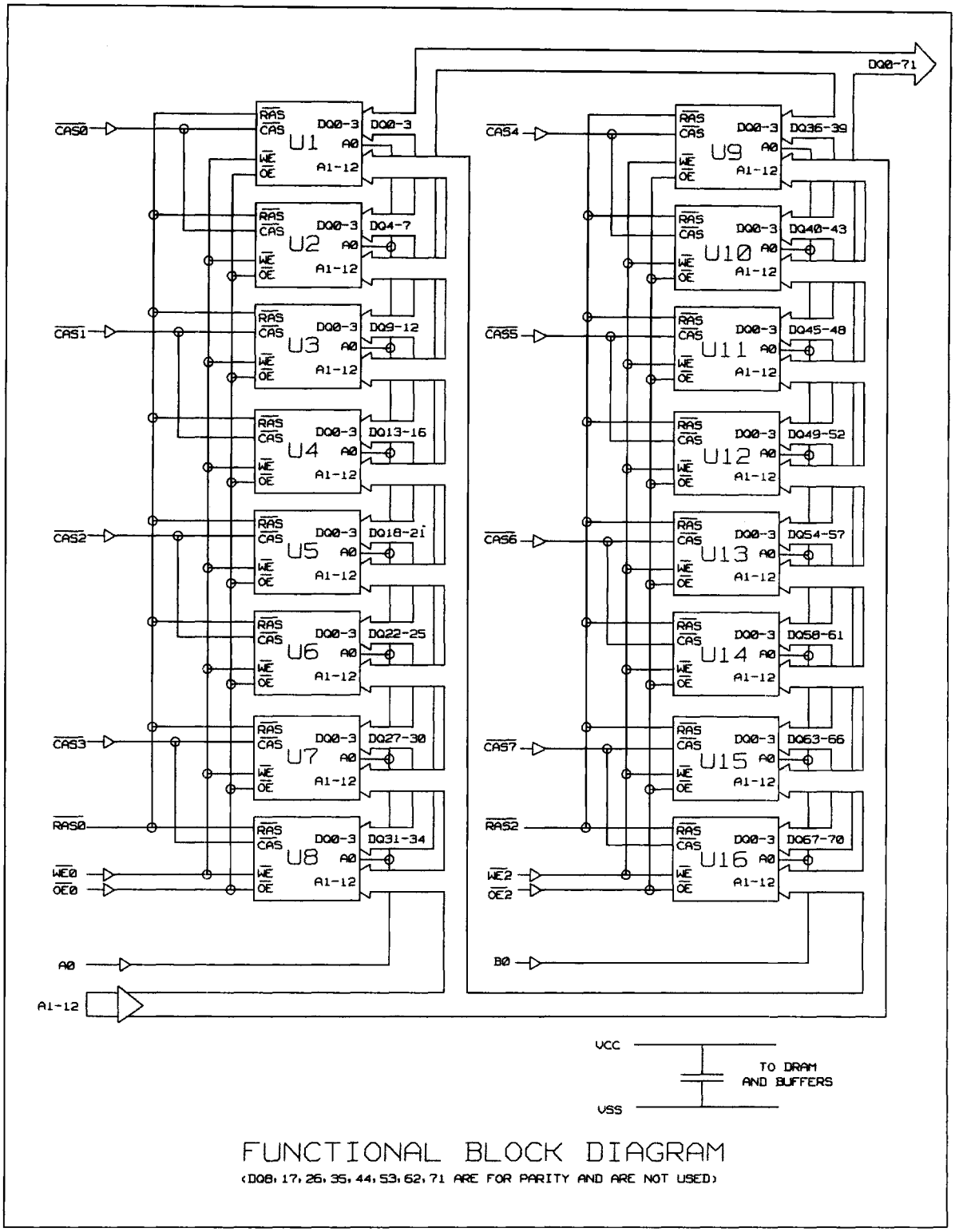
PRESENCE DETECT

PIN SYMBOL	CONFIGURATION	
	60 ns	70 ns
PD1 (PD1~PD4: Addressing/Density)	1	1
PD2	1	1
PD3	1	1
PD4	1	1
PD5 (Data Access Mode)	1	1
PD6 (PD6~PD7: Speed)	1	0
PD7	1	1
PD8 (Parity/ECC Configuration)	1	1
ID0 (DIMM Type/Width)	0	0
ID1 (Refresh Mode)	0	0

Note: PD1-8 are buffered outputs (0 = driven to V_{OL}, 1 = open)
ID0-1 are unbuffered outputs
ID0 (0 = V_{SS}, 1 = open)
ID1 = 0 for Normal Refresh, and 1 for Self Refresh

PIN CONFIGURATION

Pin #	Front Side	Pin #	Front Side	Pin #	Back Side	Pin #	Back Side
1	VSS	43	VSS	85	VSS	127	VSS
2	DQ0	44	$\overline{OE2}$	86	DQ36	128	NC
3	DQ1	45	$\overline{RAS2}$	87	DQ37	129	NC
4	DQ2	46	$\overline{CAS4}$	88	DQ38	130	$\overline{CAS5}$
5	DQ3	47	$\overline{CAS6}$	89	DQ39	131	$\overline{CAS7}$
6	VCC	48	$\overline{WE2}$	90	VCC	132	$\overline{PDE}$
7	DQ4	49	VCC	91	DQ40	133	VCC
8	DQ5	50	NC	92	DQ41	134	NC
9	DQ6	51	NC	93	DQ42	135	NC
10	DQ7	52	DQ18	94	DQ43	136	DQ54
11	NC	53	DQ19	95	NC	137	DQ55
12	VSS	54	VSS	96	VSS	138	VSS
13	DQ9	55	DQ20	97	DQ45	139	DQ56
14	DQ10	56	DQ21	98	DQ46	140	DQ57
15	DQ11	57	DQ22	99	DQ47	141	DQ58
16	DQ12	58	DQ23	100	DQ48	142	DQ59
17	DQ13	59	VCC	101	DQ49	143	VCC
18	VCC	60	DQ24	102	VCC	144	DQ60
19	DQ14	61	NC	103	DQ50	145	NC
20	DQ15	62	NC	104	DQ51	146	NC
21	DQ16	63	NC	105	DQ52	147	NC
22	NC	64	NC	106	NC	148	NC
23	VSS	65	DQ25	107	VSS	149	DQ61
24	NC	66	NC	108	NC	150	NC
25	NC	67	DQ27	109	NC	151	DQ63
26	VCC	68	VSS	110	VCC	152	VSS
27	$\overline{WE0}$	69	DQ28	111	NC	153	DQ64
28	$\overline{CAS0}$	70	DQ29	112	$\overline{CAS1}$	154	DQ65
29	$\overline{CAS2}$	71	DQ30	113	$\overline{CAS3}$	155	DQ66
30	$\overline{RAS0}$	72	DQ31	114	NC	156	DQ67
31	$\overline{OE0}$	73	VCC	115	NC	157	VCC
32	VSS	74	DQ32	116	VSS	158	DQ68
33	A0	75	DQ33	117	A1	159	DQ69
34	A2	76	DQ34	118	A3	160	DQ70
35	A4	77	NC	119	A5	161	NC
36	A6	78	VSS	120	A7	162	VSS
37	A8	79	PD1	121	A9	163	PD2
38	A10	80	PD3	122	A11	164	PD4
39	A12	81	PD5	123	NC	165	PD6
40	VCC	82	PD7	124	VCC	166	PD8
41	NC	83	ID0	125	NC	167	ID1
42	NC	84	VCC	126	B0	168	VCC



FUNCTIONAL BLOCK DIAGRAM

(DQ8, 17, 26, 35, 44, 53, 62, 71 ARE FOR PARITY AND ARE NOT USED)

TRUTH TABLE

FUNCTION	RAS	CAS	WE	OE	ROW ADDR	COL ADDR	PDE	DQx
Standby	H	X	X	X	X	X	X	Hi-Z
Read	L	L	H	L	ROW	COL	X	Valid D_{OUT}
Early-Write	L	L	L	X	ROW	COL	X	Valid D_{IN}
RMW	L	L	H→L	L→H	ROW	COL	X	Valid D_{OUT}
EDO Mode-Read 1st Cycle	L	H→L	H	L	ROW	COL	X	Valid D_{OUT}
Subsequent Cycles	L	H→L	H	L	N/A	COL	X	Valid D_{OUT}
EDO Mode-Read 1st Cycle ($\overline{WE}$ Control)	L	H→L	L	L	ROW	COL	X	Valid D_{OUT}
Subsequent Cycles	L	H→L	H→L→H	L	N/A	COL	X	Valid D_{OUT}
EDO Mode-Write 1st Cycle	L	H→L	L	X	ROW	COL	X	Valid D_{IN}
Subsequent Cycles	L	H→L	L	X	N/A	COL	X	Valid D_{OUT} Valid D_{IN}
EDO Mode-RMW 1st Cycle	L	H→L	H→L	L→H	ROW	COL	X	Valid D_{OUT} Valid D_{IN}
Subsequent Cycles	L	H→L	H→L	L→H	N/A	COL	X	Valid D_{OUT} Valid D_{IN}
$\overline{RAS}$-Only Refresh	L	H	X	X	ROW	N/A	X	Hi-Z
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh	H→L	L	H	X	X	X	X	Hi-Z
Read Presence Detects	X	X	X	X	X	X	L	Not Affected (PD Bits Valid)

X:"H" or "L" D_{IN}:Data In D_{OUT}:Data Out Hi-Z:High Impedance N/A:Not Applicable

ABSOLUTE MAXIMUM RATINGS (Note 1,22)

SYMBOL	PARAMETER	RATING	UNITS	NOTES
V_{CC}	Power Supply Voltage	-0.5 to 4.6	V	2
V_{IN}	Voltage on any Pin Relative to V_{SS}	-0.5 to 4.6	V	2
V_{OUT}		-0.5 to 4.6	V	2
T_{opr}	Operating Temperature	0 to 70	°C	
T_{stg}	Storage Temperature	-55 to 150	°C	
P_D	Power Dissipation	18.0	W	17,31
I_{OS}	Short Circuit Output Current	50	mA	17

RECOMMENDED OPERATING CONDITIONS (T_A= 0 to 70 °C) (Note 2)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS	NOTES
V_{CC}	Supply Voltage	3	3.3	3.6	V	
V_{SS}	Ground	0	0	0	V	
V_{IH}	Input High Voltage	2		Vcc+0.3	V	22
V_{IL}	Input Low Voltage	-0.3		0.8	V	22

T_A: Ambient temperature

CAPACITANCE (f = 1 MHz; T_A = 25 °C) (Note 22)

SYMBOL	PARAMETER	MAX.	UNITS	NOTES
C_{I1}	Input Capacitance (All except $\overline{RAS}$)	6	pF	
C_{I2}	Input Capacitance ($\overline{RAS1}$,$\overline{RAS3}$)	56	pF	
C_{O1}	Output Capacitance (Data In/Out)	9	pF	

T_A: Ambient temperature

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.) (Note 18,22)

SYMBOL	PARAMETER	SPEED	MIN.	MAX.	NOTES
I_{CC1}	OPERATING CURRENT: Average Power Supply Operating Current ($\overline{RAS}$,$\overline{CAS}$, Address Cycling@t_{RC} = $t_{RC(min)}$,V_{CC} = $V_{CC\ (max)}$)(mA)	60 ns	-	2097	3,4,5,6, 16
		70 ns	-	1937	
I_{CC2}	STANDBY CURRENT (TTL): Power Supply Standby Current ($\overline{RAS}$=$\overline{CAS}$=Vcc, Data out is disabled (Hi-Z), all other inputs =Vcc, V_{CC} =$V_{CC\ (max)}$) (mA)	Don't Care	-	17	
I_{CC3}	$\overline{RAS}$-ONLY REFRESH CURRENT: Average Power Supply Current, $\overline{RAS}$-Only Mode ($\overline{RAS}$, Address Cycling, $\overline{CAS}$=V_{IH}@t_{RC}=$t_{RC(min)}$,V_{CC}=$V_{CC(max)}$) (mA)	60 ns	-	2097	3,4,5,6,16, 31
		70 ns	-	1937	
I_{CC4}	EXTENDED DATA OUT MODE CURRENT: Average Power Supply Current, EDO ($\overline{RAS}$=V_{IL},$\overline{CAS}$, Address Cycling@ t_{PC}=$t_{PC(min)}$,V_{CC}=$V_{CC(max)}$) (mA)	60 ns	-	2097	3,4,5,7,16
		70 ns	-	1777	
I_{CC5}	STANDBY CURRENT (CMOS): Power Supply Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{CC}-0.2V, Data Out is disabled (Hi-Z),V_{CC} = $V_{CC(max)}$) (mA)	Don't Care	-	9	
I_{CC6}	$\overline{CAS}$-BEFORE-$\overline{RAS}$, REFRESH CURRENT: Average Power Supply Current, $\overline{CAS}$-Before-$\overline{RAS}$ Mode ($\overline{RAS}$,$\overline{CAS}$ Cycling@t_{RC}=$t_{RC(min)}$, V_{CC} = $V_{CC(max)}$)(mA)	60 ns	-	2417	3,4,5,6,16, 31
		70 ns	-	2257	
I_{LI}	INPUT LEAKAGE CURRENT: Input Leakage Current, any input (0≤V_{IN}≤V_{CC}, all other pins not under test=0V, V_{CC}= $V_{CC(max)}$) (µA)	**All except $\overline{RAS}$**	-5	5	
		$\overline{RAS}$0,$\overline{RAS}$2	-80	80	
I_{LO}	OUTPUT LEAKAGE CURRENT: (Data Out is disabled (Hi-Z), 0≤V_{OUT}≤V_{CC})(µA)		-10	10	
V_{OH}	OUTPUT HIGH LEVEL: Output "H" Level Voltage (I_{OUT}=-5mA) (V)		2.4	-	2
V_{OL}	OUTPUT LOW LEVEL: Output "L" Level Voltage (I_{OUT}=+4.2mA) (V)		-	0.4	2

AC CHARACTERISTICS

READ, WRITE, READ-MODIFY-WRITE AND REFRESH CYCLES (COMMON PARAMETERS)
(Recommended operating conditions unless otherwise noted.) (Note 8,18)

SYMBOL	PARAMETER	60 ns		70 ns		NOTES
		MIN.	MAX.	MIN.	MAX.	
t_{RC}	Random READ or WRITE Cycle Time (ns)	104	-	124	-	
t_{RP}	$\overline{RAS}$ Precharge Time (ns)	40	-	50	-	
t_{CP}	$\overline{CAS}$ Precharge Time (ns)	10	-	10	-	
t_{RAS}	$\overline{RAS}$ Pulse Width (ns)	60	10000	70	10000	23
t_{CAS}	$\overline{CAS}$ Pulse Width (ns)	10	10000	15	10000	23
t_{ASR}	Row Address Setup Time (ns)	5	-	5	-	22
t_{RAH}	Row Address Hold Time (ns)	9	-	9	-	
t_{ASC}	Column Address Setup Time (ns)	4	-	4	-	22
t_{CAH}	Column Address Hold Time (ns)	14	-	19	-	22
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time (ns)	19	40	19	45	10
t_{RAD}	$\overline{RAS}$ to Col. Address Delay Time (ns)	14	25	14	30	15
t_{RSH}	$\overline{RAS}$ Hold Time (ns)	20	-	25	-	22
t_{CSH}	$\overline{CAS}$ Hold Time (ns)	49	-	54	-	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time (ns)	10	-	10	-	22
t_{ODD}	$\overline{OE}$ to D_{IN} Delay Time (ns)	18	-	20	-	22,27
t_{DZO}	$\overline{OE}$ Delay Time from D_{IN} (ns)	-	-	-	-	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ hold Time (ns)	4	-	4	-	22
t_T	Transition Time (Rise and Fall) (ns)	2	50	2	50	22
t_{AR}	Column Address Hold Time Referenced to $\overline{RAS}$ (ns)	44	-	54	-	22

READ CYCLES (Note 8,18)

SYMBOL	PARAMETER	60 ns		70 ns		NOTES
		MIN.	MAX.	MIN.	MAX.	
t_{RAC}	Access Time from $\overline{RAS}$ (ns)	-	60	-	70	9,10,15,30
t_{CAC}	Access Time from $\overline{CAS}$ (ns)	-	20	-	25	9,10,30
t_{AA}	Access Time from Address (ns)	-	35	-	40	9,15,30
t_{OEA}	Access Time from $\overline{OE}$ (ns)	-	20	-	25	9
t_{RCS}	Read Command Setup Time (ns)	4	-	4	-	22
t_{RCH}	Read Command Hold Time to $\overline{CAS}$ (ns)	4	-	4	-	14,22
t_{RRH}	Read Command Hold Time to $\overline{RAS}$ (ns)	-1	-	-1	-	14,22
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time(ns)	35	-	40	-	22
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z (ns)	1	-	1	-	9,22
t_{OEZ}	Output Buffer Turn-off Delay from $\overline{OE}$ (ns)	1	20	1	20	12,24
t_{DZC}	Data to $\overline{CAS}$ Low Delay Time (ns)	-	-	-	-	
t_{CDD}	$\overline{CAS}$ High to Data Delay Time (ns)	-	-	-	-	
t_{OFF}	Output Buffer Turn-Off Delay (ns)	1	20	1	20	12,24

WRITE CYCLES (Note 8,18)

SYMBOL	PARAMETER	60 ns		70 ns		NOTES
		MIN.	MAX.	MIN.	MAX.	
t_{WCS}	Write Command Set Up Time (ns)	4	-	4	-	13
t_{WCH}	Write Command Hold Time (ns)	14	-	19	-	
t_{WP}	Write Command Pulse Width (ns)	10	-	15	-	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time (ns)	20	-	25	-	22
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time (ns)	19	-	19	-	
t_{DS}	D_{IN} Setup Time (ns)	-1	-	-1	-	25
t_{DH}	D_{IN} Hold Time (ns)	15	-	20	-	22,25
t_{WCR}	Write Command Hold Time Referenced to $\overline{RAS}$ (ns)	44	-	54	-	22
t_{DHR}	Data in Hold Time Referenced to $\overline{RAS}$ (ns)	45	-	55	-	22

PRESENCE DETECT READ CYCLE (Note 8,19,24)

SYMBOL	PARAMETER	MIN.	MAX.	NOTES
t_{PD}	$\overline{PDE}$ to Valid Presence Detect Data	2	7	
t_{PDOFF}	$\overline{PDE}$ Inactive to Presence Detects Inactive	2	6	12

EXTENDED DATA OUT MODE CYCLES (Note 8,9,18)

SYMBOL	PARAMETER	60 ns		70 ns		NOTES
		MIN.	MAX.	MIN.	MAX.	
t_{HPC}	EDO Mode Cycle Time (ns)	25	-	30	-	22
t_{RASP}	EDO Mode $\overline{RAS}$ Pulse Width (ns)	60	125000	70	125000	
t_{HCAS}	EDO MODE $\overline{CAS}$ Pulse Width (ns)	10	10000	15	10000	22
t_{CPRH}	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge (ns)	40	-	45	-	22
t_{CPA}	Access Time from $\overline{CAS}$ Precharge (ns)	-	40	-	45	21,22,30
t_{WPZ}	EDO Mode Write Command Pulse Width (ns)	10	-	15	-	22
t_{HPRWC}	EDO Mode Read-Modify-Write (ns)	75	-	85	-	22
t_{DOH}	D_{OUT} Hold Time (ns)	4	-	4	-	22
t_{WHZ}	Output Buffer Turn-Off Delay from $\overline{WE}$ (ns)	8	14	8	16	12,22
t_{CPW}	$\overline{WE}$ Delay Time From $\overline{CAS}$ Precharge (ns)	58	-	68	-	

REFRESH CYCLE (Note 8,18)

SYMBOL	PARAMETER	60 ns		70 ns		NOTES
		MIN.	MAX.	MIN.	MAX.	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle) (ns)	9	-	14	-	22
t_{CSR}	$\overline{CAS}$ Setup Time ($\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle) (ns)	15	-	15	-	22
t_{WRP}	$\overline{WE}$ Setup Time ($\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle) (ns)	15	-	15	-	22
t_{WRH}	$\overline{WE}$ Hold Time ($\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle) (ns)	9	-	9	-	22
t_{REF}	Refresh Period (8192 cycles) (ms)	-	64	-	64	

READ-MODIFY-WRITE CYCLE (Note 8,18)

SYMBOL	PARAMETER	60 ns		70 ns		NOTES
		MIN.	MAX.	MIN.	MAX.	
t_{RWC}	Read-Modify-Write Cycle Time (ns)	150	-	177	-	22
t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay Time (ns)	79	-	89	-	13
t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay Time (ns)	39	-	44	-	13,22
t_{AWD}	Column Address to $\overline{WE}$ Delay Time (ns)	59	-	69	-	13,22
t_{OEH}	$\overline{OE}$ Hold Time After $\overline{WE}$ Low (ns)	19	-	24	-	

NOTES

1. Permanent damage to the device may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2. All voltages referenced to V_{SS}.

3. I_{CC} is specified as an average current.

4. This parameter depends on output loading and/or cycle rates.

5. Specified values are obtained with the output open.

6. Address can be changed a maximum of once while $\overline{RAS}=V_{IL}$.

7. Address can be changed a maximum of once while $\overline{CAS}=V_{IH}$.

8. $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals. Transition time (t_T) is measured between $V_{IH(min)}$ and $V_{IL(max)}$, and is assumed to be 2ns for all inputs. All input signals must transit between V_{IH} and V_{IL} (or V_{IL} and V_{IH}) without slope reversal.

9. Measured with a load equivalent to 2 TTL loads and 100pF.

10. Operation within the $t_{RCD(max)}$ limit ensures that $t_{RAC(max)}$ can be met. $t_{RCD(max)}$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD(max)}$ limit, then access time is controlled exclusively by t_{CAC}.

11. Assumes that $t_{RAD} \leq t_{RAD(max)}$.

12. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.

13. This is a non-restrictive operating parameter. It is included in the data sheet as an electrical characteristic only. If $t_{WCS} \geq t_{WCS(min)}$ the cycle is an early write cycle and the data out pins will remain high impedance (open circuit) for the duration of the cycle. If $t_{CWD(min)} \geq t_{CWD(min)}$, $t_{RWD} \geq t_{RWD(min)}$, $t_{AWD} \geq t_{AWD(min)}$, and $t_{CPW} \geq t_{CPW(min)}$ (for Fast Page Mode cycle only), then the cycle is a Read-Modify-Write cycle and the data output pins will hold the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out (at access time) is indeterminate.

14. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

15. Operation within the $t_{RAD(max)}$ limit ensures that $t_{RAC(max)}$ can be met. $t_{RAD(max)}$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD(max)}$ limit, then access time is controlled exclusively by t_{AA}.

16. Specified values are obtained with minimum cycle time.

17. Specified values are obtained with T_A=25°C.

18. An initial pause of 200µs is required after power-up followed by a minimum of eight initialization cycles (any 8 $\overline{CAS}$-before-$\overline{RAS}$ or $\overline{RAS}$-only Refresh cycles with $\overline{WE}$ high) before proper device operation is assured. Also, any 8 $\overline{CAS}$-before-$\overline{RAS}$ or $\overline{RAS}$-only Refresh cycles with $\overline{WE}$ high are required after prolonged periods (greater than t_{REF}) of $\overline{RAS}$ inactivity before proper device operation is assured.

19. Measured with a load equivalent to 50pF and 500 ohms.

20. Write cycle is applicable instead of read cycle. Timing requirements for $\overline{RAS}$,$\overline{CAS}$ and Address are the same for Hidden Refresh Write Cycle as that shown for Hidden Refresh Read Cycle. $\overline{WE}$, D_{IN} and D_{OUT} for Hidden Refresh Write Cycle are the same as for Write Cycle.

21. t_{CPA} is access time from $\overline{CAS}$ precharge (that is caused by changing $\overline{CAS}$ from "L" to "H"). Therefore, if t_{CP} is long, then t_{CPA} is longer than $t_{CPA(max)}$.

22. Calculated based on data supplied by the DRAM manufacturer(s).

23. Maximum value is calculated based on data supplied by the DRAM manufacturer(s).

24. Minimum value is calculated based on data supplied by the DRAM manufacturer(s).

25. This parameter is referenced to the $\overline{CAS}$ leading edge in Early Write cycles and to the $\overline{WE}$ leading edge in Read-Modify-Write cycles.

26. V_{IN} = 0 Volt.

27. Either t_{CDD} or t_{ODD} must be satisfied.

28. Either t_{DZC} or t_{DZO} must be satisfied.

29. $t_{RASP(MIN)}$ is specified as two cycles of $\overline{CAS}$ input are performed.

30. The access time is limited by all four parameters t_{RAC}, t_{CAC}, t_{AA}, t_{CPA}.

31. This assumes all $\overline{RAS}$ (and all $\overline{CAS}$ for CBR refresh) are active.

For Timing Diagrams see **"EDO Timing Diagrams"** (Document No. **20431C**).

Available from fax-on-demand and Website: **http://www.celestica.com/memory/**

Contact Information
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