54F/74F146

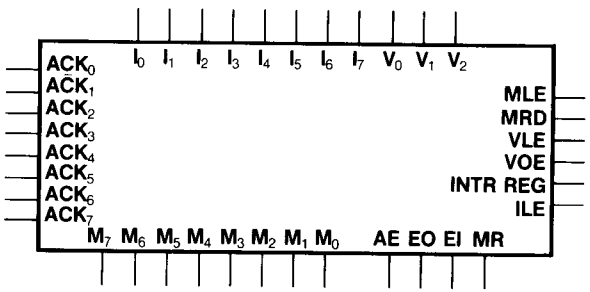
Priority Interrupt/DMA Request Controller

Description

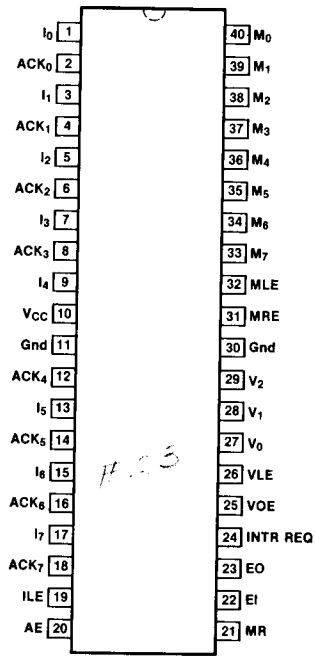
The 'F146 Priority Interrupt/DMA Request Controller is used to control the access of input and output units to the processing unit. The 'F146 can handle simultaneous or multiple requests according to their priority. Both a signal indicating an interrupt/DMA request and 3-bit binary coded vector of the the highest level interrupt are generated. Interrupt input and vector output latches are provided to add flexibility to the interrupt scheme. The mask latch provides masking capability of any level interrupt before prioritization. The I/O ports and control logic allow direct bus interfacing. The acknowledge outputs generate the bus acknowledge signals for DMA controlling or multi-processor environments.

Ordering Code: See Section 5

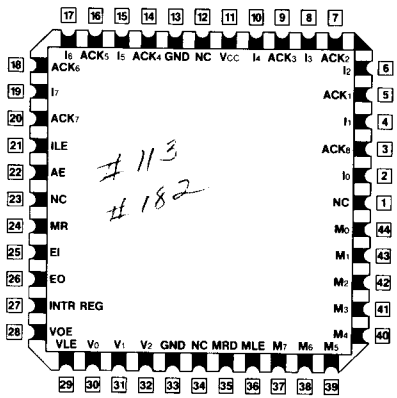
Logic Symbol



Connection Diagrams



Pin Assignment for DIP



Pin Assignment for LCC and PCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
$\overline{I}_0$-$\overline{I}_7$	Interrupt Pins	0.5/0.375
$\overline{ACK}_0$-$\overline{ACK}_7$	Acknowledge Outputs	25/12.5
ILE	Interrupt Latch Enable	0.5/0.375
$\overline{AE}$	Acknowledge Enable (Active LOW)	0.5/0.375
$\overline{MR}$	Master Reset	0.5/0.375
$\overline{INRQ}$	Interrupt Request	25/12.5
M_0-M_7	Mask Inputs	0.5/0.375
$\overline{CS}$	Mask Latch Address Select Line	0.5/0.375
R/$\overline{W}$	Mask Latch Read/Write Control Line	0.5/0.375
$\overline{V}_0$-$\overline{V}_2$	Priority Vector	25/12.5
VLE	Vector Latch Enable	0.5/0.375
$\overline{VOE}$	Vector Output Enable (Active LOW)	0.5/0.375
$\overline{EO}$	Expansion Output (Active LOW)	25/12.5
$\overline{EI}$	Expansion Input (Active LOW)	0.5/0.375

Functional Description

The basic function of the 'F146 Priority Interrupt/DMA Controller is as follows. The receipt of an interrupt signal from the Interrupting Peripheral generates an Interrupt Request signal, stopping the processor after the current instruction or bus cycle. The processor will respond by enabling the vector data generated by the 'F146 to be read on the data bus and generating an acknowledge enable signal. This Acknowledge signal is used by the 'F146 to generate the Peripheral Acknowledge signal and reset the Interrupt Request. The 'F146 consists of four major sections as described below:

Interrupt Latch

The interrupt latch is organized as eight SR latches. The Set input is used to catch negative transitions on the Interrupt ($\overline{I}_n$) inputs. Latch Enable (ILE) latches the current interrupt status and inhibits further changes. The Reset ($\overline{MR}$) input to each latch is fully overriding, resetting the latch regardless of the state of the ILE input. If both S and R are HIGH, the previous state of the Latch is held.

Mask Latch

The Mask Latch is an Octal Latched Transceiver. This latch allows changes to the interrupt scheme to be made dynamically by masking out chosen interrupts before prioritizing. The Address Select Line ($\overline{CS}$) selects the mask latch on the negative transition and the Latch Read/Write Control Line (R/$\overline{W}$) controls the Read/Write status of the mask latch. The Mask (M) I/O ports add the freedom of storing the current mask word for retrieval at a later time, thus requiring no register overhead.

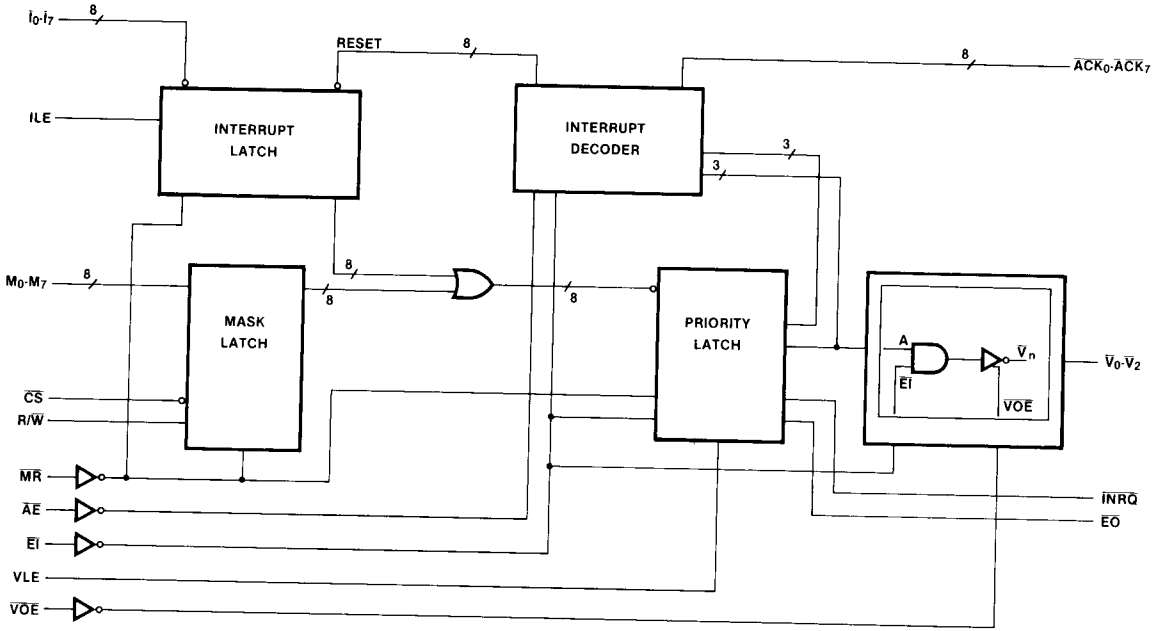
Priority Latch

The Priority Encoder ($\overline{V}_n$) and Vector Latch (VLE) can be integrated into one functional block. The Priority Latch encodes the eight interrupt lines (and the complements) providing a 3-bit binary vector. A priority is assigned to each input so that when two or more inputs are active, the one with the highest priority is represented by the vector output. The Expansion Input ($\overline{EI}$) and the Expansion Output ($\overline{EO}$) signals are provided for cascade expansion, with the $\overline{EO}$ being the more significant Priority Encoder driving the $\overline{EI}$ which is less significant. The latch is employed to prevent erroneous vector outputs during reading and peripheral acknowledge cycles. The Group Signal ($\overline{INRQ}$) provides direct detection of an interupt before vector generation is complete.

Interrupt Decoder

A 3-to-8 line decoder decodes the vector address generating the peripheral acknowledge outputs ($\overline{ACK}_n$) and the Interrupt Latch Reset ($\overline{MR}$) signals.

Block Diagram



DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current		100	150	mA	V_{CC} = Max

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F	54F	74F	Units
		$T_A = +25°C$ $V_{CC} = +5.0\ V$ $C_L = 50\ pF$	T_A, V_{CC} = Mil $C_L = 50\ pF$	T_A, V_{CC} = Com $C_L = 50\ pF$	
		Min Typ Max	Min Max	Min Max	
t_{PLH} t_{PHL}	Propagation Delay $\overline{I}$ to $\overline{INRQ}$	14.0 14.0			ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{EI}$ to $\overline{EO}$, $\overline{ACK_n}$, $\overline{V_n}$ or $\overline{INRQ}$	8.0 8.0			ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{CS}$ to $\overline{INRQ}$ or $\overline{V_n}$	14.0 14.0			ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{I_n}$ to $\overline{V_n}$	14.0 14.0			ns
t_{PLH} t_{PHL}	Propagation Delay ILE to $\overline{V_n}$	14.0 14.0			ns
t_{PLH} t_{PHL}	Propagation Delay ILE to $\overline{INRQ}$	14.0 14.0			ns
t_{PLH} t_{PHL}	Propagation Delay R/$\overline{W}$ to $\overline{INRQ}$ or $\overline{V_n}$	14.0 14.0			ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{MR}$ to $\overline{V_n}$	10.0 10.0			ns
t_{PLH} t_{PHL}	Propagation Delay VLE to $\overline{V_n}$	11.5 11.5			ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{AE}$ to $\overline{ACK_n}$	8.0 8.0			ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{MR}$ to $\overline{INRQ}$	14.0 14.0			ns
t_{PLH} t_{PHL}	Propagation Delay M_n to $\overline{INRQ}$ or $\overline{V_n}$	14.0 14.0			ns
t_{PHZ} t_{PLZ}	Output Enable Time $\overline{VOE}$ to $\overline{V_n}$	8.0 8.0			ns
t_{PZH} t_{PZL}	Output Disable Time $\overline{VOE}$ to $\overline{V_n}$	8.0 8.0			ns
t_{PHZ} t_{PLZ}	Output Enable Time $\overline{CS}$ or R/$\overline{W}$ to M_n	8.0 8.0			ns
t_{PZH} t_{PZL}	Propagation Delay $\overline{CS}$ or R/$\overline{W}$ to M_n	8.0 8.0			ns

AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	54F/74F	54F	74F	Units
		$T_A = +25°C$ $V_{CC} = +5.0\ V$	T_A, V_{CC} = Mil	T_A, V_{CC} = Com	
		Min Typ Max	Min Max	Min Max	
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW $\overline{I}_n$ to ILE	4.0 4.0			ns
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW $\overline{I}_n$ to ILE	3.0 3.0			
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW M_n to $\overline{CS}$ or R/$\overline{W}$	4.0 4.0			ns
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW M_n to $\overline{CS}$ or R/$\overline{W}$	3.0 3.0			
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW M_n or $\overline{I}_n$ to VLE	7.0 7.0			ns
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW M_n or $\overline{I}_n$ to VLE	3.0 3.0			
$t_w(L)$	$\overline{MR}$ Pulse Width, LOW	6.0			ns
$t_w(L)$	ILE or VLE Pulse Width, LOW	6.0			ns
t_{rec}	Recovery Time $\overline{MR}$ to ILE	6.0			ns
t_{rec}	Recovery Time $\overline{MR}$ to $\overline{CS}$ or R/$\overline{W}$	6.0			ns

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