DS 3290 -1.0

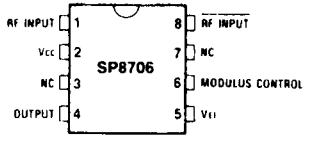
SP8706

980MHz LOW CURRENT TWO-MODULUS DIVIDER

The SP8706 is a divide by 80/81 programmable divider with a maximum specified operating frequency of 980MHz.

The signal (clock) inputs are biased externally and require to be capacitor coupled.

The SP8706 will operate from a supply of 5V.



MP8

Figure 1 Pin connections - top view

FEATURES

- DC to 980MHz Operation
- -40°C to +70°C Temperature Range

QUICK REFERENCE DATA

- Supply Voltage 4.5V to 5.5V
- Supply Current 20mA - Including Output Emitter Follower

ABSOLUTE MAXIMUM RATINGS

Supply voltage	7V
Storage temperature range	-55°C to +125°C
Junction temperature	+175°C

ORDERING INFORMATION

SP8706 KG MPAS

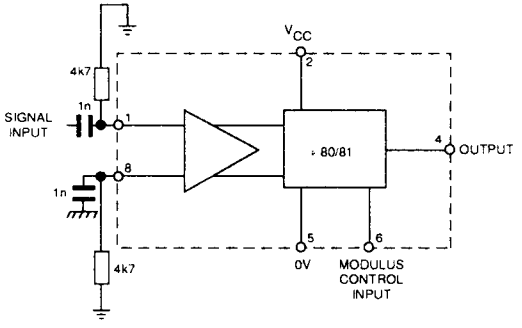


Figure 2 : Functional diagram SP8706

ABSOLUTE MAXIMUM CHARACTERISTICS & RATINGS

Symbol	Parameter	Min.	Max.	Units	Duration	Notes
V_{CC}	Supply Voltage	-0.5	7.0	V	<1Hr	
MC	Modulus Control Input	-0.5	6.0	V	<1Hr	
V_{IN}	RF Input Voltage	-	2.5	V p-p	-	1
T_{OP}	Operating Temperature	-40	70	°C	-	
T_{STG}	Storage Temeperature	-55	150	°C	-	

Stress above those listed may cause permanent damage to the device. This is a stress rating only and fuctional operation of the device at these conditions, or at any other condition above those indicated in the operations section of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliablity.

NOTE1. Vin is the voltage measured differentially between RFINPUT and $\overline{\text{RFINPUT}}$.

ELECTRICAL CHARACTERISTICS

Unless otherwise stated, device performance is guaranteed over the following conditions:

Supply Voltage, Vcc 4.5V to 5.5V. Operating Temperature -40°C to +70°C

Parameter	Conditions	Min.	Typ.	Max.	Units	Notes
Supply Current	V_{CC} = 5.5V	-	14	20	mA	1
Input Voltage Range	80-150MHz	25	-	500	mVrms	2
	150-750MHz	15	-	500	mVrms	
	750-850MHz	22	-	500	mVrms	
	850-980MHz	50	-	500	mVrms	
MOD Control Input HIGH	Divide by 80	2.0	-	-	V	
MOD Control Input LOW	Divide by 81	-	-	1.0	V	
Output Voltage Swing	R_L = 10K, C_L = 10pF	-	1.0	-	V p-p	
Modulus Set-up Time	See Fig. 3		26	-	nS	3
Modulus Hold Time	See Fig. 3	$1/F_{IN}$	-	-	Sec	3
Modulus Release Time	See Fig. 3	-	$t_h + t_S$	-	Sec	3

N.B. All electrical testing is performed at room temperature

Notes:
1. Includes external bias resistors.
2. The device will operate to 10MHz with higher minimum input level.
3. These parameters are not tested.

Pin	Pin Name	Description
1	RF Input	Must be AC coupled to RF source with suitable capacitor.
2	Vcc	4.5V to 5.5V with a typical supply current of 14mA. Must be well decoupled to Gnd.
4	Output	1V peak to peak output swing driving 10pF and 10K
5	VEE	Negative supply pin
6	Modulus Control	Low input (1V) gives divide by 81 High input (2V) gives divide by /80
8	$\overline{\text{RF Input}}$	Must be decoupled with suitable capacitor to the reference supply of the input signal. This may be Vcc for VCOs.

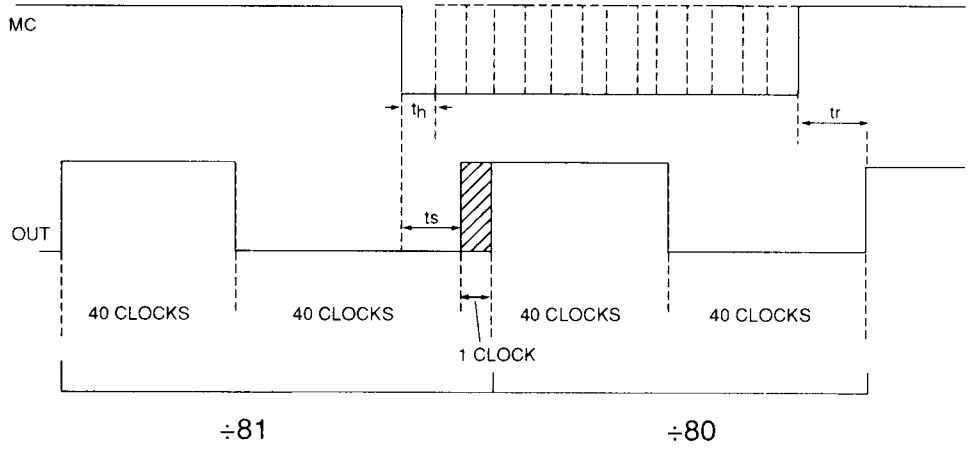
Table 1 : Pin Functions

OPERATING NOTES

1. The RF inputs are biased externally and coupled to a signal source with suitable capacitors.
2. The 4K7 RF input bias resistors must be matched to within ±1% of value.
3. The circuits will operate down to DC but slew rate must be better than 100V/µs.
4. The output stage is of an unusual design and is intended to interface with CMOS. External pull-up resistors or circuits should not be used.
5. This device is NOT suitable for driving TTL or its derivatives.

Pin 6	Division Ratio
L	81
H	80

Table 2 : Truth Table



t_s = The minimum time required between 'Modulus Control' going low and the next output rising edge, in order to ensure a P+1 modulus change.

t_h = The minimum time 'Modulus Control' must remain low to sustain the P + 1 modulus for that O/P period.

t_r = The minimum time allowed between 'Modulus Control' going high and the O/P rising edge in order to aviod a P + 1 modulus change in the following O/P cycle.

Figure 3 : Modulus Control Timing Diagram

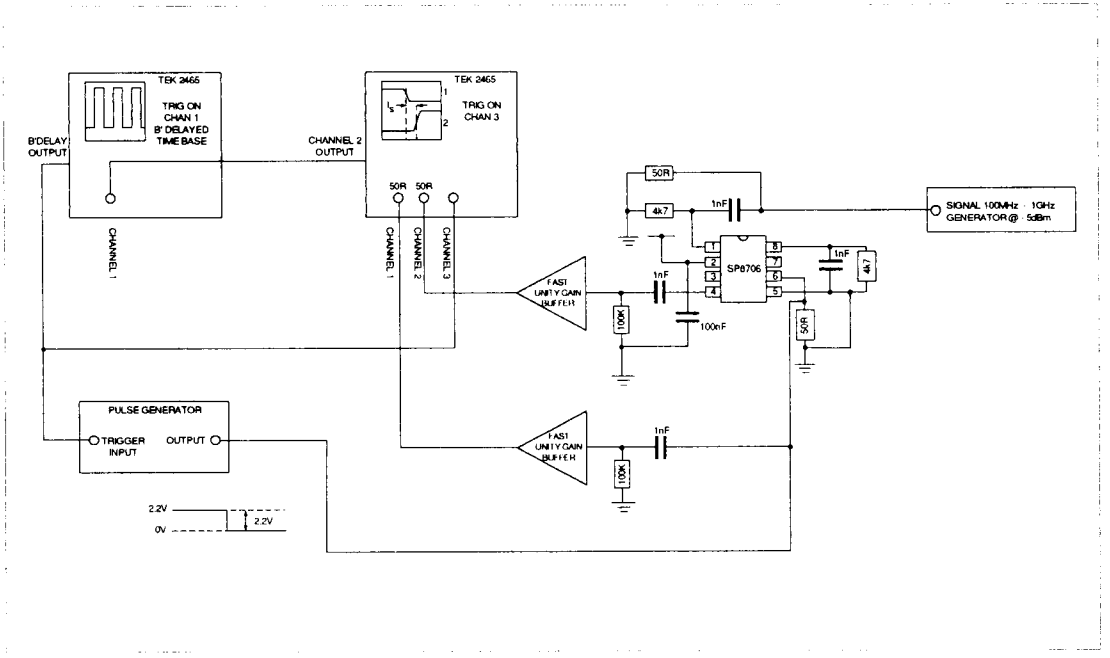


Figure 4 : Test circuit for setup and release time measurement

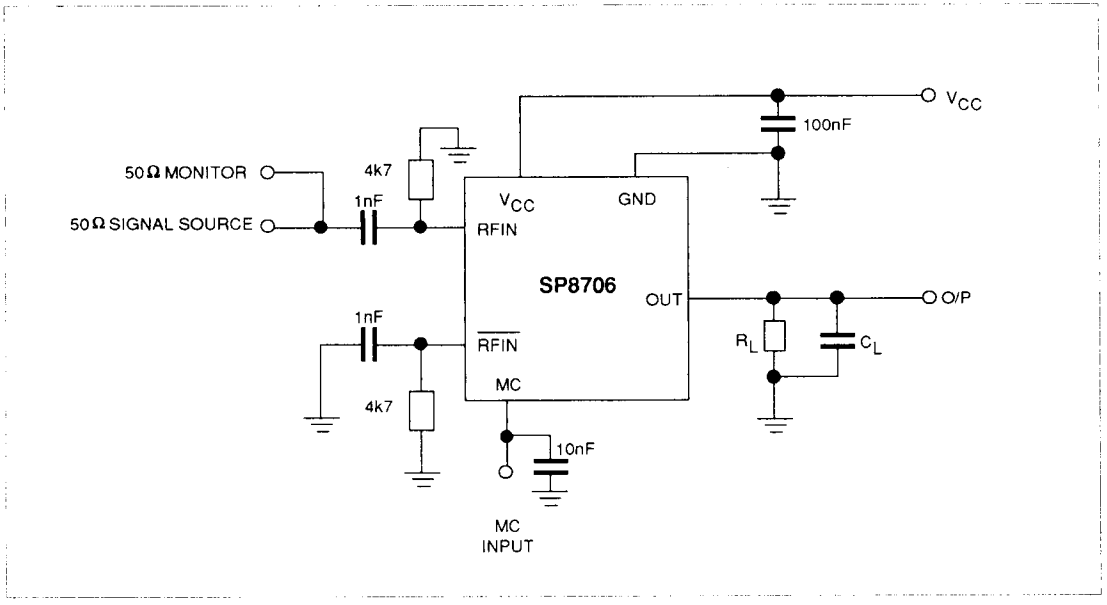
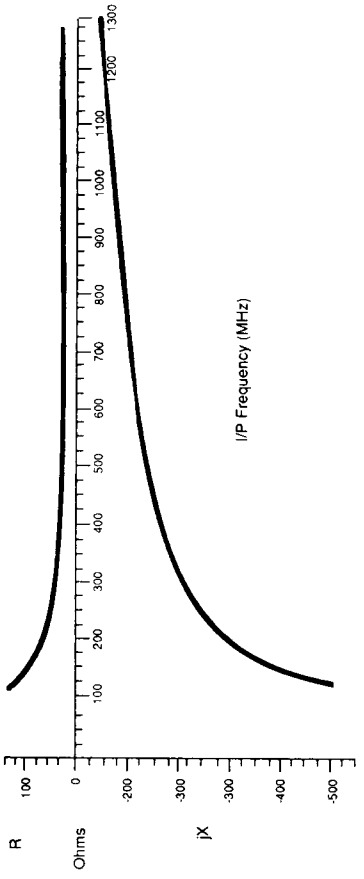


Figure 5 : Toggle Frequency Test Circuit



Freeuency (MHz)	R (Ω)	jX (Ω)
130	195	-351
156	133	-321
183	105	-281
209	78	-248
236	65	-223
262	55	-203
289	48	-185
315	42	-169
342	37	-156
368	33	-145
395	31	-136
421	27	-127
448	25	-119
474	23	-112
501	23	-106
527	21	-100
554	19	-94
580	18	-89
607	17	-85
633	17	-81
660	16	-77
686	15	-73
713	15	-70
739	14	-67
766	14	-64
792	13	-61
819	13	-58
845	13	-55
872	12	-53
898	12	-50
925	12	-48
951	12	-46
978	12	-44
1004	11	-42
1031	11	-39
1057	11	-37
1084	11	-36
1110	11	-34
1137	12	-33
1163	11	-31
1190	12	-29

Figure 6 : Typical Input impedance vs frequency

V_{CC} = 5.0V	Plot normalised from 50R
START	0.1300GHz
STOP	1.1900GHz
MARKER ↓	0.98GHz
Z_{IN} at 0.98GHz	12.15Ω - -j44.02Ω (de normalised)

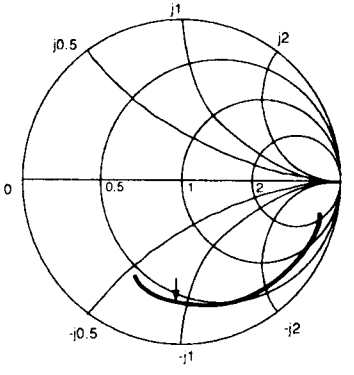


Figure 7 : SP8706MP Smith Chart S_{11} Measurement