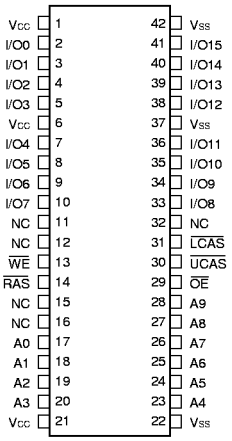
1Mx16 CMOS FPM Dynamic RAM

*PRELIMINARY**

PIN CONFIGURATION
TOP VIEW



PIN DESCRIPTION

A_{0-9}	Address Inputs
I/O_{0-15}	Data Input/Outputs
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
$\overline{RAS}$	Row Address Strobe
$\overline{UCAS}$	Upper Column Adress Strobe
$\overline{LCAS}$	Lower Column Adress Strobe
V_{CC}	+5.0V Power Supply
V_{SS}	Ground
NC	Not Connected

PLASTIC PLUS™ FEATURES

- Fast Access Time (t_{RAC}): 70ns
- Power Supply: 5V ±0.5V
- Packaging
  - 42 Lead Plastic Surface-Mount SOJ (TJ)
- Industrial and Military Temperature Ranges
- Three-State Unlatched Output
- Fast Page Mode
- TTL-Compatible Inputs and Outputs
- $\overline{RAS}$-Only Refresh
- $\overline{xCAS}$ Before $\overline{RAS}$ Refresh
- Hidden Refresh
- 1024 Cycle Refresh in 16ms
- Low Power Dissipation
- Long Refresh Period Option

* *This data sheet describes a product under development, not fully characterized, and is subject to changewithout notice.*

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Operating Temperature	T_A	-55	+125	°C
Storage Temperature	T_{STG}	-65	+150	°C
Short Circuit Output Current	I_{OS}		50	mA
Power Dissipation	P_T		1	W
Supply Voltage Range	V_{CC}	-1.0	7.0	V
Voltage Range on any Pin*	V_T	-1.0	7.0	V

Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stess ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. exposed to absolute-maximum-rated conditions for extended periods may affect device reliability.
* All voltage values are with respect to Vss.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{CC}	4.5	5.5	V
Input High Voltage	V_{IH}	2.4		V
Input Low Voltage*	V_{IL}		+0.8	V
Operating Temp. (Mil.)	T_A	-55	+125	°C
Operating Temp. (Ind.)	T_A	-40	+85	°C

* The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used for logic-voltage levels only.

CAPACITANCE

(T_A = 25°C)

Parameter	Symbol	Max	Unit
A_{0-9} Input Capacitance	$C_{I(A)}$	10	pF
$\overline{RAS}$ and $\overline{CAS}$ Input Capacitance	$C_{I(RC)}$	10	pF
$\overline{OE}$ Input Capacitance	$C_{I(OE)}$	10	pF
$\overline{WE}$ Input Capacitance	$C_{I(WE)}$	10	pF
Output Capacitance	C_O	15	pF

This parameter is guaranteed by design but not tested.

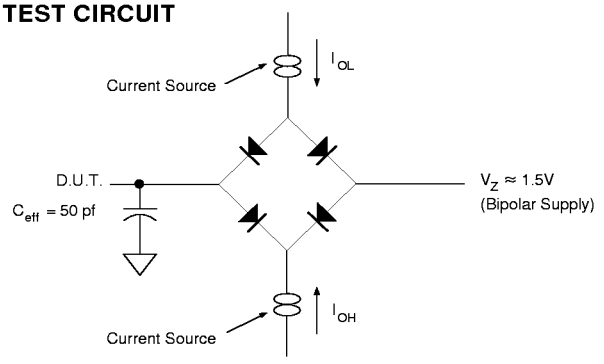
DC CHARACTERISTICS

(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -55°C to +125°C)

Parameter	Test Condition	Symbol	70 Min	70 Max	Units
High Level Output Voltage	I_{OH} = -5mA	V_{OH}	2.4		V
Low Level Output Voltage	I_{OL} = 4.2mA	V_{OL}		0.4	V
Input Current (Leakage)	V_I = 0V to +6.5V All others = 0V to Vcc	I_I		10	µA
Output current (Leakage)	VO = 0V to Vcc, CAS high	I_O		10	µA
Read or Write Cycle Current (1,2)	Vcc = 5.5V, minimum cycle	I_{CC1}		190	mA
Standby Current	V_{IH} = 2.4V (TTL), After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high	I_{CC2}		2	mA
	V_{IH} = Vcc - 0.05V (CMOS), After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high	I_{CC2}		1	mA
Average Page Current (2)	$\overline{RAS}$ low, $\overline{CAS}$ cycling	I_{CC4}		100	mA

NOTES:
1. Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}.
2. Measured with a maximum of one address change while $\overline{CAS}$ = V_{IH}.

AC TEST CIRCUIT



AC TEST CONDITIONS

Parameter	Typ	Unit
Input Pulse Levels	V_{IL} = 0, V_{IH} = 3.0	V
Input Rise and Fall	5	ns
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

NOTES:
V_Z is programmable from -2V to +7V.
I_{OL} & I_{OH} programmable from 0 to 16mA.
Tester Impedance Z_0 = 75 Ω.
V_Z is typically the midpoint of V_{OH} and V_{OL}.
I_{OL} & I_{OH} are adjusted to simulate a typical resistive load circuit.
ATE tester includes jig capacitance.

AC CHARACTERISTICS*

(T_A = -55°C to +125°C, V_{CC} = 5.0V ±10%)

Parameter	Symbol	-70		Units
		Min	Max	
Column-Address Access Time	t_{AA}		35	ns
$\overline{CAS}$ Low Access Time	t_{CAC}		18	ns
Column Precharge Access Time	t_{CPA}		40	ns
$\overline{RAS}$ Low Access Time	t_{RAC}		70	ns
$\overline{OE}$ Low Access Time	t_{OEA}		18	ns
Output Disable Time after $\overline{CAS}$ High (1)	t_{OFF}	0	18	ns
Output Disable Time after $\overline{OE}$ High (1)	t_{OEZ}	0	18	ns

* Valid data is presented at the outputs after all access times are satisfied but can go from the high-impedance state to an invalid-data state prior to the specified access times as the outputs are driven when $\overline{CAS}$ goes low.
1. t_{OFF} and t_{OEZ} are specified when the outputs are no longer driven. The outputs are disabled by bringing either $\overline{OE}$ or $\overline{CAS}$ high.

AC CHARACTERISTICS

(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -55°C to +125°C)

Parameter	Symbol	-70		Units
		Min	Max	
Cycle Time, Read or Write Random (1)	t_{RC}	130		ns
Cycle Time, Read-Write (1)	t_{RWC}	181		ns
Cycle Time, Page Mode Read or Write (1,2)	t_{PC}	45		ns
Cycle Time, Page Mode Read-Write (1)	t_{PRWC}	96		ns
Pulse Duration, $\overline{RAS}$ Low Page Mode (3)	t_{RASP}	70	100,000	ns
Pulse Duration, $\overline{RAS}$ Low Nonpage Mode (3)	t_{RAS}	70	10,000	ns
Pulse Duration, $\overline{CAS}$ Low (4)	t_{CAS}	18	10,000	ns
Pulse Duration, $\overline{CAS}$ High	t_{CP}	10		ns
Pulse Duration, $\overline{RAS}$ High (Precharge)	t_{RP}	50		ns
Pulse Duration, $\overline{WE}$ Low	t_{WP}	10		ns
Setup Time, Column Address before $\overline{CAS}$ Low	t_{ASC}	0		ns
Setup Time, Row Address before $\overline{RAS}$ Low	t_{ASR}	0		ns
Setup Time, Data (5)	t_{DS}	0		ns
Setup Time, $\overline{WE}$ High before $\overline{CAS}$ Low	t_{RCS}	0		ns
Setup Time, $\overline{WE}$ Low before $\overline{CAS}$ High	t_{CWL}	18		ns
Setup Time, $\overline{WE}$ Low before $\overline{RAS}$ High	t_{RWL}	18		ns
Setup Time, $\overline{WE}$ Low before $\overline{CAS}$ Low (early-write operation only)	t_{WCS}	0		ns
Setup Time, $\overline{WE}$ High before $\overline{RAS}$ Low (CBR refresh only)	t_{WRP}	10		ns
Hold Time, Column Address after $\overline{CAS}$ Low	t_{CAH}	15		ns
Hold Time, Data (5)	t_{DH}	15		ns
Hold Time, Row Address after $\overline{RAS}$ Low	t_{RAH}	10		ns
Hold Time, $\overline{WE}$ High after $\overline{CAS}$ High (6)	t_{RCH}	0		ns
Hold Time, $\overline{WE}$ High after $\overline{RAS}$ High (6)	t_{RRH}	0		ns

1. All cycle times assume t_T = 5ns, reference to V_{IH} (min) and V_{IL} (max).
2. To assume t_{PC} min, t_{ASC} should be ≥ t_{CP}.
3. In read-write cycle, t_{RWD} and t_{RWL} must be observed.
4. In read-write cycle, t_{CWD} and t_{CWL} must be observed.
5. Referenced to the later of xCAS or $\overline{WE}$ in write operations.
6. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

AC CHARACTERISTICS

(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -55°C to +125°C)

Parameter	Symbol	-70		Units
		Min	Max	
$\overline{WE}$ Low before $\overline{CAS}$ Low Hold Time (early-write operation only)	t_{WCH}	15		ns
$\overline{WE}$ High after $\overline{RAS}$ Low Hold Time (CBR refresh only)	t_{WRH}	10		ns
$\overline{OE}$ Command Hold Time	t_{OEH}	18		ns
$\overline{RAS}$ Referenced to $\overline{OE}$ Hold Time	t_{ROH}	10		ns
$\overline{RAS}$ High from $\overline{CAS}$ Precharge Hold Time	t_{RHCP}	40		ns
Column Address to $\overline{WE}$ Low Delay Time (read-write operation only)	t_{AWD}	63		ns
$\overline{RAS}$ Low to $\overline{CAS}$ High Delay Time (CBR refresh only)	t_{CHR}	10		ns
$\overline{CAS}$ High to $\overline{RAS}$ Low Delay Time	t_{CRP}	5		ns
$\overline{RAS}$ Low to $\overline{CAS}$ High Delay Time	t_{CSH}	70		ns
$\overline{CAS}$ Low to $\overline{RAS}$ Low Delay Time (CBR refresh only)	t_{CSR}	5		ns
$\overline{CAS}$ Low to $\overline{WE}$ Low Delay Time (read-write operation only)	t_{CWD}	46		ns
$\overline{OE}$ to Data Delay Time	t_{OED}	18		ns
$\overline{RAS}$ Low to Column Address Delay Time (1)	t_{RAD}	15	35	ns
Column Address to $\overline{RAS}$ High Delay Time	t_{RAL}	35		ns
Column Address to $\overline{CAS}$ High Delay Time	t_{CAL}	35		ns
$\overline{RAS}$ Low to $\overline{CAS}$ Low Delay Time (1)	t_{RCD}	20	52	ns
$\overline{RAS}$ High to $\overline{CAS}$ Low Delay Time	t_{RPC}	0		ns
$\overline{CAS}$ Low to $\overline{RAS}$ High Delay Time	t_{RSH}	18		ns
$\overline{RAS}$ Low to $\overline{WE}$ Low Delay Time (read-write operation only)	t_{RWD}	98		ns
$\overline{WE}$ Low after $\overline{CAS}$ Precharge Delay Time (read-write operation only)	t_{CPW}	63		ns
Refresh Time Interval	t_{REF}		16	ms
Transition time (2)	t_T			

1. The maximum value is specified only to assure access time
2. Transition times (rise and fall) for $\overline{RAS}$ and $\overline{xCAS}$ are to be a minimum of 3ns and a maximum of 30ns.

OPERATIONS

DUAL $\overline{CAS}$

Two $\overline{CAS}$ pins ($\overline{LCAS}$ and $\overline{UCAS}$) are provided to give independent control of the 16 data-I/O pins (I/O0-15), with $\overline{LCAS}$ corresponding to I/O0-7 and $\overline{UCAS}$ corresponding to I/O8-15. For read or write cycles, the column address is latched on the first $\overline{xCAS}$ falling edge. Each $\overline{xCAS}$ going low enables its corresponding I/Ox pin with data associated with the column address latched on the first falling $\overline{xCAS}$ edge. All address setup and hold parameters are referenced to the first falling $\overline{xCAS}$ edge. The delay time from $\overline{xCAS}$ low to valid data out (see parameter t_{CAC}) is measured form each individual $\overline{xCAS}$ to its corresponding I/Ox pin.

In order to latch in a new column address, both $\overline{xCAS}$ pins must be brought high. The column-precharge time (see parameter t_{CP}) is measured from the last $\overline{xCAS}$ rising edge to the first $\overline{xCAS}$ falling edge of the new cycle. Keeping a column address valid while toggling $\overline{xCAS}$ requires a minimum setup time, t_{CLCH}. During t_{CLCH}, at least one $\overline{xCAS}$ must be brought low before the other $\overline{xCAS}$ is taken high.

For early-write cycles, the data is latched on the first $\overline{xCAS}$ falling edge. Only the I/Os that have the corresponding $\overline{xCAS}$ low are written into. Each $\overline{xCAS}$ must meet t_{CAS} minimum in order to ensure writing into the storage cell. To latch a new address and new data, all $\overline{xCAS}$ pins must be high and meet t_{CP}.

PAGE MODE

Page-mode operation allows faster memory access by keeping the same row address while selecting random column addresses. The time for row-address setup and hold and address multiplex is eliminated. The maximum number of columns that can be accessed is determined by the maximum $\overline{RAS}$ low time and the $\overline{xCAS}$ page-mode cycle time used. With minimum $\overline{xCAS}$ page-cycle time, all columns can be accessed without intervening $\overline{RAS}$ cycles.

Unlike conventional page-mode DRAMs, the column address buffers in this device are activated on the falling edge of $\overline{RAS}$. The buffers act as transparent or flow-through latches while $\overline{xCAS}$ is high. The falling edge of the first $\overline{xCAS}$ latches the column addresses. This feature allows the devices to operate at a higher data bandwidth than conventional page-mode parts because data retrieval begins as soon as the column address is valid rather than when $\overline{xCAS}$ transitions low. This performance improvement is referred to as enhanced page mode. A valid column address may be presented immediately after t_{RAH} (row-address hold time) has been satisfied, usually well in advance of the falling edge of $\overline{xCAS}$. In this case, data is obtained after t_{CAC} maximum (access time from $\overline{xCAS}$ low) if t_{AA} maximum (access time from column address) has been satisfied. In the event that column addresses for the next page cycle are valid at the time $\overline{xCAS}$ goes high, minimum access time for the next cycle is determined by t_{CPA} (access time from rising edge of the last $\overline{xCAS}$).

ADDRESS: A0-9

Twenty address bits are required to decode 1 of 1048576 storage cell locations. For the WPD1M16-70TJX, 10 row-address bits are set up on A0 through A9 and latched onto the chip by $\overline{RAS}$. Ten, column-address bits are set up on A0 through A9 and latched onto the chip by the first $\overline{xCAS}$. All addresses must be stable on or before the falling edge of $\overline{RAS}$ and $\overline{xCAS}$. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{xCAS}$ is used as a chip select, activating its corresponding output buffer and latching the address bits into the column-address buffers.

WRITE ENABLE ($\overline{WE}$)

The read or write mode is selected through $\overline{WE}$. A logic high on $\overline{WE}$ selects the read mode and a logic low selects the write mode. The data inputs are disabled when the read mode is selected. When $\overline{WE}$ goes low prior to $\overline{xCAS}$ (early write), data out remains in the high-impedance state for the entire cycle, permitting a write operation with $\overline{OE}$ grounded.

DATA IN (I/O0-15)

Data is written during a write or read-modify-write cycle. Depending on the mode of operation, the falling edge of $\overline{xCAS}$ or $\overline{WE}$ strobes data into the on-chip data latch. In an early-write cycle, $\overline{WE}$ is brought low prior to $\overline{xCAS}$ and the data Is strobed in by the first occurring $\overline{xCAS}$ with setup and hold times referenced to this signal. In a delayed-write or read-modify-write cycle, $\overline{xCAS}$ is already low and the data is strobed in by $\overline{WE}$ with setup and hold times referenced to this signal. In a delayed-write or read-modify-write cycle, $\overline{OE}$ must be high to bring the output buffers to the high-impedance state prior to impressing data on the I/O lines.

DATA OUT (I/O0-15)

Data out is the same polarity as data in. The output is in the high-impedance (floating) state until $\overline{xCAS}$ and $\overline{OE}$ are brought low. In a read cycle, the output becomes valid after the access time interval t_{CAC} (which begins with the negative transition of $\overline{xCAS}$) as long as t_{RAC} and t_{AA} are satisfied.

OUTPUT ENABLE ($\overline{OE}$)*

$\overline{OE}$ controls the impedance of the output buffers. When $\overline{OE}$ is high, the buffers remain in the high-impedance state. Bringing $\overline{OE}$ low during a normal cycle activates the output buffers, putting them in the low-impedance state. It is necessary for both $\overline{RAS}$ and $\overline{xCAS}$ to be brought low for the output butters to go into the low-impedance state, and they remain in the low-impedance state until either $\overline{OE}$ or $\overline{xCAS}$ is brought high.

* *Output Enable can be held low during write cycles.*

$\overline{RAS}$-ONLY REFRESH

A refresh operation must be performed at least once every 16 ms (128 ms for long refresh periods) to retain data. This can be achieved by strobing each of the 1024 rows (A_{0-9}). A normal read or write cycle refreshes all bits in each row that is selected. A $\overline{RAS}$-only operation can be used by holding both $\overline{xCAS}$ at the high (inactive) level, conserving power as the output buffers remain in the high-impedance state. Externally generated addresses must be used for a $\overline{RAS}$-only refresh.

HIDDEN REFRESH

Hidden refresh can be performed while maintaining valid data at the output pin. This is accomplished by holding $\overline{xCAS}$ at V_{IL} after a read operation and cycling $\overline{RAS}$ after a specified precharge period, similar to a $\overline{RAS}$-only refresh cycle. The external address is ignored and the refresh address is generated internally.

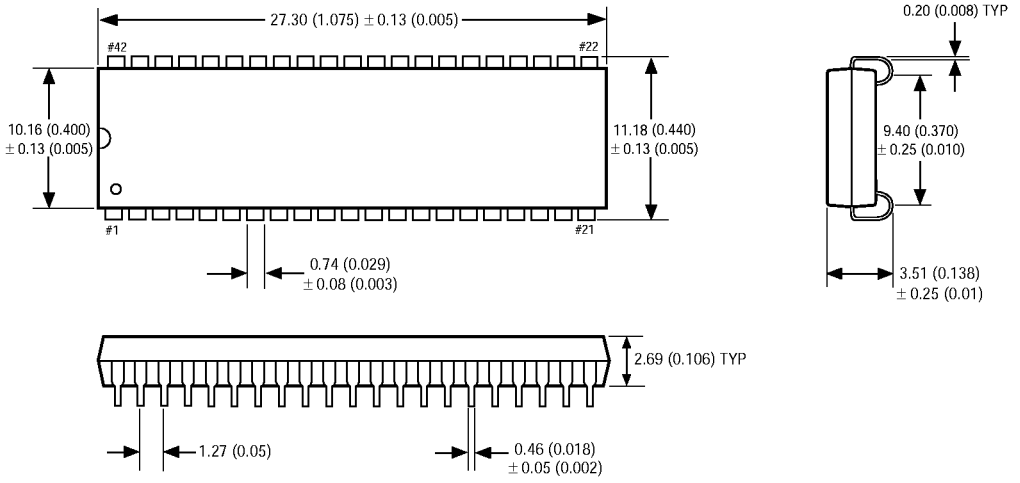
$\overline{xCAS}$-BEFORE-$\overline{RAS}$ ($\overline{xCBR}$) REFRESH

$\overline{xCBR}$ refresh is utilized by bringing at least one $\overline{xCAS}$ low earlier than $\overline{RAS}$ (see parameter t_{CSR}) and holding it low after $\overline{RAS}$ fails (see parameter t_{CHR}). For succesive $\overline{xCBR}$ refresh cycles, $\overline{xCAS}$ can remain low while cycling $\overline{RAS}$. The external address is ignored and the refresh address is generated internally.

POWER UP

To achieve proper device operation, an initial pause of 200µs followed by a minimum of eight initialization cycles is required after power up to full Vcc level. These eight initialization cycles must include at least one refresh ($\overline{RAS}$-only or $\overline{xCBR}$) cycle.

PACKAGE DIMENSION: 42 LEAD SOJ, (TJ)



TOLERANCES: ±0.13 (0.005) UNLESS OTHERWISE SPECIFIED
ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

ORDERING INFORMATION

W P D 1M 16 X - 70 TJ X

DEVICE GRADE:
- M = Military Temperature -55°C to +125°C
- I = Industrial Temperature -40°C to +85°C

PACKAGE:
TJ = 42 Lead Plastic Surface Mount SOJ

ACCESS TIME (ns)

IMPROVEMENT MARK
- B = Burn-in
- T = Temperature Cycle
- C = Burn-in and Temp Cycle

ORGANIZATION, 1M x 16

DRAM

PLASTIC PLUS™

WHITE MICROELECTRONICS