M-984 Special Tone & Call Progress Tone Detector

The Teltone® Special Tone and Call Progress Tone Detector is a monolithic integrated circuit designed to provide reliable detection of many common telephone network status signals. In particular, it detects the signals known as special information tones (SITs) or error tones as defined by the CCITT, and single tones often used as dial tone, audible ringing, and other general progress indications. The M-984 uses CMOS switched capacitor filters and a crystal time base to achieve the high stability and accuracy specified. Each tone detection window has an associated output pin, which can be placed in a high impedance state for use with time-share microcomputer bus applications.

Features

- Detects single-frequency tones used for error indication and call progress in telephone systems
- Provides detection windows for:
  400/425 Hz (Call Progress)
  950 Hz (Special and error indication)
  1400 Hz (Special and error indication)
  1800 Hz (Special and error indication)
- Separate 3-state outputs for each tone window
- 3.58 MHz crystal time base
- Auxiliary 3.58 MHz clock output
- CMOS with switched capacitor technology
- Compact 14-pin DIP package
- single 4 VDC supply
- 0 to -30 dBm detect range

Features

- Automatic dialers
- Modems
- Telecom text equipment
- Telephone traffic measurement
- Service evaluation
- Billing equipment

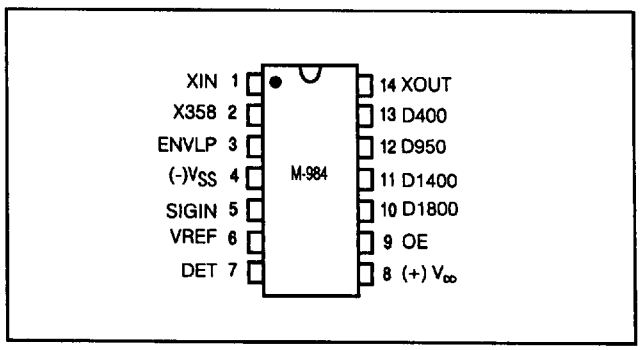

Figure 1 Pin Diagram

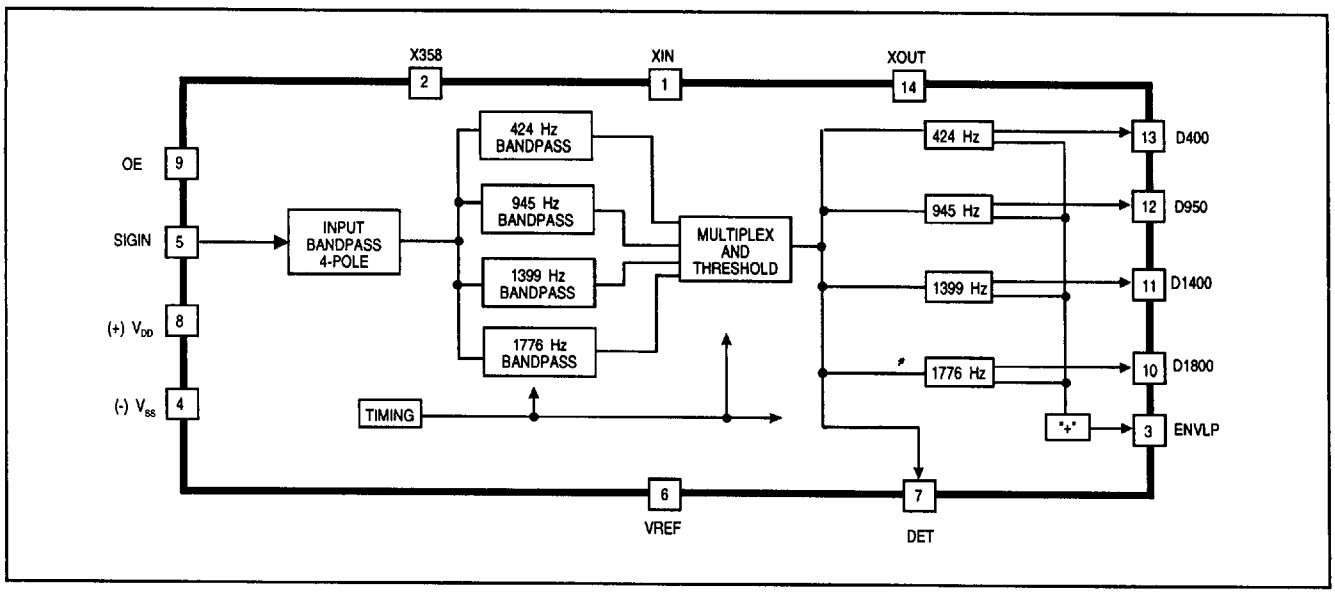

Figure 2 Block Diagram

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Table 1 Pin Functions

PIN	Desc	FUNCTION
1	XIN	Crystal Connection — 3.58 MHz crystal across these pins will produce the timebase needed for proper operation of the M-984. An external clock signal may be fed to XIN providing the clock signal has a duty cycle of 50 ± 10% and comes within 0.2 volts of the supply rails. XOUT remains unconnected when an external clock is used. When used with a crystal, a 1 megohm resistor should be connected across XIN and XOUT.
14	XOUT	
2	X358	A buffered output pin. A 3.58 MHz clock signal is available for use in other circuits as a timebase. Leave open when unused.
3	ENVLP	The strobe pin is a common detection indicator for the four detect pins. Simply put, the strobe is a logical "OR" of the active detect circuits for each of the four windows, though there is a delay provided to permit strobe to latch the first active detect pin. Strobe is not 3-state controlled.
4	V_{SS},	The power supply pins, VDD being the most positive. Commonly, V_{DD} is at 5 volts, while VSS is at ground.
8	V_{DD}	
5	SIGIN	The signal input pin, for analog signals referenced to V_{SS}. The input voltage range is between V_{DD} and V_{SS}, and an input impedance of about 80 kohms is presented.
6	VREF	VREF is a vias voltage generated in the chip for use in external analog circuits, such as actrive filters and AC-coupled buffers. Leave open when unused.
7	DET	This is a general digital output pin not designated for use in application. The combined output of the four bandpass window filters after the signal has beenconvereted to square wave and before the digital timing circuits appears on the pin. Leave open.
9	OE	The 3-state control pin. OE places the DET pins in the active mode when at logic "1". When at logic "0," OE causes the DET outputs to appear as high impedance. Should be tied to logic "1" when the M-984 is not used in a time-shared bus application.
10	D1800	The detect outputs associated with each window. 3-state control is available through use of the OE pin 9. Timing is shown in the timing diagram.
11	1400	
12	D950	
13	D400	

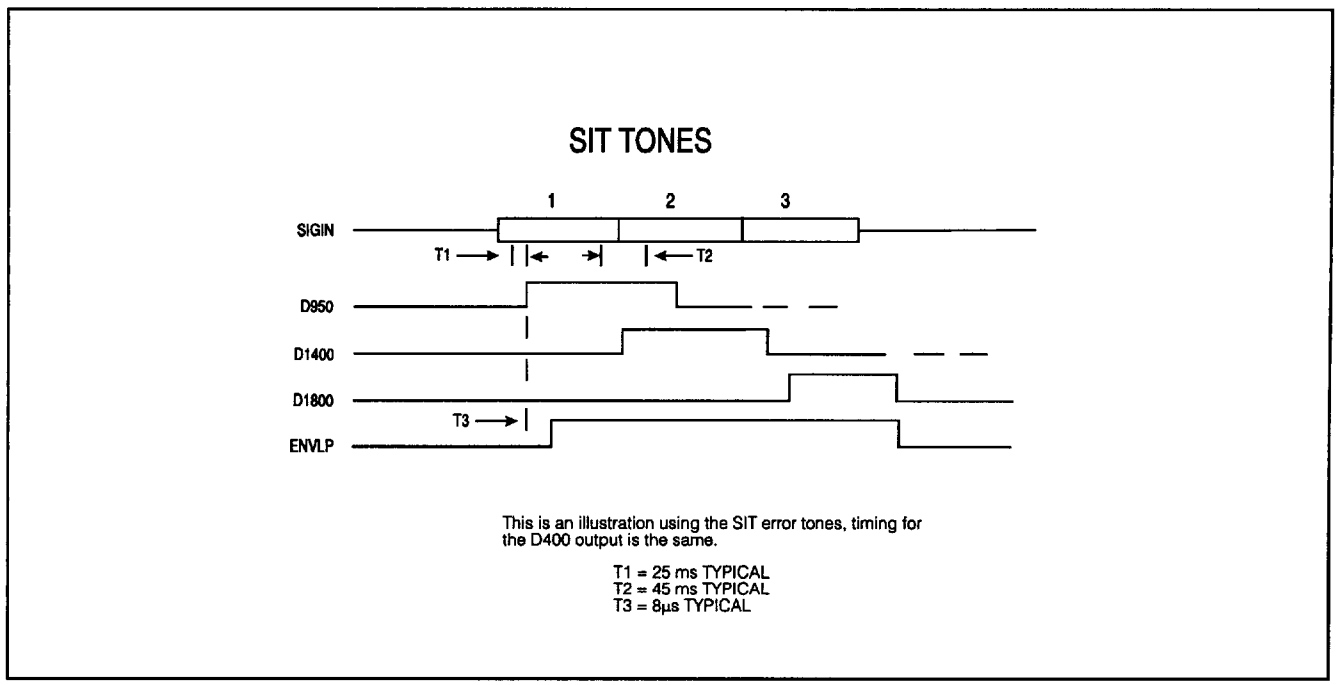

Figure 3 Timing Diagram

Table 2 Specifications

	PARAMETER	MIN	TYPICAL	MAX	UNITS	NOTES
Basic Operation	Power Supply	4.5	-	5.5	volts	
		-	4	30	mA	5.0 VDC
		-	-	20	mV	Noise Limit
	Input Spectrum	-	-	28	kHz	
Signal Detection	Level	-30	-	0	dBm	
	Duration	50	-	-	ms	
	Bridge Time	15	35	-	ms	
	S/N Ration	16	-	-	dB	
	Drop Out	-	-	50	ms	
Signal Rejection	Level (In-Band)	-	-35	-40	dBm	200-3400 Hz
	(Other)	-	-	0	dBm	1% outside limit
Logic Conventions	V (Out Low)	-	-	0.5	volts	1.0 mA Sink
(except X358)	V (Out High)	VDD-0.5	-	-	volts	0.5 mA Source
	V (In Low)	-	-	0.5	volts	
	V (In High)	VDD-2.0	-	-	volts	
Clock Buffer (X358)	V (Out Low)	-	-	0.5	volts	1.0 mA, 20 pF
	V (Out High)	VDD-0.5	-	-	volts	1.0 mA, 20 pF
	Duty Cycle	40	-	60	percent	C = 20 pF
3-State Operation	Enable Time	-	200	250	ns	C = 50 pF
	Disable Time	-	200	250	ns	R = 100 kohm

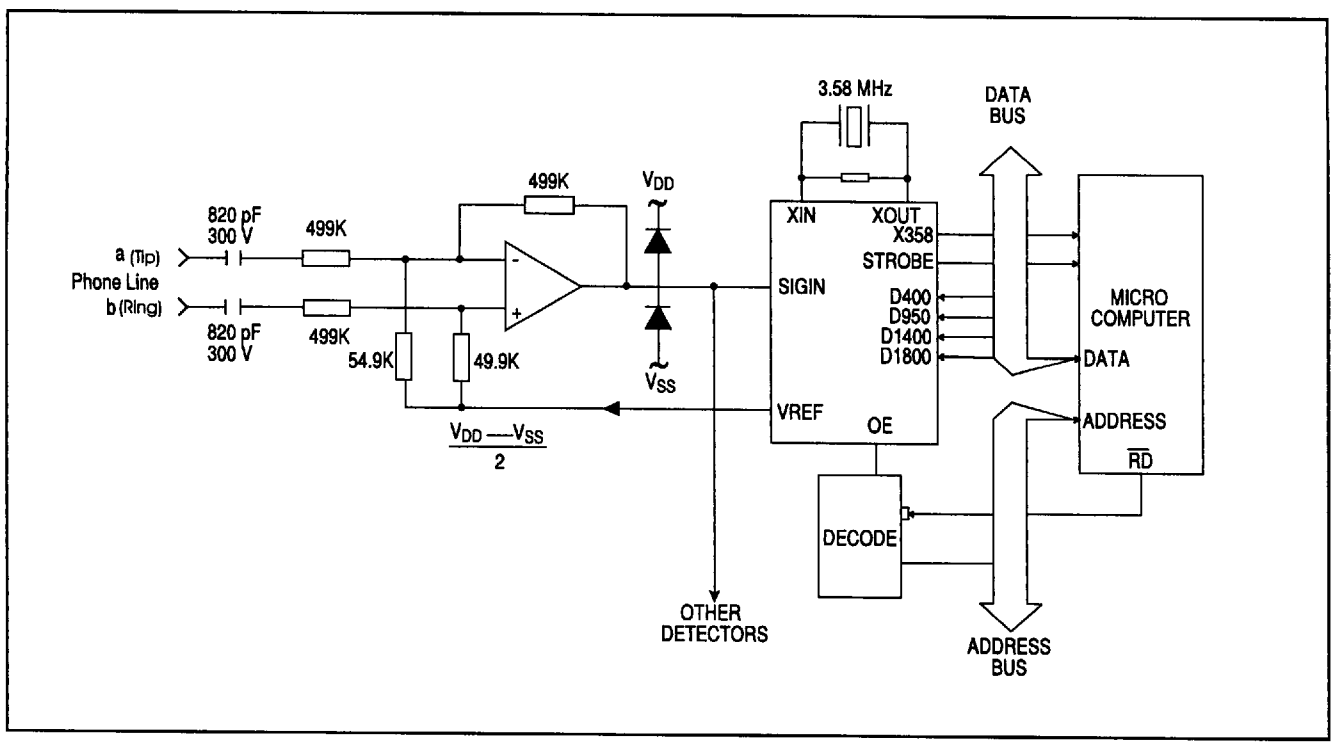

Figure 4 Typical Application

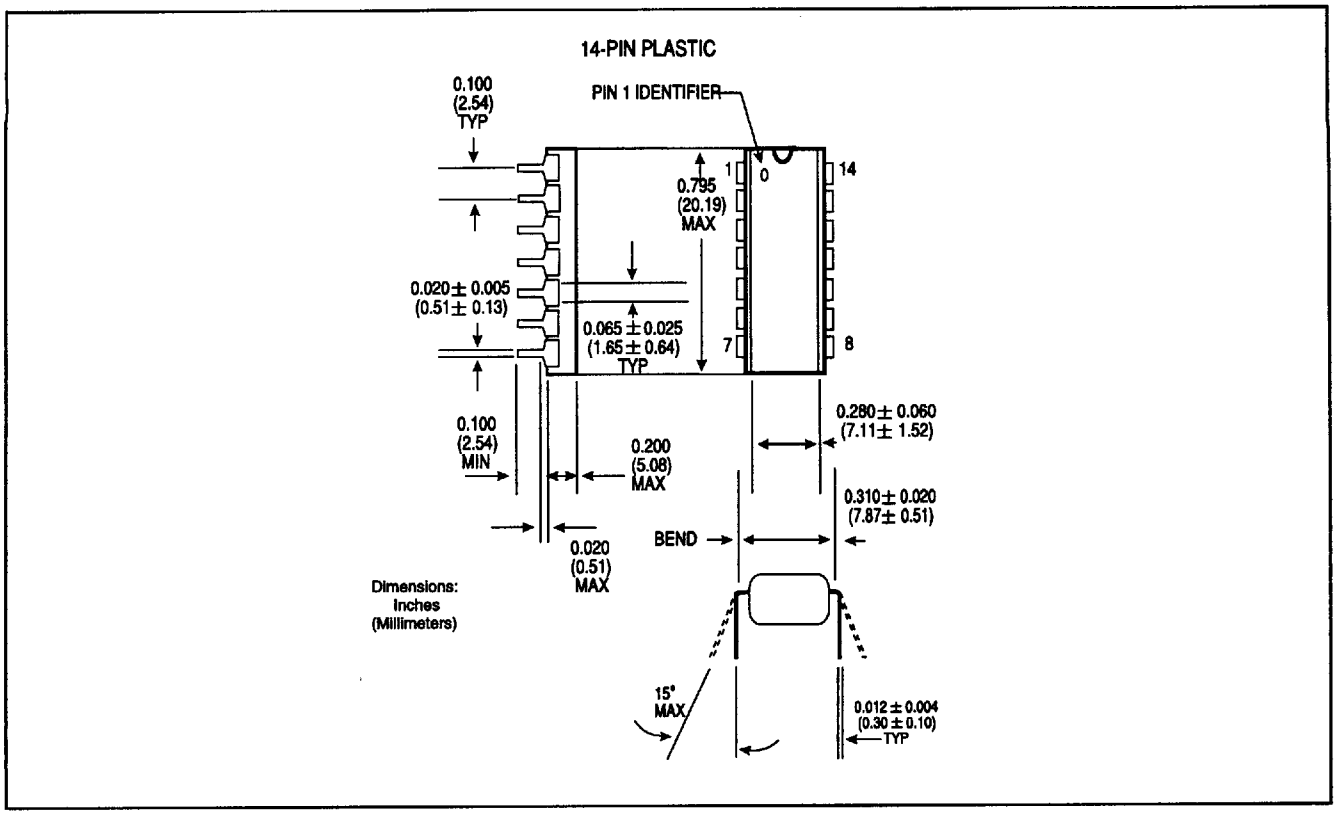

Figure 5 Package Dimensions

Table 3 Detector Frequency Windows

WINDOW	PIN	LOW REJECT	LOW ACCEPT	HIGH ACCEPT	HIGH REJECT
1	D400	363	392	459	493
2	D950	845	895	1005	1060
3	D1400	1290	1343	1457	1512
4	D1800	1675	1741	1812	1882

Table 4 Absolute Maximum Ratings

DC Supply Voltage	7.0V
Voltage on Any Pin	V_{DD} + 0.5 to V_{SS} - 0.5V
Storage Temperature Range	0° C to +7-0 °C
Operating Temperature Range	-40° C to +85° C
Lead Soldering Tempearture	260° C for 5 seconds

Ordering Information

M-984	14-pin plastic DIP