

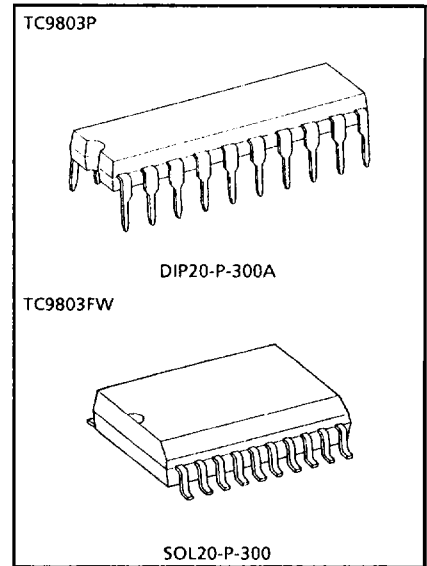
TC9803P, TC9803FW

TC9803 is a CMOS programmable logic device (PLD) based on EEPROM cells. Designed using Toshiba's original technology, this device features low power dissipation and inputs that are compatible with TTL, NMOS, and CMOS output voltage levels.

It has both AND and OR arrays which the user can program like a field programmable logic array (FPLA). TC9803 is a high-speed version of TC9801. Its pin connections and functions are the same as those of TC9801.

FEATURES

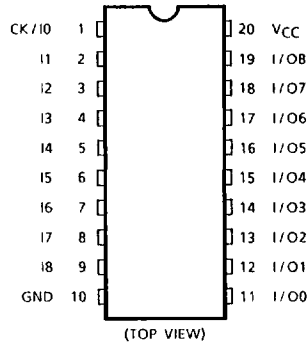
- Architecture 41 AND terms
9 OR terms
8 macro cells with registers
- Security cell Protection of proprietary information
- Signature word 41 bits for user ID code or inventory control
- High speed operation t_{pd} (input-output) = 23ns (Typ.)
 t_{co} (clock-output) = 10ns (Typ.)
- Low power dissipation I_{CC} (standby) = 4 μ A (max. @25°C)
- Compatible with TTL inputs V_{IH} = 2V (min.) V_{IL} = 0.8V (max.)
- Package 20-pin plastic DIP (TC9803P)
20-pin plastic SOL (TC9803FW)



Weight DIP20-P-300A : 1.30g (Typ.)
SOL20-P-300 : 0.46g (Typ.)

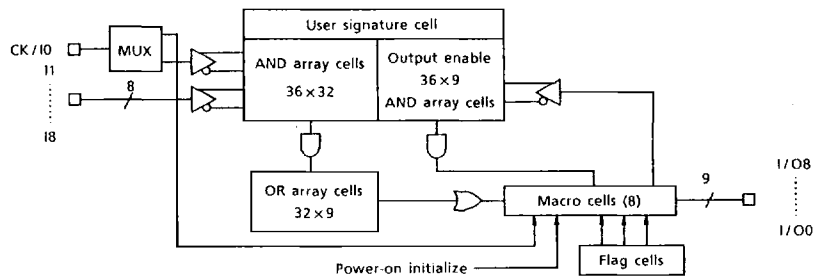
TC9803P, TC98093W

PIN NAMES & FUNCTIONS

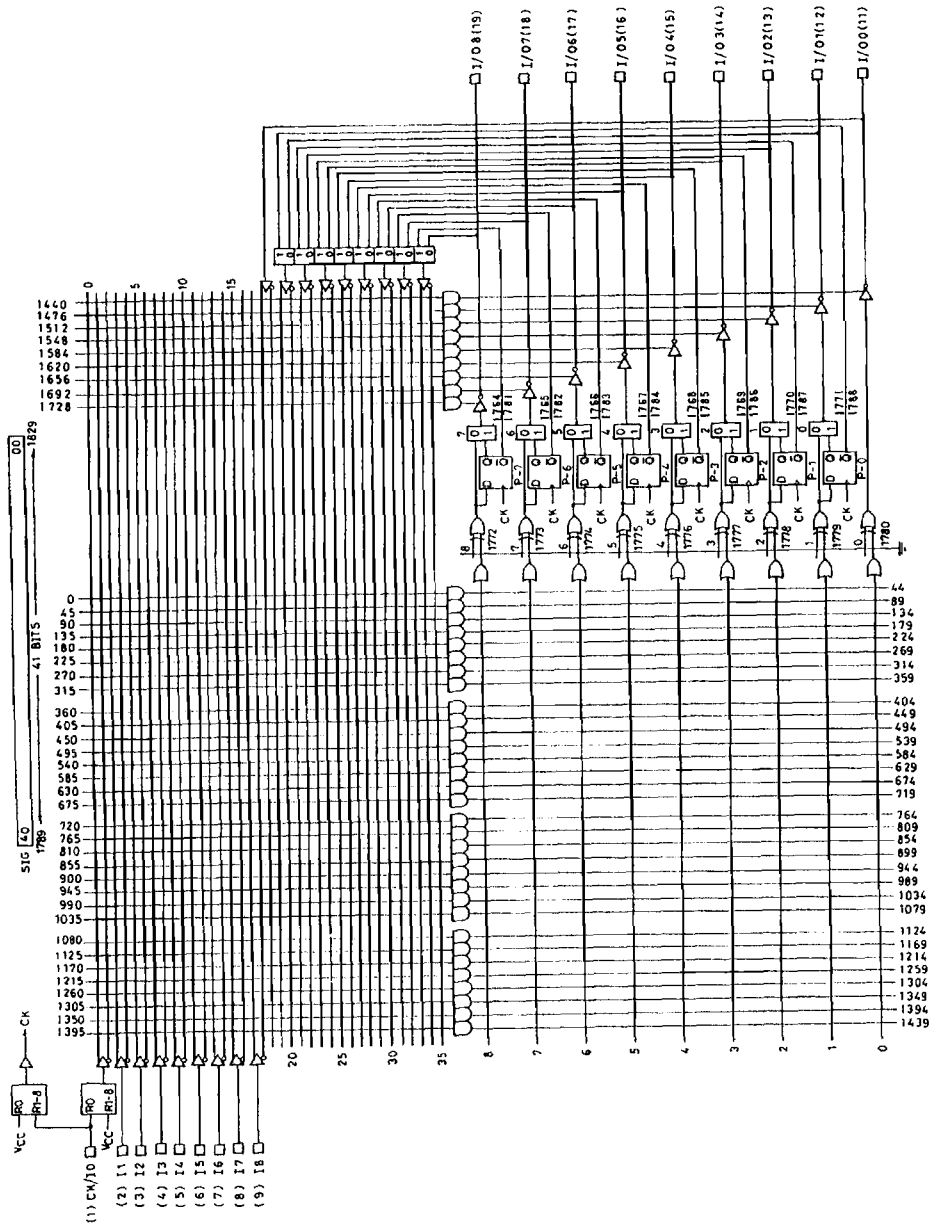


- CK/I0 Clock input (when register is selected)
- I1~I8 Dedicated to input
- I/O0 Input / Output (without register output)
- I/O1~I/O8 Input / Output (with register output)

FUNCTION DIAGRAM



LOGIC DIAGRAM



ARCHITECTURE

1. MEMORY CELLS

Programmable memory cells are divided into the following five types : AND array, OR array, output control array, flag, and user signature.

Setting program data to 1 disconnects signals to an AND/OR array : setting to 0 connects.

(1) AND array (36×32)

Total of 41 product terms (32 AND terms and 9 output control terms)

(2) OR array (32×9)

32 AND terms input to 9 OR terms.

(3) Output control array (36×9)

Output from this array enables CMOS output (I/O0~I/O8).

(4) Flag cell

- A. Output polarity selection cell 9 bits
- B. Register selection cell 8 bits
- C. Initial register setting cell 8 bits
- D. Security cell 1 bit

(5) User signature cell

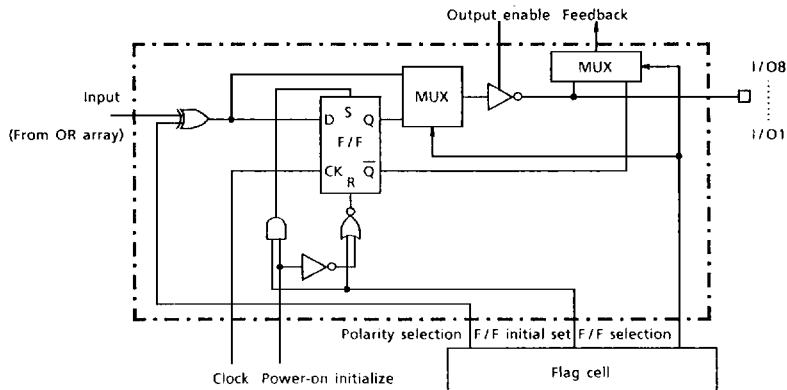
User can program a 41-bit memory array for a variety of uses including ID codes, inventory control, and revision number.

Programming the security bit (security cell) disables access of cells other than the signature cell.

2. Macro cells

TC9803 has 8 macro cells containing D-type flip/flops (register).

Macro Cell



1) Output polarity of OR array

Nine exclusive OR gates control the output polarity of the OR array. These gates are user programmable : setting program data to 1 inputs the output signal from the OR array as inverted ; setting program data to 0, as non-inverted.

2) Register selection

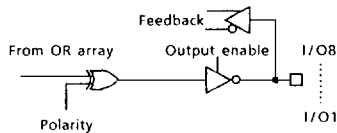
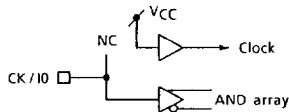
The eight output registers can be independently selected. Setting the program data to 1 selects an output register ; setting to 0 does not select an output register. When an output register is selected, the CK / I0 pin (pin 1) is automatically set to clock input. If an output register is not selected, pin 1 (like I1~I8) is set to dedicated data input. The register operates when the clock pulse goes positive.

3) Initial state of registers at power-up

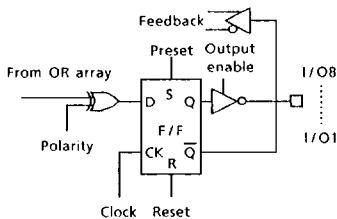
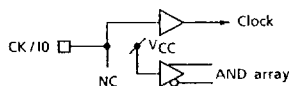
The user can program reset or preset of register outputs at power-up. Setting program data to 1 presets register output ; setting to 0 resets register output. This function can only be used when registers are selected.

Selected / Not selected

A) Not selected (Program data is "0")



B) Selected (Program data is "1")



TC9803P, TC9803FW

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V _{CC}	-0.5~7	V
DC Input Voltage	V _{IN}	-0.5~V _{CC} +0.5	V
DC Output Voltage	V _{OUT}	-0.5~V _{CC} +0.5	V
Input Diode Current	I _{IK}	±20	mA
Output Diode Current	I _{OK}	±20	mA
DC Output Current	I _{OUT}	±35	mA
DC V _{CC} /Ground Current	I _{CC}	±70	mA
Power Dissipation	P _D	500 (DIP) * / 180 (SOL)	mW
Storage Temperature	T _{stg}	-65~150	°C
Lead Temperature (10s)	T _L	300	°C

- * 500mW in the range of T_a = -40~65°C. From T_a = 65°C to 85°C a derating factor of -10mW/°C should be applied up to 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V _{CC}	4.5~5.5	V
Input Voltage	V _{IN}	0~V _{CC}	V
Output Voltage	V _{OUT}	0~V _{CC}	V
Operating Temperature	T _{opr}	-40~85	°C
Input Rise and Fall Time	t _r , t _f	0~500	ns

DC ELECTRICAL CHARACTERISTICS

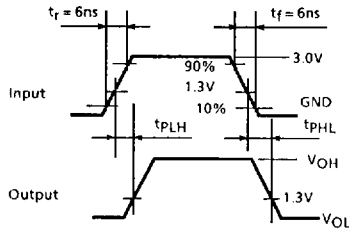
PARAMETER	SYM-BOL	TEST CIR-CUIT	TEST CONDITION	Ta = 25°C				Ta = -40 ~85°C		UNIT	
				V _{CC}	MIN.	TYP.	MAX.	MIN.	MAX.		
High-level input voltage	V _{IH}	—		4.5 ↓ 5.5	2.0	—	—	2.0	—	V	
Low-level input voltage	V _{IL}	—		4.5 ↓ 5.5	—	—	0.8	—	0.8	V	
High-level output voltage	V _{OH}	—	V _{IN} = V _{IH} or V _{IL}	I _{OH} = -20μA	4.5	4.4	4.5	—	4.4	—	V
				I _{OH} = -6mA	4.5	4.18	4.31	—	4.13	—	
Low-level output voltage	V _{OL}	—	V _{IN} = V _{IH} or V _{IL}	I _{OH} = 20μA	4.5	—	0.0	0.1	—	0.1	V
				I _{OH} = 6mA	4.5	—	0.17	0.26	—	0.33	
3-State output off-state current	I _{OZ}	—	V _{IN} = V _{IH} or V _{IL} V _{OUT} = V _{CC} or GND	5.5	—	—	±0.5	—	±5.0	μA	
Input leakage current	I _{IN}	—	V _{IN} = V _{CC} or GND	5.5	—	—	±0.1	—	±1.0		
Quiescent current	I _{CCSB}	—	V _{IN} = V _{CC} or GND Standby	5.5	—	—	4.0	—	40.0	μA	
Operating current	I _{CCOP}	—	f _{IN} = 1MHz Operating	5.0	—	—	—	—	25.0	mA	

AC ELECTRICAL CHARACTERISTICS (C_L = 50pF, Input t_r = t_f = 6ns)

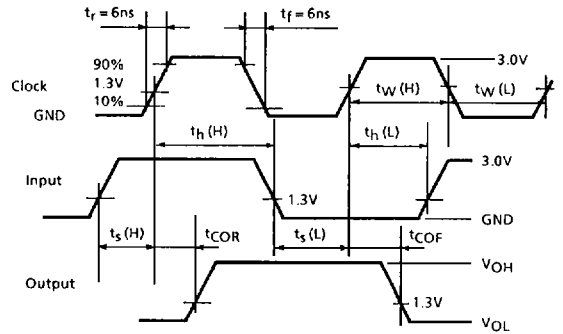
PARAMETER	SYM-BOL	TEST CIR-CUIT	TEST CONDITION	Ta = 25°C				Ta = -40 ~85°C		UNIT
				V _{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time (Input, I/O-Output)	t _{PLH} t _{PHL}	—		4.5	—	23	35	—	40	ns
Propagation Delay Time (Clock-Output)	t _{COR} t _{COF}	—		4.5	—	10	17	—	19	ns
Output Enable Time	t _{PZL} t _{PZH}	—		4.5	—	19	30	—	34	ns
Output Disable Time	t _{PLZ} t _{PHZ}	—		4.5	—	23	33	—	38	ns
Minimum Pulse Width	t _{W(L)} t _{W(H)}	—		4.5	—	7	11	—	13	ns
Minimum Set-up Time	t _S	—		4.5	—	—	30	—	34	ns
Minimum Hold Time	t _H	—		4.5	—	—	0	—	0	ns
Maximum Clock Frequency	f _{MAX}	—		4.5	16	—	—	14	—	MHz

Switching Characteristic Test Waveform

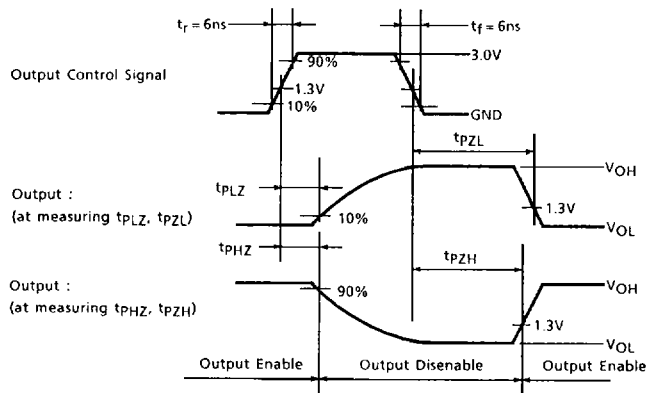
1) t_{PD} (t_{PLH} , t_{PHL})



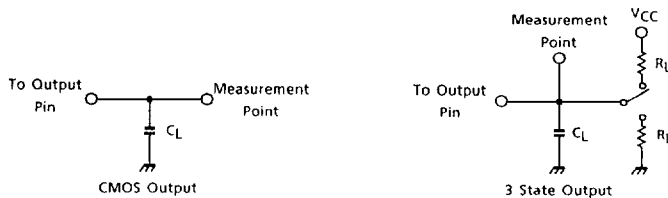
2) t_{CO} (t_{COR} , t_{COF} , t_s , t_h , t_w)



3) t_{PLZ} , t_{PHZ} , t_{PZL} , t_{PZH}



4) Output Test Connection Diagram



Note) C_L includes the capacitance of probe.