MITSUBISHI BIPOLAR DIGITAL ICs

M54502P

DUAL AND GATE WITH DRIVE TRANSISTOR

DESCRIPTION

The M54502P is a semiconductor integrated circuit containing two TTL AND gates and two high current, high breakdown voltage transistors.

FEATURES

- High driving current ($I_{O(max)}$=600mA)
- High breakdown voltage output ($V_{O(max)}$=30V)
- AND gate and transistor are separated.
- Strobe input provided

APPLICATION

General purpose, for use in industrial and consumer digital equipment. Suitable for driving magnetic relays and lamps.

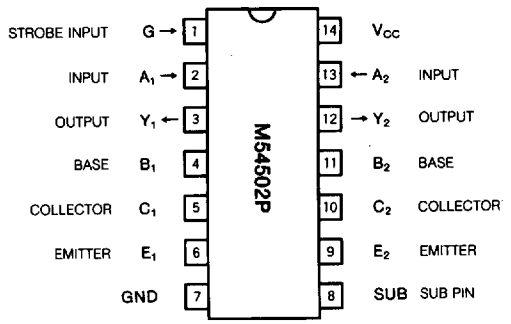
FUNCTION

The M54502P consists of two driver circuits, each having a two input AND gate and a high current, high breakdown voltage transistor. The AND gates and transistors are independent of each other and therefore possible to use as individual circuits. If AND gate output Y is externally connected to base B of the transistor, the unit can be used to drive a magnetic relay or lamp directly. Besides this, the unit can be used as a translater either from TTL to MOS, or from MOS to TTL. With all these features an extremely wide range of usage is ensured.
The AND gate can be directly connected to either TTL or DTL.

FUNCTION TABLE 〈AND Gate〉

A	G	Y
H	H	H
H	L	L
L	H	L
L	L	L

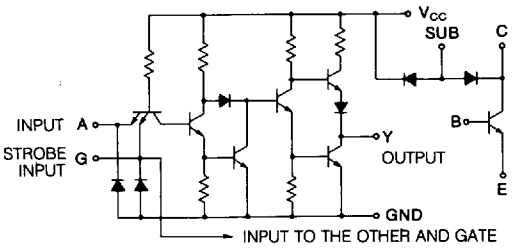
PIN CONFIGURATION (TOP VIEW)



ALWAYS ENSURE THAT SUB PIN IS CONNECTED TO THE LOWEST VOLTAGE POINT.
(EQUAL TO OR LOWER THAN GND)

Outline 14P4

CIRCUIT SCHEMATIC (EACH DRIVER)



ABSOLUTE MAXIMUM RATINGS (T_a = 0~75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		7	V
V_I	Input voltage		5.5	V
V_O	Output voltage (output state High) (Note 1)		V_{CC}	V
V_O	Output voltage (output state High) (Note 2)		30	V
I_O	Output current (output state Low) (Note 2)		600	mA
V_{VS}	V_{CC} to substrate voltage		70	V
V_{CS}	Collector to substrate voltage		70	V
V_{CBO}	Collector to base voltage		70	V
V_{CER}	Collector to emitter voltage (R_{BE} = 500Ω)		65	V
V_{EBO}	Emitter to base voltage		5	V
I_C	Collector current		600	mA
P_d	Power dissipation	T_a = 25℃	1.19	W
T_{opr}	Operating temperature		0~75	℃
T_{stg}	Storage temperature		−65~+150	℃

Note 1 : When gate only is in use.
2 : When gate output is connected to the base of an output transistor.

MITSUBISHI ELECTRIC

DUAL AND GATE WITH DRIVE TRANSISTOR

RECOMMENDED OPERATING CONDITIONS (T_a = 0~75℃, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{CEO}	Collector to emitter voltage			24	V
I_C	Collector current			300	mA

ELECTRICAL CHARACTERISTICS (T_a = 0~75℃, unless otherwise noted)

⟨TTL Gate⟩

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ	Max	
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{OH}	High-level output voltage	V_{CC} = 4.5V, V_I = 2V, I_{OH} = −400 μA		2.4			V
V_{OL}	Low-level output voltage	V_{CC} = 4.5V, V_I = 0.8V, I_{OL} = 16mA				0.4	V
I_{IH}	High-level input current (A)	V_{CC} = 5.5V	V_I = 2.4V			40	μA
			V_I = 4.5V			60	
I_{IH}	High-level input current (G)	V_{CC} = 5.5V	V_I = 2.4V			80	μA
			V_I = 4.5V			120	
I_{IL}	Low-level input current (A)	V_{CC} = 5.5V, V_I = 0.4V				−1.6	mA
I_{IL}	Low-level input current (G)	V_{CC} = 5.5V, V_I = 0.4V				−3.2	mA
I_{OS}	Output short-circuit current	V_{CC} = 5.5V, V_O = 4.5V		−18		−55	mA
I_{CCH}	High-level supply current	V_{CC} = 5.5V, V_I = 4.5V				11	mA
I_{CCL}	Low-level supply current	V_{CC} = 5.5V, V_I = 0V				20	mA

⟨Characteristics when TTL Gate and output transistor are connected⟩

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current	V_{CC} = 4.5V, V_I = 0.8V, V_O = 30V			100	μA
V_{OL}	Low-level output voltage	V_{CC} = 4.5V, V_I = 2V, I_{OL} = 100mA			0.4	V
V_{OL}	Low-level output voltage	V_{CC} = 4.5V, V_I = 2V, I_{OL} = 300mA			0.7	V
I_{CCL}	Low-level supply current	V_{CC} = 5.5V, V_I = 5V			95	mA

⟨Output transistor⟩

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$V_{(BR)CBO}$	Collector to base breakdown voltage	I_C = 100μA, I_E = 0mA	70			V
$V_{(BR)CER}$	Collector to emitter breakdown voltage	I_C = 100μA, R_{BE} = 500Ω	65			V
$V_{(BR)EBO}$	Emitter to base breakdown voltage	I_E = 100μA, I_C = 0mA	5			V
h_{FE}	Direct current amplification factor (Note 3)	V_{CE} = 3V, I_C = 100mA, T_a = 25℃	25			—
		V_{CE} = 3V, I_C = 300mA, T_a = 25℃	30			
		V_{CE} = 3V, I_C = 100mA, T_a = 0℃	20			
		V_{CE} = 3V, I_C = 300mA, T_a = 0℃	25			
V_{BE}	Base to emitter voltage	I_B = 10mA, I_C = 100mA			1	V
		I_B = 30mA, I_C = 300mA			1.2	
$V_{CE(sat)}$	Collector to emitter saturation voltage	I_B = 10mA, I_C = 100mA			0.4	V
		I_B = 30mA, I_C = 300mA			0.7	

Note 3 : Measurement should be done in a short time.

PRECAUTIONS FOR USE (WHEN TTL GATE AND OUTPUT TRANSISTOR ARE CONNECTED)

The permissible amount of collector current of the output transistor I_O varies according to the conditions. Calculate it as follows, using Fig. 1 "Heat Dissipation Rate Characteristics", Fig. 2 "Pulse Power Chart", and the following formula.

$$P_d = \frac{V_{CC}}{M+N}(M \cdot I_{CCL} + N \cdot I_{CCH}) + M \cdot I_O \cdot V_{OL} \cdots\cdots(1)$$

Where P_d : Power dissipation
I_{CCL} : Supply current when all outputs of output transistors are "Low".
I_{CCH} : Supply current when all outputs of output transistors are "High".
V_{OL} : Output voltage when output is "Low".
M : The number of output transistors whose state is "Low".
N : The number of output transistors whose state is "High".
M+N : The total number of gates included in one package.

When trying to determine permissible amount of constant current, first, read the largest permissible power dissipation P_d for the given operating free-air ambient temperature range from Fig. 1. Then calculate I_O by substituting into Formula (1) the maximum values of I_{CCL}, I_{CCH} and V_{CC} as well as values M and N.

When calculating pulse current I_O, use Fig. 2. First, determine maximum permissible power dissipation P_d from the duty cycle and pulse width, then calculate using Formula (1). In this case, be careful that I_O does not exceed the absolute maximum rating.

TYPICAL CHARACTERISTICS

Fig.1 "HEAT DISSIPATION RATE CHARACTERISTICS"

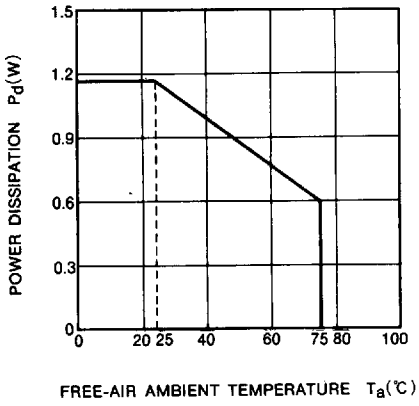
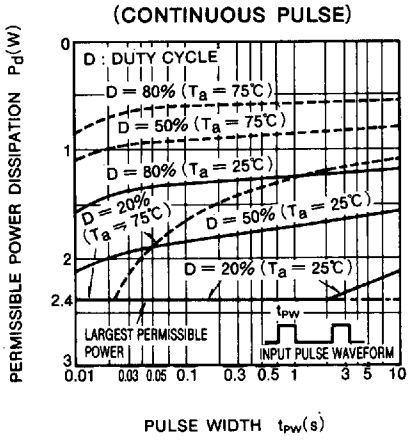


Fig.2 PULSE POWER CHART (CONTINUOUS PULSE)



SAFE RANGE OF OPERATION FOR THE OUTPUT TRANSISTOR (WHEN USED INDEPENDENTLY OF TTL GATE)

Both Fig. 3 and Fig. 4 show the safe operating ranges of output transistors when they are separate from and independent of the gates. Fig. 4 gives characteristics when t_{PW} = 20ms. When used for values other than 20ms determine the safe operating range using the method given below.

Calculate P_C using Formula (2). (P_C being the total of collector dissipation of all "ON" transistors)

$$P_C = P_d - \frac{V_{CC}}{M+N}(M \cdot I_{CCL} + N \cdot I_{CCH}) \cdots\cdots(2)$$

Where P_d : Permissible power dissipation read from Fig. 1 and Fig. 2.

I_{CCL} : Supply current when gate output state is "Low".

I_{CCH} : Supply current when gate output state is "High".

(NOTE: The values of I_{CCL} and I_{CCH} will vary somewhat depending on the load connected to gate outputs.)

After using Formula (2) to calculate P_C, enter it into the following Formula (3) to find the safe operating range.

$$P_C = V_{CE} \cdot I_C \cdots\cdots(3)$$

However, the absolute maximum rating of $V_{CE} \leqq 30V$ and $I_C \leqq 600mA$ must be observed.

Note that Figs 3 and 4 express power dissipation per package. Therefore, one transistor may consume all the power indicated in Fig. 3 and Fig. 4 if the other transistor and the gates are not used.

Fig.3 SAFE OPERATING RANGE OF OUTPUT TRANSISTOR (ONE SHOT PULSE)

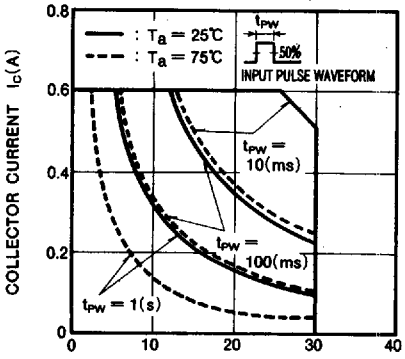


Fig.4 SAFE OPERATING RANGE OF OUTPUT TRANSISTOR (CONTINUOUS PULSE)