

Z80382 SL1944

HIGH-PERFORMANCE DATA COMMUNICATIONS PROCESSOR

FEATURES

- Embedded Z380™ Microprocessor
 - Maintains Object Code Compatibility with Z80® and Z180™ Microprocessors
 - Enhanced Instruction Set for 16-Bit Operation
 - 16 MB Linear Addressing
 - Two Clock Cycle Instruction Execution Minimum
 - Four On-Chip Register Banks
 - BC/DE/HL/IX/IY Augmented to 32 Bits
 - Clock Divide-by-Two and Multiply-by-Two Options
 - Fully Static CMOS Design with Low-Power Standby Mode
 - 16-Bit Internal Bus
 - Dynamic Bus Sizing (8/16-Bit Inter-Operability)
- 16550 Mimic with I/O Mailbox, DMA Mailbox, and 16 mA Bus Drive
- Three HDLC Synchronous Serial Channels
 - Serial Data Rate of up to 10 Mbps
- GCI/SCIT Bus Interface
- Eight Advanced DMA Channels with 24-Bit Addressing
- Plug-and-Play ISA Interface
- PCMCIA Interface
- Two Enhanced ASCIs (UARTs) with 16-Bit Baud Rate Generators (BRG)
- Clocked Serial I/O Channel (CSIO) for Use with Serial Memory
- Two 16-Bit Timers with Flexible Prescalers
- Three Memory Chip Selects with Wait-State Generators
- Watch-Dog Timer (WDT)
- Up to 32 General-Purpose I/O Pins
- DC to 20 MHz Operating Frequency @ 5.0V
- 144-Pin QFP and VQFP Style Packages

GENERAL DESCRIPTION

The Z80382 (Z382) is designed to address high-end data communication applications such as digital modems (ISDN, GSM, Mobitex & Modacom), xDSL and analog modems (V.34 and beyond). The Z382 provides a performance upgrade to existing Z80- and Z18x-based designs by utilizing the increased bandwidth of the 380C processor. The Z8L382 is a low voltage version of the device.

Note: In this document the notation “380C” denotes the Z380-compatible CPU core which is embedded in the Z382.

The 380C microprocessor is a high-performance processor with fast and efficient throughput and increased memory addressing capabilities. The 380C offers a continuing

growth path for present Z80- or Z18x-based designs, while maintaining Z80 and Z180 object code compatibility. Its enhancements include added instructions, expanded 16 MB address space and flexible bus interface timing.

In the 380C, the basic addressing modes of the Z80 microprocessor have been augmented to include Stack Pointer Relative loads and stores, 16-bit and 24-bit indexed offsets, and more flexible Indirect Register addressing. Internally, all of the addressing modes allow up to 32-bit linear addressing; however, because the Z382 has only 24 address pins, it can only address 16 MB of memory.

Other additions to the instruction set include a full complement of 16-bit arithmetic and logical operations, 16-bit I/O

GENERAL DESCRIPTION (Continued)

operations, multiply and divide, and a complete set of register-to-register loads and exchanges.

The 380C register file includes alternate versions of the IX and IY registers. There are four banks of registers in the 380C, along with instructions for switching among them. All of the 16-bit register pairs and index registers in the basic Z80 microprocessor register file are expanded to 32 bits.

The Z382 includes dynamic bus sizing to allow any mix of 16- and 8-bit memory, and I/O devices in a system. One application for this capability would be to copy code from a low-cost, slow 8-bit ROM to 16-bit RAM, from which it can be executed at much higher speeds. Memory bus sizes can be configured internally by software to eliminate the need for external logic to drive MSIZE.

Some features that have traditionally been handled by external peripherals have been incorporated in the Z382. These on-chip peripherals reduce system chip count and interconnections on the external bus. These peripherals, illustrated in the Z382 Block Diagram in Figure 1, are summarized below.

HDLC Synchronous Channels. Three HDLC channels operate at serial data rates of up to 10 Mbps and feature 8-byte receive and transmit FIFOs. These can be used for modems, general data communications, and ISDN. The ISDN can be handled separately or through the GCI/SCIT bus interface. HDLC Channels always transfer data through the DMA channels. A transparent mode is selectable. Two of the HDLC cells can be pin multiplexed with the ASCIs (UARTs) to provide dynamically switchable (async-sync) DTE interfaces.

DMA Channels. The eight DMA channels provide 24-bit memory addressing and can transfer memory block sizes of up to 64 KB (16-bits). These DMA channels can be dynamically assigned to serve the HDLC ports, Mimic COM port, Host DMA Mailbox, or ASCIs in any mixture. Linked list operation allows all HDLC transmitters and receivers to operate at or above E1 rates simultaneously without loading the bus bandwidth.

16550 Mimic. Provides connection to a PC ISA bus and emulation of the 16550 UART register set. Improvements include 16 mA output drivers and internal COM port address decoding to reduce external PC interface components.

ASCI. Two flexible asynchronous serial channels with baud rate generators, modem control and status.

CSIO. A clocked serial I/O channel which can be used for serial memory interface.

Timers. Two 16-bit counter/timers with flexible prescalers for wide-range timing applications.

GCI/SCIT Bus Interface. A common interface to ISDN interface devices. Internal signals from this module can be connected to the HDLC channels to provide B-channels and D-channel for ISDN.

Plug-and-Play ISA Interface. Provides auto-configuration in ISA (AT bus) applications.

PCMCIA Interface. Provides connectivity to a PCMCIA bus.

32-Bit General-Purpose I/O. For non-PC add-in applications, four 8-bit ports are provided for general-purpose I/O. In ISA or PCMCIA applications, the pins from two of the ports are reallocated to host bus signals and are not available. Pins from the other two ports are selectively multiplexed with on-chip peripheral functions (ASCIs, CSIO, PRT). These pins are individually programmable for input/output mode.

I/O Chip Selects. Two I/O chip selects are provided to support I/O access of external peripherals. Each has a programmable base address and provides I/O decode sizes ranging from 8 to 512 bytes.

ROM/RAM Chip Selects with Wait-State Generators. Chip select outputs are provided to decode memory addresses and provide memory chip enables. Each chip select has its own Wait State Generator to allow use of memories with different speeds.

Watch-Dog Timer. A Watch-Dog Timer (WDT) with a wide range of time-constants prevents code runaway and possible resulting system damage. The /RESET input can be forced as an output upon the terminal count of the WDT. This allows external peripherals to be reset along with the Z382.

Note: This Customer Procurement Specification applies only to the Z80382, SL1944. Any reference to the Z8L382 (3.3V version) in this document should be ignored.

Notes: All signals with a preceding front slash, "/", are active Low. For example, B//W (WORD is active Low); /B//W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V _{CC}	V _{DD}
Ground	GND	V _{SS}

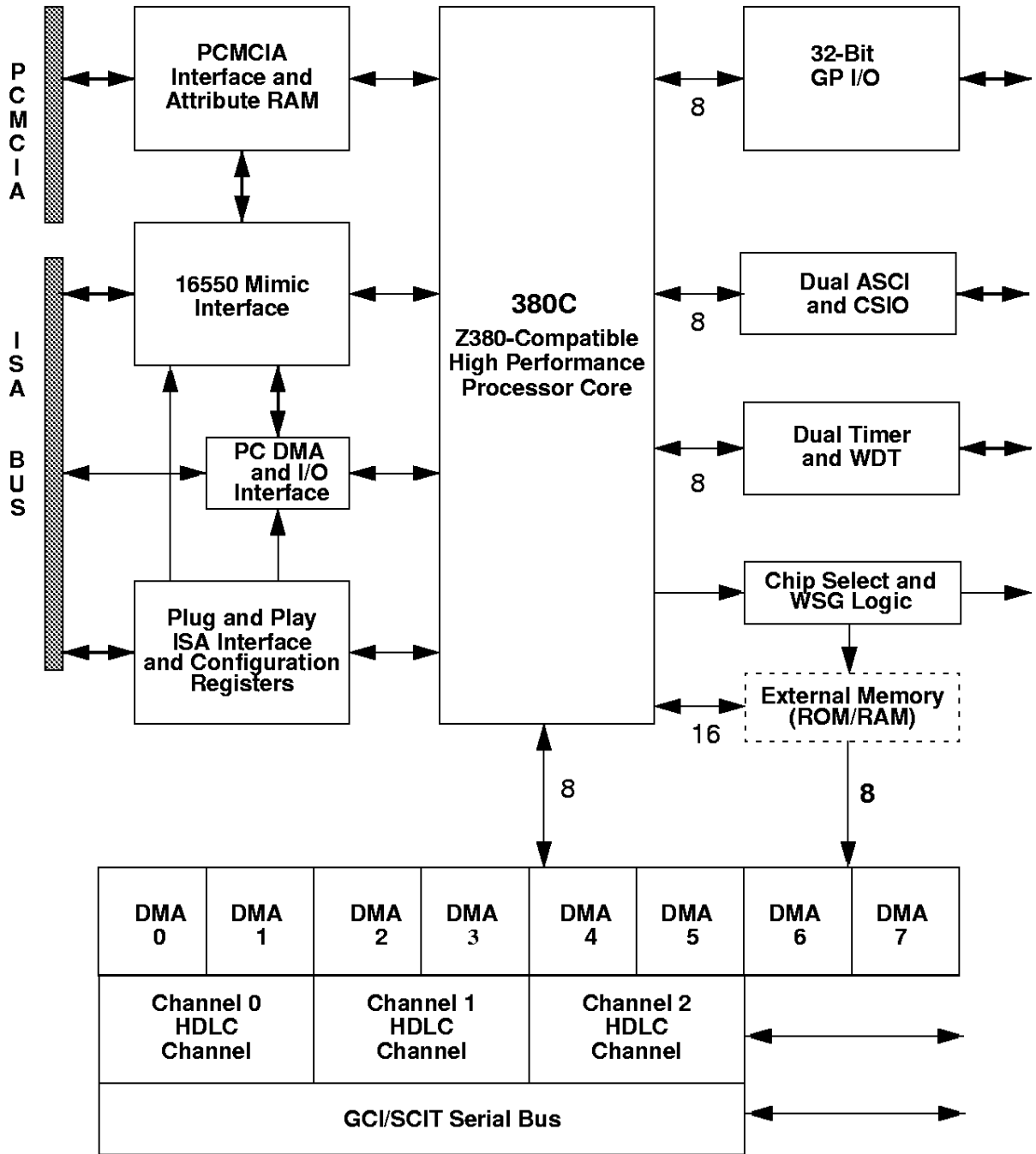


Figure 1. Z80382 Block Diagram

Z80382 PIN DESCRIPTION

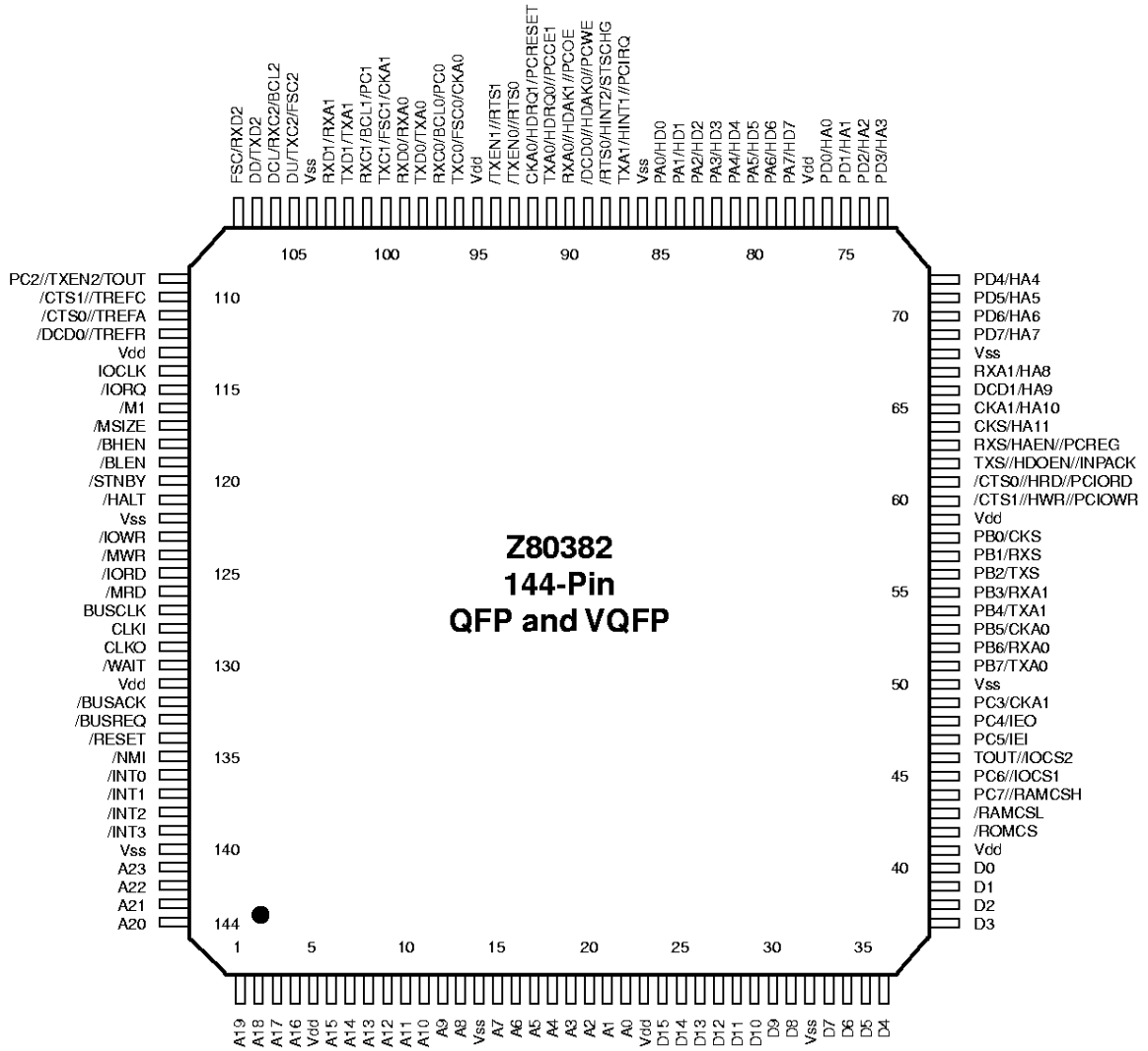


Figure 2. Z80382 144-Pin QFP and VQFP Pin Description

ABSOLUTE MAXIMUM RATINGS

Symbol	Description	Value	Unit
V_{DD}	Supply Voltage	-0.3 to +7.0	V
V_{IN}	Input Voltage	-0.3 to $V_{DD}+0.3$	V
T_{OPR}	Operating Temp	0 to +70	°C
T_{STG}	Storage Temp	-55 to +150	°C

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

STANDARD TEST CONDITIONS

The DC Characteristics which follow apply for the following standard test conditions, unless otherwise noted. All voltages are referenced to GND (0V). Positive current flows into the referenced pin (Figure 3, Test Load Diagram).

- Operating temperature range:
 - Standard: 0°C to 70°C
- Voltage Supply Range:
 - $+4.5V \leq V_{DD} \leq +5.5V$ (Z80382 versions)
 - $+3.0V \leq V_{DD} \leq +3.6V$ (Z8L382 versions)

All AC parameters assume a load capacitance of 50 pF. Add 10 ns delay for each 50 pF increase in load up to a maximum of 150 pF for the data bus and 100 pF for address and control lines. AC timing measurements are referenced to 1.5 volts (except for clock, which is referenced to the 10% and 90% points). Maximum capacitive load for PHI is 125 pF.

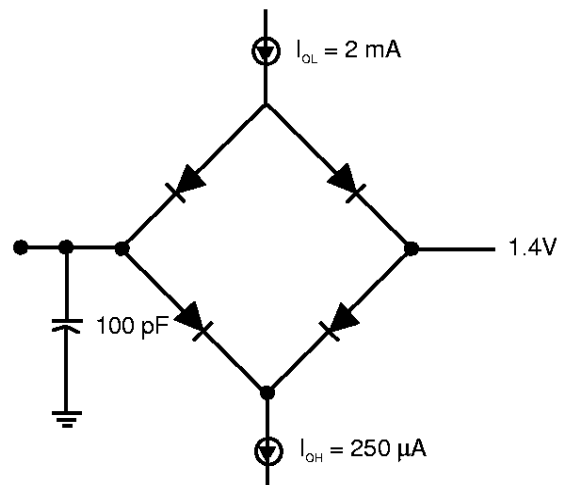


Figure 3. Test Load Diagram

DC CHARACTERISTICS

Pin Numbers and Input/Output Classifications

Pin Number(s)	Pin Description	Input Class ¹	Output Class ¹
118	/BHEN		O
119	/BLEN		O
132	/BUSACK		O
133	/BUSREQ	I	
61	/CTS0//HRD//PCIORD	I	
111	/CTS0//TREFA	I	O
60	/CTS1//HWR//PCIOR	I	
110	/CTS1//TREFC	I	O
89	/DCD0//HDAK0//PCWE	I	
112	/DCD0//TREFR	I	O
66	/DCD1//HA9	I	
121	/HALT		O
136 - 139	/INT0-3	R	
125	/IORD	I	3
115	/IORQ	I	3
123	/IOWR	I	3
116	/M1	I	3
126	/MRD	I	3
117	/MSIZE	I	D
124	/MWR	I	3
135	/NMI	R	
43	/RAMCSL		O
134	/RESET	R	D
42	/ROMCS	O	
88	/RTS0//HINT2//STSCHG		H
120	/STNBY		O
94 - 93	/TXEN1-0//RTS1-0		O
130	/WAIT	I	D
141 - 144, 1 - 4, 6 - 13, 15 - 22	A23-0	I	3
127	BUSCLK		H
92	CKA0//HDRQ1//PCRESET	I	H
65	CKA1//HA10	I	3
64	CKS//HA11	I	3
128	CLKI	R	
129	CLKO		O
24 - 31, 33 - 40	D15-0	I	3
106	DCL//RXC2//BCL2	I	
107	DD//TXD2	I	D (DD) O (TXD2)
105	DU//TXC2//FSC2	I	D (DU) O (TXC2, FSC2)
108	FSC//RXD2	I	
114	IOCLK	I	O
78 - 85	PA7-0//HD7-0	I	H
58	PB0//CKS	I	3

DC CHARACTERISTICS (Continued)

Pin Number(s)	Pin Description	Input Class ¹	Output Class ¹
57	PB1/RXS	i	3
56	PB2/TXS	i	3
55	PB3/RXA1	i	3
54	PB4/TXA1	i	3
53	PB5/CKA0	i	3
52	PB6/RXA0	i	3
51	PB7/TXA0	i	3
109	PC2//TXEN2/TOUT	i	3
49	PC3/CKA1	i	3
48	PC4/IEO	i	3
47	PC5/IEI	i	3
45	PC6//IOCS1	i	3
44	PC7//RAMCSH	i	3
69 - 76	PD7-0/HA7-0	i	3
90	RXA0//HDAK1//PCOE	i	D
67	RXA1/HA8	i	3
101, 97	RXC1-0/BCL1-0/PC1-0	i	3
103, 99	RXD1-0/RXA1-0	i	O
63	RXS/HAEN//PCREG	i	D
46	TOUT//IOCS2		3
91	TXA0/HDRQ0//PCCE1	i	H
87	TXA1/HINT1//PCIRQ		H
100, 96	TXC1-0/FSC1-0/CKA1-0	i	3
102, 98	TXD1-0/TXA1-0		O
62	TXS//HDOEN//INPACK		O
5, 23, 41, 59, 77, 95, 113, 131	V _{DD}		
14, 32, 50, 68, 86, 104, 122, 140	V _{SS}		

Note: 1. Characteristics of each pin are listed in terms of the classifications in the DC Characteristics Tables 1 and 2 which follow.

DC CHARACTERISTICS (Continued)

Specifications apply over Standard Operating Conditions unless otherwise noted.

Table 1. Output Class Characteristics

Output Class ⁽¹⁾	Type	V _{OL} Max.	V _{OH} Min.	C _{OUT} Max. ⁽²⁾
O	Totem Pole	0.4V @ I _{OL} = 2.0 ma	V _{DD} - 1.2V @ I _{OH} = 200 μA	15 pF
Slew Rate = 0.33 V/ns min @ C _{LOAD} = 50 pF				
3	Tri-State	0.4V @ I _{OL} = 2.0 ma	V _{DD} - 1.2V @ I _{OH} = 200 μA	
Slew Rate = 0.33 V/ns min @ C _{LOAD} = 50 pF				
H	High Drive Tri-State	0.4V max @ I _{OL} = 16 mA, V _{DD} = 5V	2.4V min @ I _{OH} = 5mA, V _{DD} = 5V	15 pF
Slew Rate = 0.33 V/ns min @ C _{LOAD} = 50 pF				
D	Open-Drain	0.4V max @ I _{OL} = 16 mA	--	15 pF

Notes:

1. The Pin Numbers and Input/Output Classifications table in the previous section identifies the specific output pins in each class.
2. Applies to Output only or I/O.

Table 2. Input Class Characteristics

Input Class ⁽¹⁾	V _{IL} Max. (Z80382)	V _{IL} Max. (Z8L382)	V _{IH} Min. (Z80382)	V _{IH} Min. (Z8L382)	Minimum Hysteresis
I	0.8V	0.6V	2.0V	2.0V	0.4V
I _I = ±10 μA max, V _I = 0 to 5V (includes leakage if I/O) C _{IN} = 5 pF max (if input only, see output type if I/O)					
Note: Inputs of this type include a weak-latch circuit, except that a register bit can disable those for pins PB7-0.					
R	0.4V	0.4V	V _{DD} - 0.6V	V _{DD} - 0.3V	0.4V
I _I = ±10 μA max, V _I = 0 to 5V C _{IN} = 5 pF max					

Note: Inputs of this type except CLKI include a weak-latch circuit.

Note: The Pin Numbers and Input/Output Classifications table in the previous section identifies the specific input pins in each class.

Table 3. DC Electrical Characteristics

Symbol	Item	Condition	Min.	Typ.	Max.	Unit	Notes
V_{IH}	Input High Voltage		See Table 2			V	
V_{IL}	Input Low Voltage		See Table 2			V	
V_{OH}	Output High Voltage		See Table 1			V	
V_{OL}	Output Low Voltage		See Table 1			V	
I_{IL}	Input Leakage Current, All Inputs Except CLKI, CLKO	$V_{IN} = 0.5V$ to $V_{DD} - 0.5V$			1.0	μA	
I_{TL}	Tri-State Leakage Current	$V_{IN} = 0.5$ to $V_{DD} - 0.5$			1.0	μA	
I_{DD}	V_{DD} Supply Current Normal Operation	BUSCLK = 10 MHz $V_{DD} = 3.3V$			75	mA	1,3
		BUSCLK = 10 MHz $V_{DD} = 5V$			90	mA	1,3
		BUSCLK = 20 MHz $V_{DD} = 5V$			150	mA	1,3
I_{DDs}	V_{DD} Supply Current Standby Mode	BUSCLK = 10 MHz $V_{DD} = 3.3V$			50	μA	1,2,3
		BUSCLK = 10 MHz $V_{DD} = 5V$			50	μA	1,2,3
		BUSCLK = 20 MHz $V_{DD} = 5V$			50	μA	1,2,3

Notes:

1. V_{IH} min = $V_{DD} - 1.0V$, V_{IL} max = 0.8V. All output terminals are at no load.
2. On-chip peripherals with independent clocks are inactive (not being clocked).
3. BUSCLK is the internal processor clock frequency.

AC CHARACTERISTICS

380C Processor Timing (See Figure 4)

Specifications apply over Standard Operating Conditions unless otherwise noted. $C_L = 50$ pF for outputs.

Symbol	Parameter	Z80382		Z8L382		Notes	Unit
		Min.	Max.	Min.	Max.		
t1	Clock Cycle Time	25	DC	50	DC	1	ns
t2	Clock High Time	10		20		1	ns
t3	Clock Low Time	10		20		1	ns
t4	Clock Rise Time		3		5	1	ns
t5	Clock Fall Time		3		5	1	ns
t6	CLKI Low to BUSCLK High Delay		25		35		ns
t7	CLKI High to BUSCLK Low Delay		25		35		ns
t8	BUSCLK High to Output Valid		10		10	2	ns
t9	BUSCLK Low to Output Valid		10		10	3	ns
t10	Input Setup to BUSCLK Rise	10		15		4	ns
t11	Input Hold from BUSCLK High	0		0		4	ns
t12	/BUSREQ Setup to BUSCLK Fall	10		15		5	ns
t13	/BUSREQ Hold from BUSCLK Low	0		0		5	ns
t14	/WAIT Setup to BUSCLK Rise	10		15		6	ns
t15	/WAIT Hold from BUSCLK High	0		0		6	ns
t16	/WAIT Setup to BUSCLK Fall	15		15		6	ns
t17	/WAIT Hold from BUSCLK Low	0		0		6	ns
t18	/NMI Width Low	15		15			ns
t19	/RESET Width Low	10		10			t1
t20	/INT1, /INT2, /INT3 Low Width	15		15		7	ns
t21	/INT1, /INT2, /INT3 High Width	15		15		7	ns

Notes:

1. Applies to the oscillator or external clock input. The maximum internal clock frequency (BUSCLK) is limited to 20 MHz for the Z80382 and 10 MHz for the Z8L382. Input clock frequencies greater than these values must use the CLKI/2 mode for creating BUSCLK. This is the default state after Reset.
2. Applies to A23-0, /BHEN, /BLEN, IOCLK, /IOCS1, /IOCS2, /ROMCS, /RAMCSL, /RAMCSH, /M1, /BUSACK, /MRD, /MWR, /TREFA, /TREFC, /TREFR
3. Applies to D15-0, /HALT, /STNBY, /IORQ, /IORD, /IOWR, /MSIZE, /BUSACK, /MRD, /MWR, /TREFC, /TREFR
4. Applicable for Data Bus and /MSIZE inputs.
5. /BUSREQ can also be asserted/deasserted asynchronously.
6. External waits asserted at /WAIT input.
7. In edge-triggered mode.

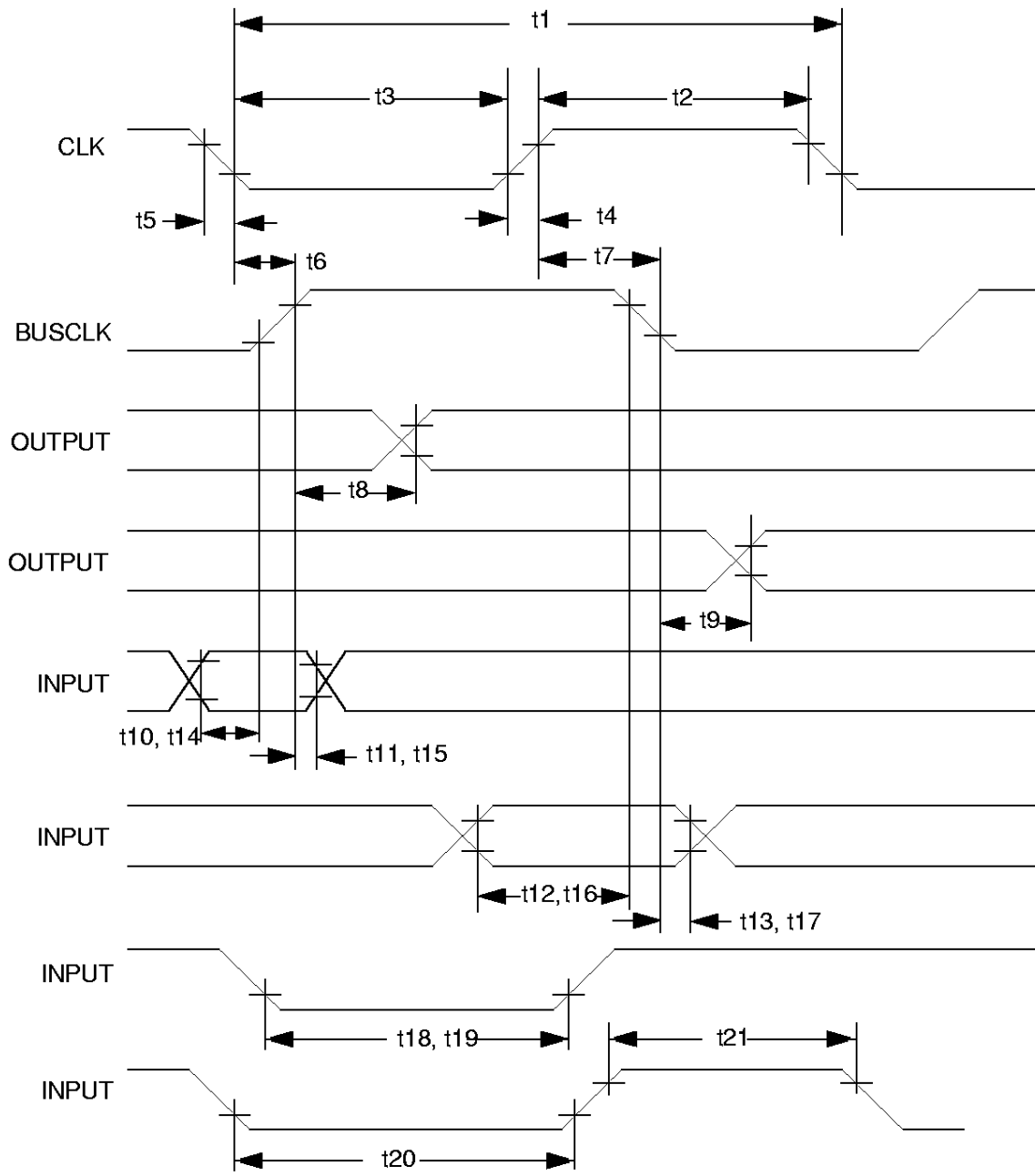


Figure 4. 380C Processor Timing

AC CHARACTERISTICS (Continued)

Host - PCMCIA Attribute Memory Read Timing (See Figure 5)

Specifications apply over Standard Operating Conditions unless otherwise noted. $C_L = 50$ pF for outputs.

Symbol	Parameter	Z80382		Z8L382		Unit
		Min.	Max.	Min.	Max.	
t22	Address Setup to /PCCE1 Fall	15		20		ns
t23	Address Setup to /PCOE Fall	15		20		ns
t24	Address Hold from /PCCE1 High	5		5		ns
t25	Address Hold from /PCOE High	5		5		ns
t26	/PCCE1 Low to Data Active	0		0		ns
t27	/PCOE Low to Data Active	0		0		ns
t28	/PCCE1 Low to Data Valid		60	5	60	ns
t29	/PCOE Low to Data Valid		60	5	60	ns
t30	Data Invalid from /PCCE1 High	5				ns
t31	Data Invalid from /PCOE High	5				ns
t32	Data Tri-state from /PCCE1 High		20		20	ns
t33	Data Tri-state from /PCOE High		20		20	ns

Note: Timings also apply for reads from registers located in the attribute memory space.

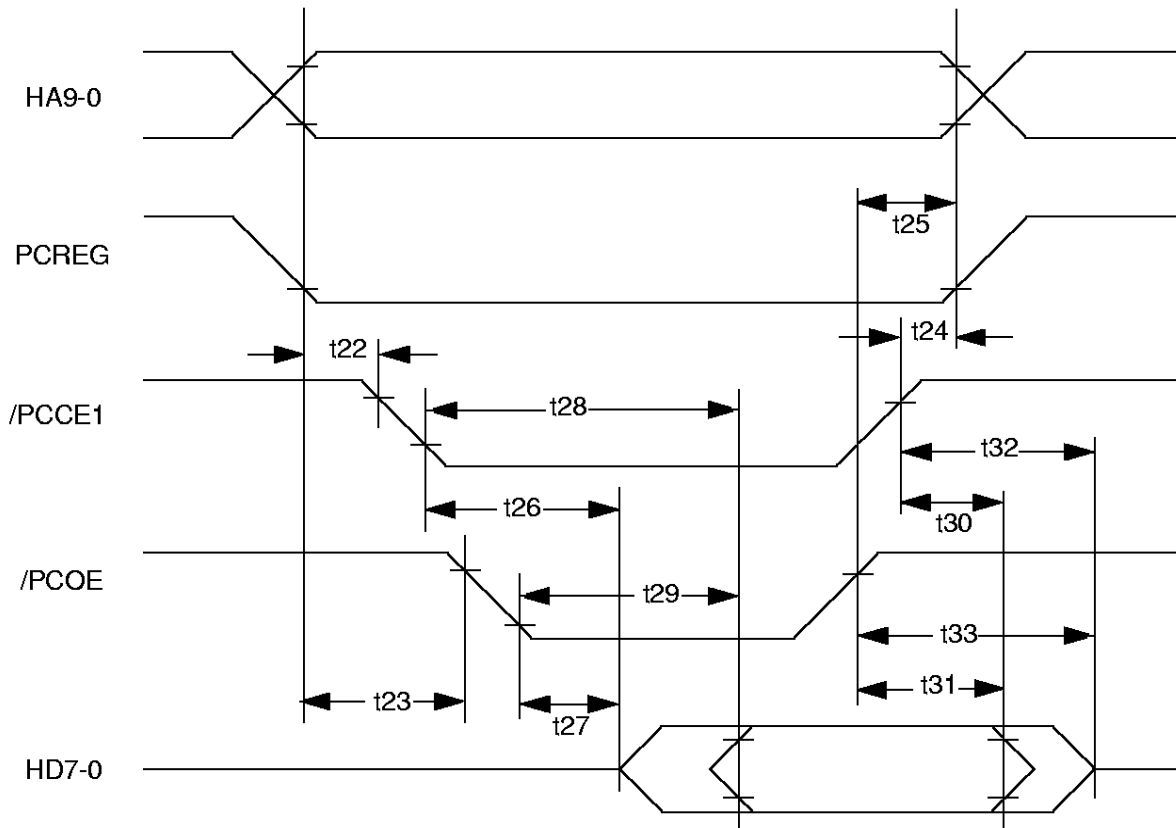


Figure 5. Host - PCMCIA Attribute Memory Read Timing

Host - PCMCIA Attribute Memory Write Timing (See Figure 6)

Specifications apply over Standard Operating Conditions unless otherwise noted. $C_L = 50$ pF for outputs.

Symbol	Parameter	Z80382		Z8L382		Unit
		Min.	Max.	Min.	Max.	
t34	Address Setup to /PCCE1 Fall	30		35		ns
t35	Address Setup to /PCWE Fall	30		35		ns
t36	Address Hold from /PCCE1 High	10		10		ns
t37	Address Hold from /PCWE High	10		10		ns
t38	Data Setup to /PCCE1 Rise	20		20		ns
t39	Data Setup to /PCWE Rise	20		20		ns
t40	Data Hold from /PCCE1 High	10		10		ns
t41	Data Hold from /PCWE High	10		10		ns

Timings also apply for writes to registers located in the attribute memory space.

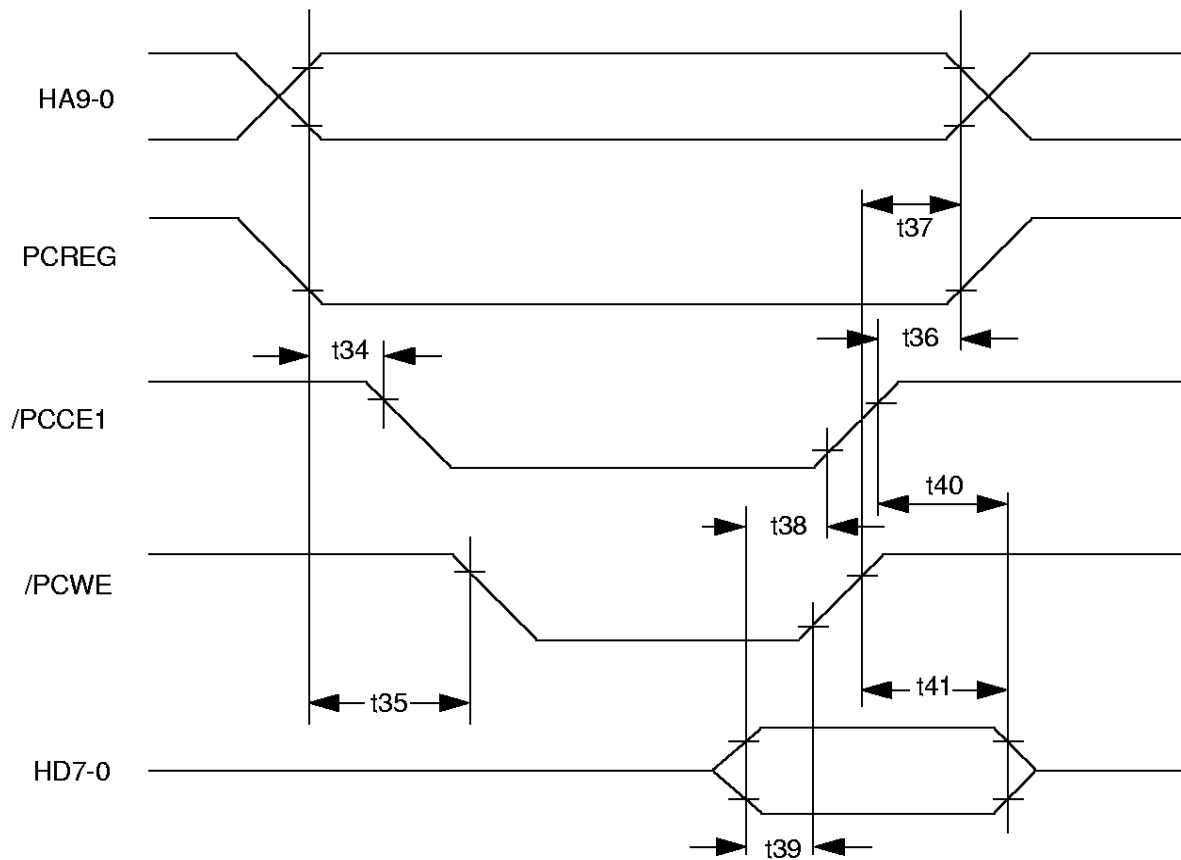


Figure 6. Host - PCMCIA Attribute Memory Write Timing

AC CHARACTERISTICS (Continued)

Host - PCMCIA I/O Read Timing (See Figure 7)

Specifications apply over Standard Operating Conditions unless otherwise noted. $C_L = 50$ pF for outputs.

Symbol	Parameter	Z80382		Z8L382		Units
		Min.	Max.	Min.	Max.	
t42	Address Setup to /PCIORD Fall	50		50		ns
t43	/PCREG Setup to /PCIORD Fall	5		5		ns
t44	/PCCE1 Setup to /PCIORD Fall	5		5		ns
t45	/PCIORD Low Width	125		125		ns
t46	/INPACK Low from /PCIORD Low		10		10	ns
t47	Data Valid from /PCIORD Low		50		50	ns
t48	Data Invalid from /PCIORD High	5		5		ns
t49	/INPACK High from /PCIORD High		10		10	ns
t50	/PCCE1 Hold from /PCIORD High	10		10		ns
t51	/PCREG Hold from /PCIORD High	10		10		ns
t52	Address Hold from /PCIORD High	10		10		ns
t53	/PCIORD Low to Data Active	0		0		ns
t54	Data Tri-state from /PCIORD High		20		20	ns

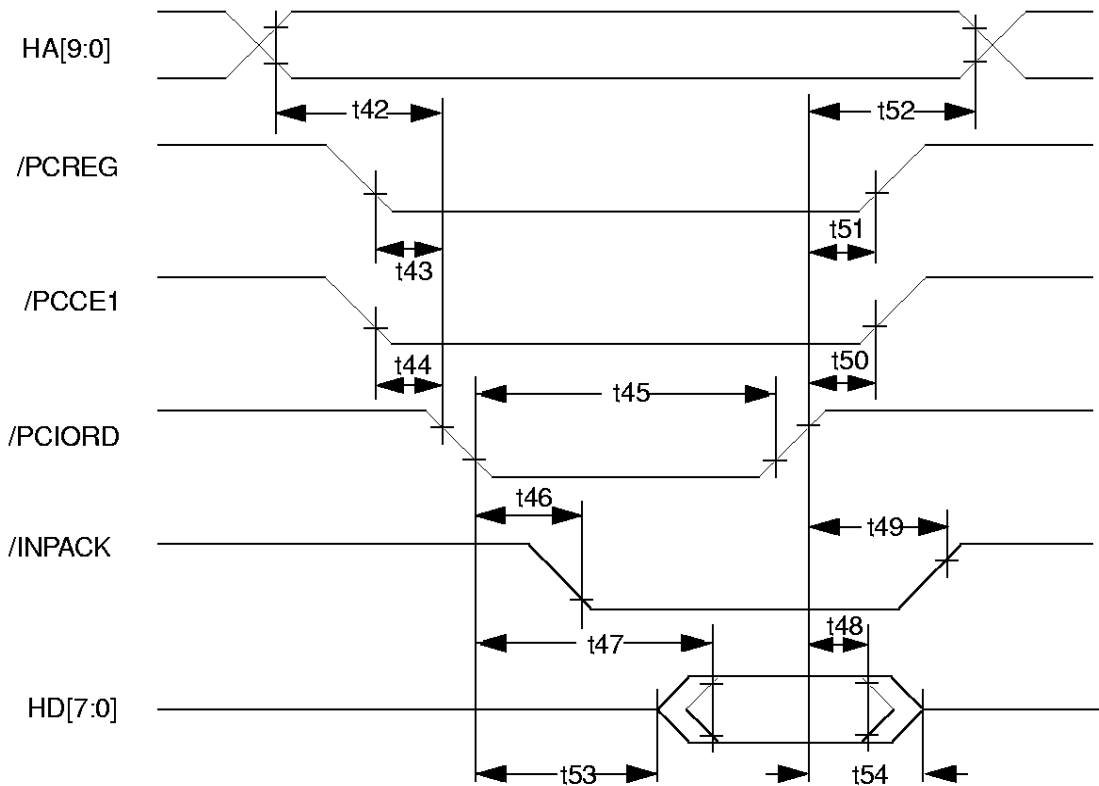


Figure 7. Host - PCMCIA I/O Read Timing

Host - PCMCIA I/O Write Timing (See Figure 8)

Specifications apply over Standard Operating Conditions unless otherwise noted. $C_L = 50$ pF for outputs.

Symbol	Parameter	Z80382		Z8L382		Units
		Min.	Max.	Min.	Max.	
t55	Address Setup to /PCIOWR Fall	50		50		ns
t56	/PCREG Setup to /PCIOWR Fall	5		5		ns
t57	/PCCE1 Setup to /PCIOWR Fall	5		5		ns
t58	/PCIOWR Low Width	125		125		ns
t59	Data Setup to /PCIOWR Rise	35		35		ns
t60	Data Hold from /PCIOWR High	20		20		ns
t61	/PCCE1 Hold from /PCIOWR High	10		10		ns
t62	/PCREG Hold from /PCIOWR High	10		10		ns
t63	Address Hold from /PCIOWR High	10		10		ns

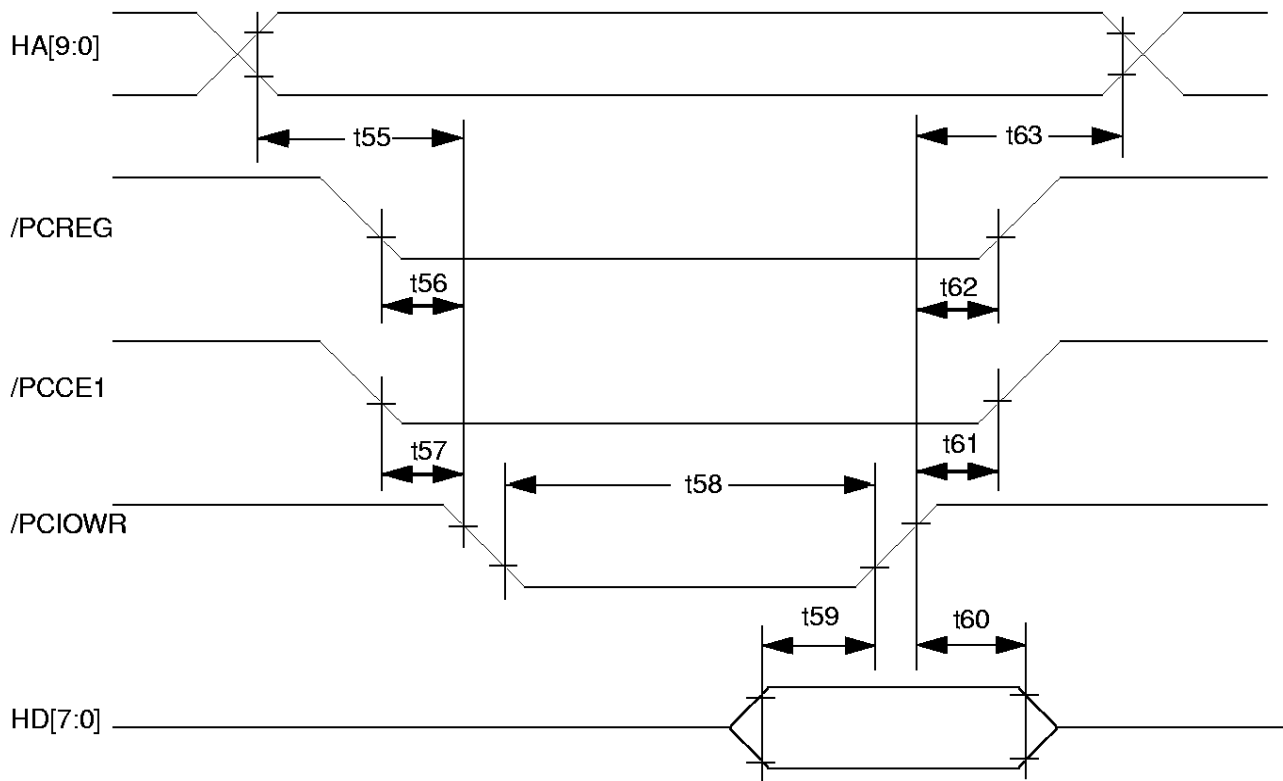


Figure 8. Host PCMCIA I/O Write Timing

AC CHARACTERISTICS (Continued)

Timer Output Timing (See Figure 9)

Specifications apply over Standard Operating Conditions unless otherwise noted. $C_L = 50$ pF for outputs.

Symbol	Parameter	Z80382		Z8L382		Units
		Min.	Max.	Min.	Max.	
t64	BUSCLK Low to TOUT Valid		20		20	ns

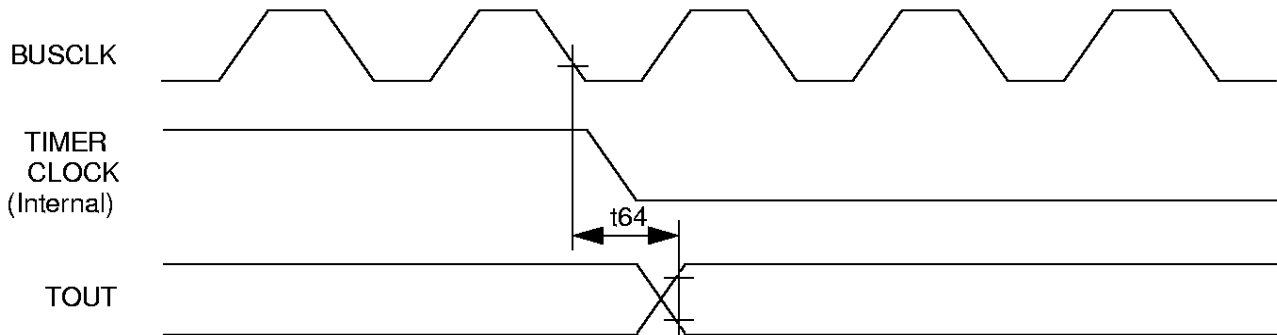


Figure 9. Timer Output Timing

CSI/O Receive/Transmit Timing (See Figure 10)

Specifications apply over Standard Operating Conditions unless otherwise noted. $C_L = 50$ pF for outputs.

Symbol	Parameter	Z80382		Z8L382		Units
		Min.	Max.	Min.	Max.	
t66	CKS Low to TXS Valid		40		40	ns
t67	RXS Setup to CKS Rise	20		20		ns
t68	RXS Hold from CKS High	5		5		ns
t71	CKS External Clock Period	50		50		ns

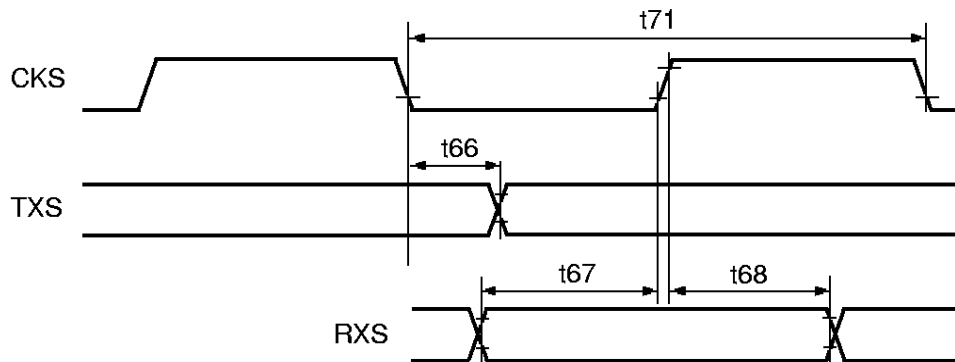


Figure 10. CSI/O Receive and Transmit Timing

AC CHARACTERISTICS (Continued)

ASCI Transmitter Timing (See Figure 11)

Specifications apply over Standard Operating Conditions unless otherwise noted. $C_L = 50$ pF for outputs.

Symbol	Parameter	Z80382		Z8L382		Units
		Min.	Max.	Min.	Max.	
t72	External Transmit Clock Period	50		50		ns
t73	External Transmit Clock Low Width	30		30		ns
t74	External Transmit Clock High Width	30		30		ns
t75	External Transmit Clock Fall Time		5		10	ns
t76	External Transmit Clock Rise Time		5		10	ns
t77	CKA Low to TXA Data Valid		20		30	ns

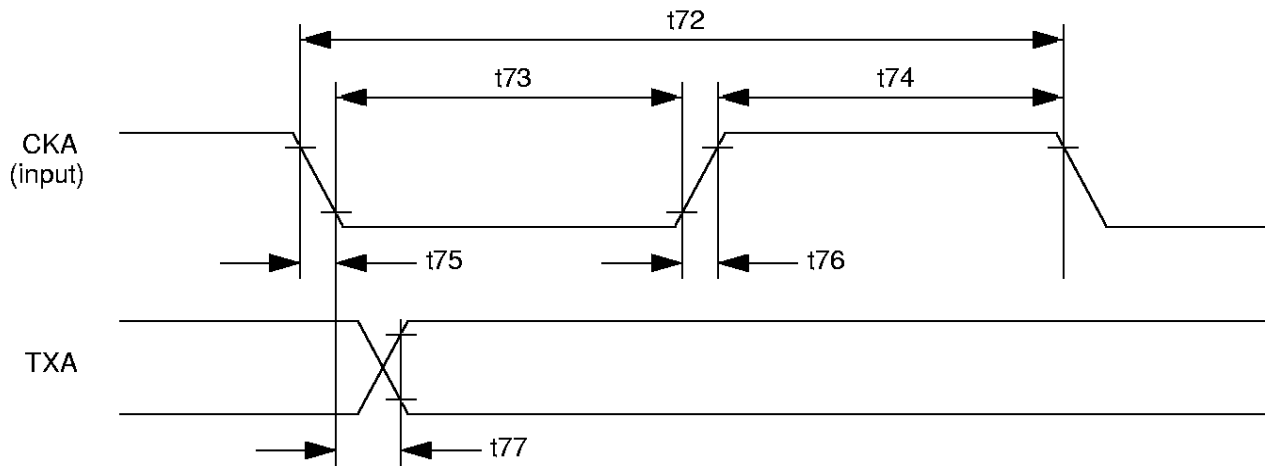


Figure 11. ASCII Transmitter Timing

ASCI Receiver Timing (See Figure 12)

Specifications apply over Standard Operating Conditions unless otherwise noted. $C_L = 50$ pF for outputs.

Symbol	Parameter	Z80382		Z8L382		Units
		Min.	Max.	Min.	Max.	
t79	External Receive Clock Period	50		50		ns
t80	External Receive Clock Low Time	30		30		ns
t81	External Receive Clock High Time	30		30		ns
t82	External Receive Clock Fall Time		5		10	ns
t83	External Receive Clock Rise Time		5		10	ns
t84	RXA Setup to CKA Rise	20		25		ns
t85	RXA Hold from CKA High	5		5		ns

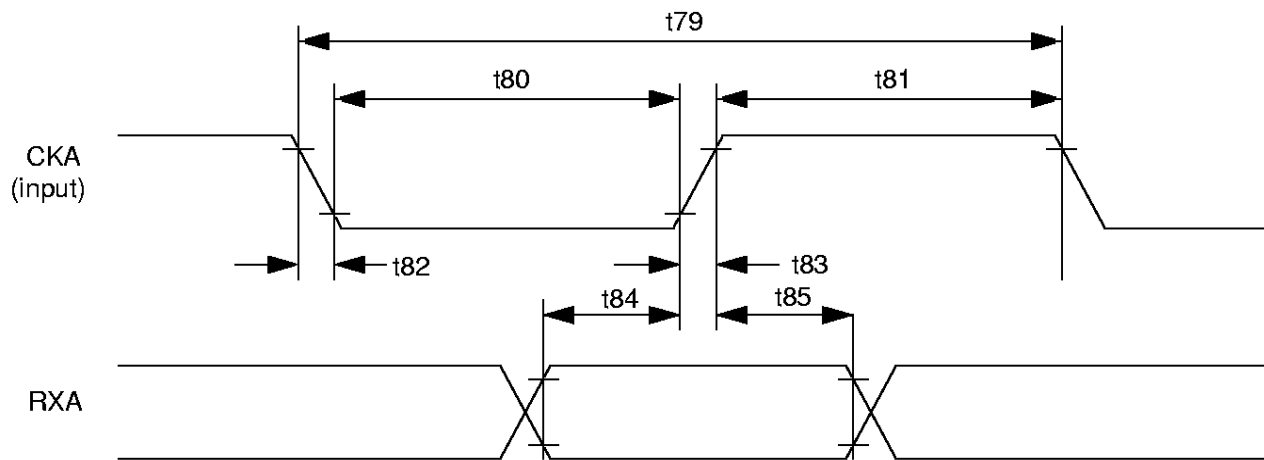


Figure 12. ASCII Receiver Timing

AC CHARACTERISTICS (Continued)

ASCII/CSIO Timing - Baud Rate Generator, /CTS_A, /DCDA, and /RTSA Timing
(See Figures 13, 14 and 15)

Specifications apply over Standard Operating Conditions unless otherwise noted. C_L = 50 pF for outputs.

Symbol	Parameter	Z80382		Z8L382		Units
		Min.	Max.	Min.	Max.	
t88	BUSCLK High to BRG Output Delay		30		40	ns
t89	BRG Output Fall Time		10		15	ns
t90	BRG Output Rise Time		10		15	ns
t91	/CTS Low Time	100		100		ns
t92	/CTS High Time	100		100		ns
t93	/DCD Low Time	100		100		ns
t94	/DCD High Time	100		100		ns
t95	BUSCLK Low to /RTS Valid		20		20	ns

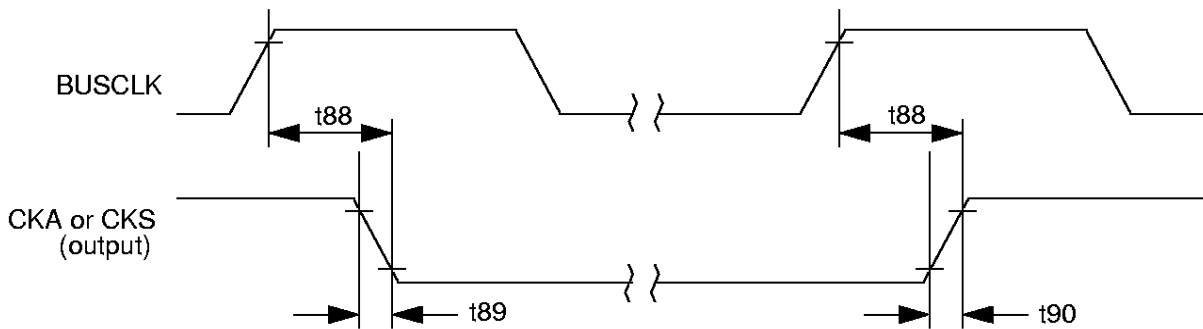


Figure 13. Baud Rate Generator Timing

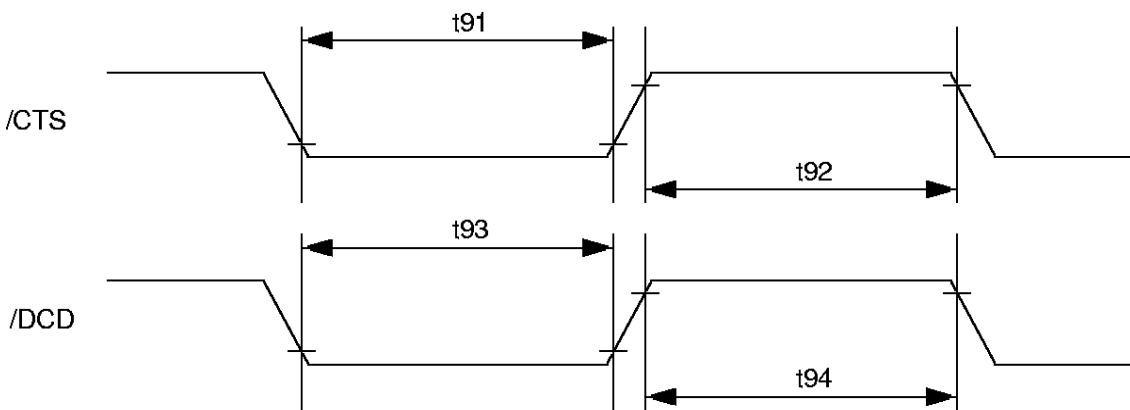


Figure 14. /CTSA and /DCDA Timing

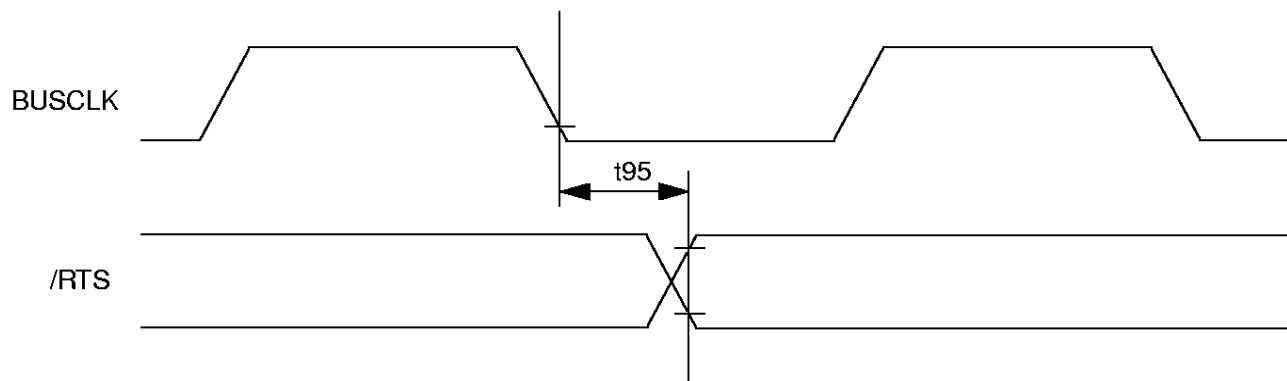


Figure 15. /RTSA Timing

AC CHARACTERISTICS (Continued)

General-Purpose I/O Port Timing. (See Figure 16)

Specifications apply over Standard Operating Conditions unless otherwise noted. $C_L = 50$ pF for outputs.

Symbol	Parameter	Z80382		Z8L382		Units
		Min.	Max.	Min.	Max.	
t100	I/O Port Data Setup to /IORD Fall	10		10		ns
t101	I/O Port Data Hold from /IORD High	5		5		ns
t102	I/O Port Data Valid from /IOWR High		20		20	ns

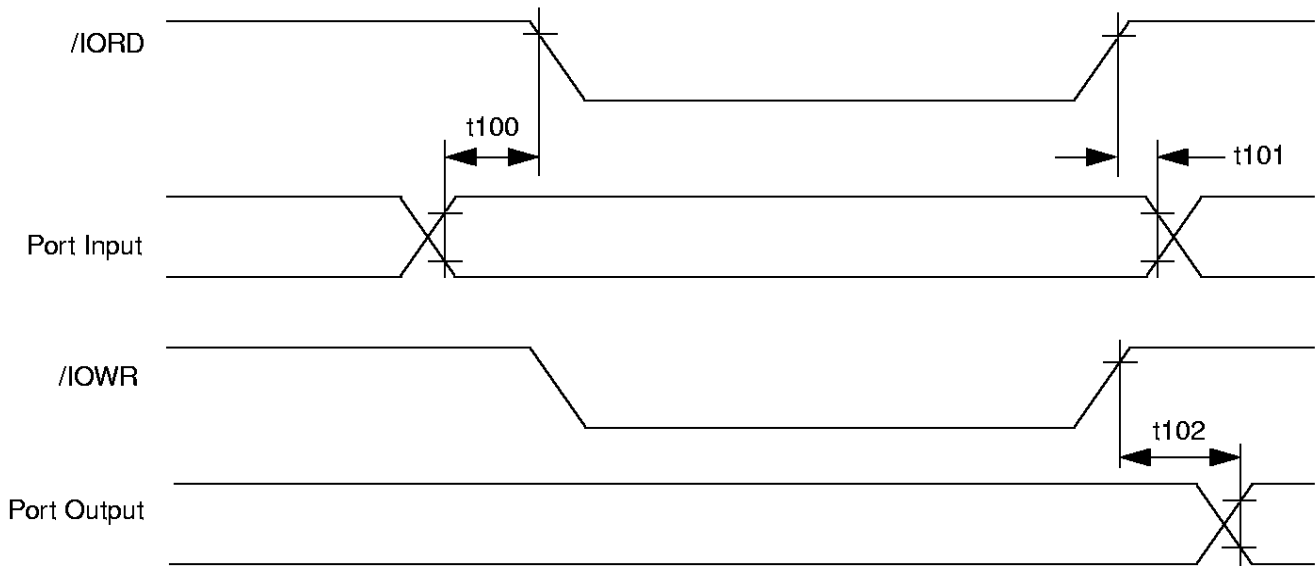
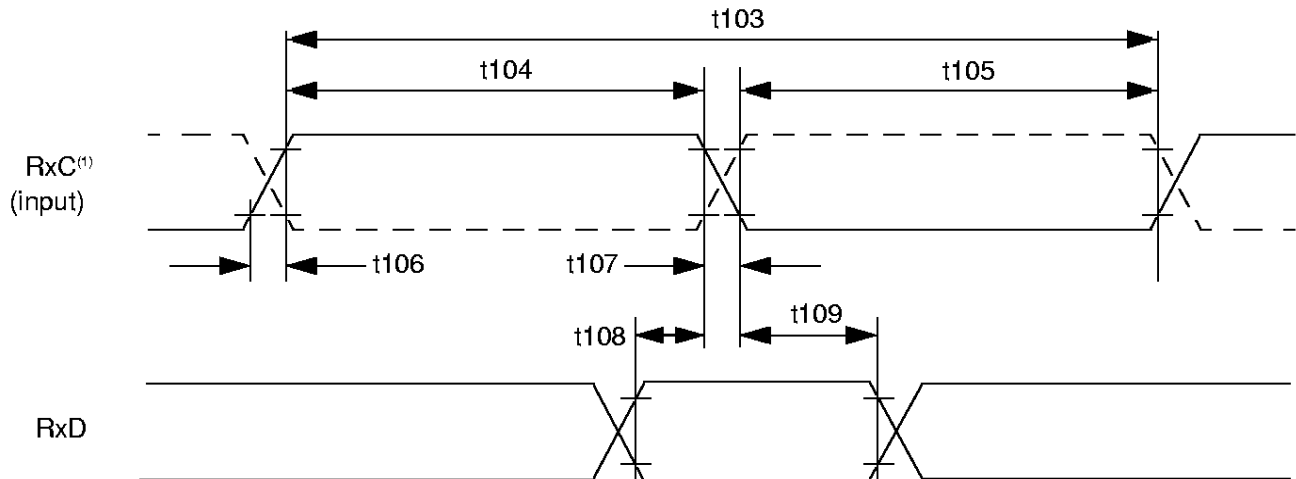


Figure 16. General-Purpose I/O Port Timing

HDLC Receive Timing- Full Time HDLC Mode (See Figures 17 and 18)

Specifications apply over Standard Operating Conditions unless otherwise noted. $C_L = 50$ pF for outputs.

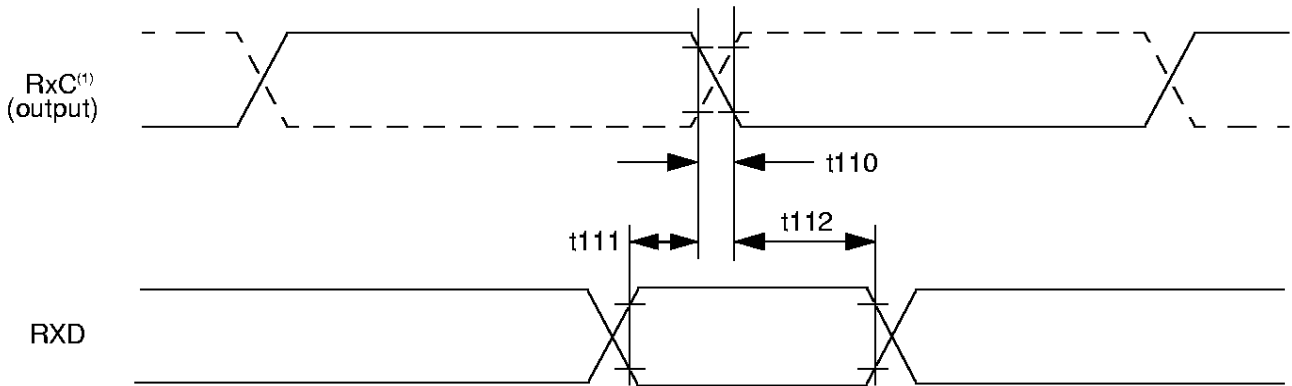
No	Parameter	Z80382		Z8L382		Units	Notes
		Min.	Max.	Min.	Max.		
t103	External Receive Clock Period	50		50		ns	1
t104	External Receive Clock Low Time	15		15		ns	
t105	External Receive Clock High Time	15		15		ns	
t106	External Receive Clock Rise Time		5		10	ns	
t107	External Receive Clock Fall Time		5		10	ns	
t108	RxD Setup to RxC Edge (External RxC)	20		20		ns	1
t109	RxD Hold from RxC Low/High (External RxC)	5		5		ns	1
t110	RxC rise/fall time (Internal RxC)		5		10	ns	1
t111	RxD Setup to RxC Edge (Internal RxC)	20		25		ns	1
t112	RxD Hold from RxC Low/High (Internal RxC)	5		10		ns	1

Note: 1. Receive clock sampling edge is configurable by means of RIRn[6]. See Z80382 User Manual.

Note 1. HDLC clock triggering polarity is configurable by means of RIRn[6]. See Z80382 User Manual.

Figure 17. HDLC Receive Timing (Full Time HDLC, RxC Input)

AC CHARACTERISTICS (Continued)



Note 1. Receive clock sampling edge is configurable by means of $RIRn[6]$. See Z80382 User Manual.

Figure 18. HDLC Receive Timing (Full Time HDLC, RxC Output)

HDLC Transmit Timing- Full Time HDLC Mode (See Figure 19)

Specifications apply over Standard Operating Conditions unless otherwise noted. $C_L = 50$ pF for outputs.

Symbol	Parameter	Z80382		Z8L382		Units
		Min.	Max.	Min.	Max.	
t113	External Transmit Clock Period	50		50		ns
t114	External Transmit Clock High Time	15		15		ns
t115	External Transmit Clock Low Time	15		15		ns
t116	External Transmit Clock Fall Time		5		10	ns
t117	External Transmit Clock Rise Time		5		10	ns
t118	TxC Low to TxD Data Valid		20		25	ns

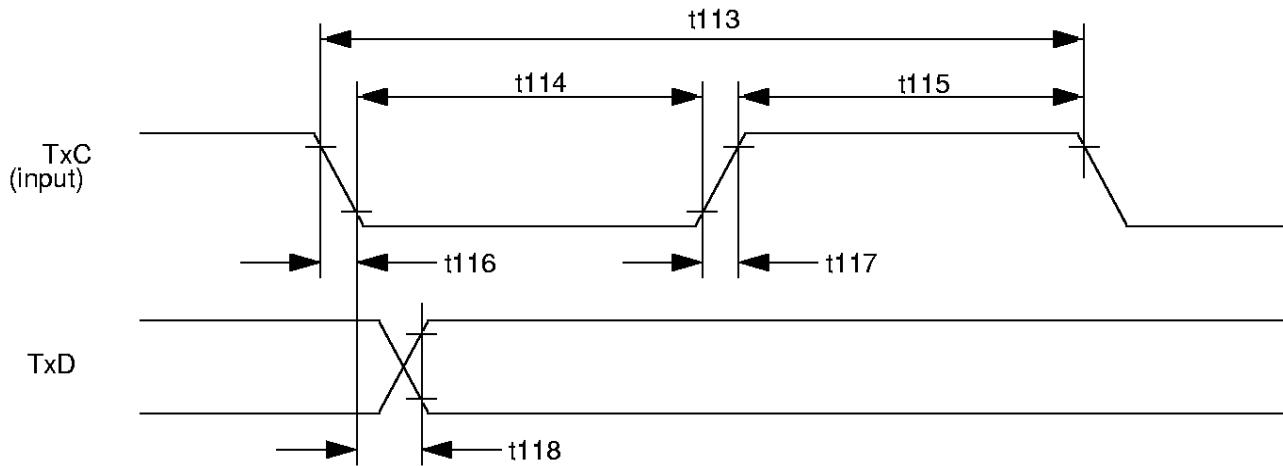


Figure 19. HDLC Transmit Timing (Full Time HDLC)

AC CHARACTERISTICS (Continued)

HDLC Timing - Non-GCI TDM mode (See Figure 20)

Specifications apply over Standard Operating Conditions unless otherwise noted. $C_L = 50$ pF for outputs.

Symbol	Parameter	Z80382		Z8L382		Units	Notes
		Min.	Max.	Min.	Max.		
t120	FSC Setup to BCL Fall	30		50		ns	
t121	FSC Hold from BCL Low	20		30		ns	
t122	BCL Period	50		50		ns	
t123	BCL High Time	15		15		ns	
t124	BCL Low Time	15		15		ns	
t125	BCL High to TxEN Low		15		20	ns	
t126	BCL High to TxEN High		15		20	ns	
t127	BCL High to TxD Valid		15		20	ns	
t128	BCL High to TxD Invalid	15		20		ns	
t129	RxD Setup to BCL Fall (Rise)	15		20		ns	1
t130	RxD Hold from BCL Low (High)	5		5		ns	1

Note: 1. Receive clock sampling edge is configurable by means of RIRn[6]. See Z80382 User Manual.

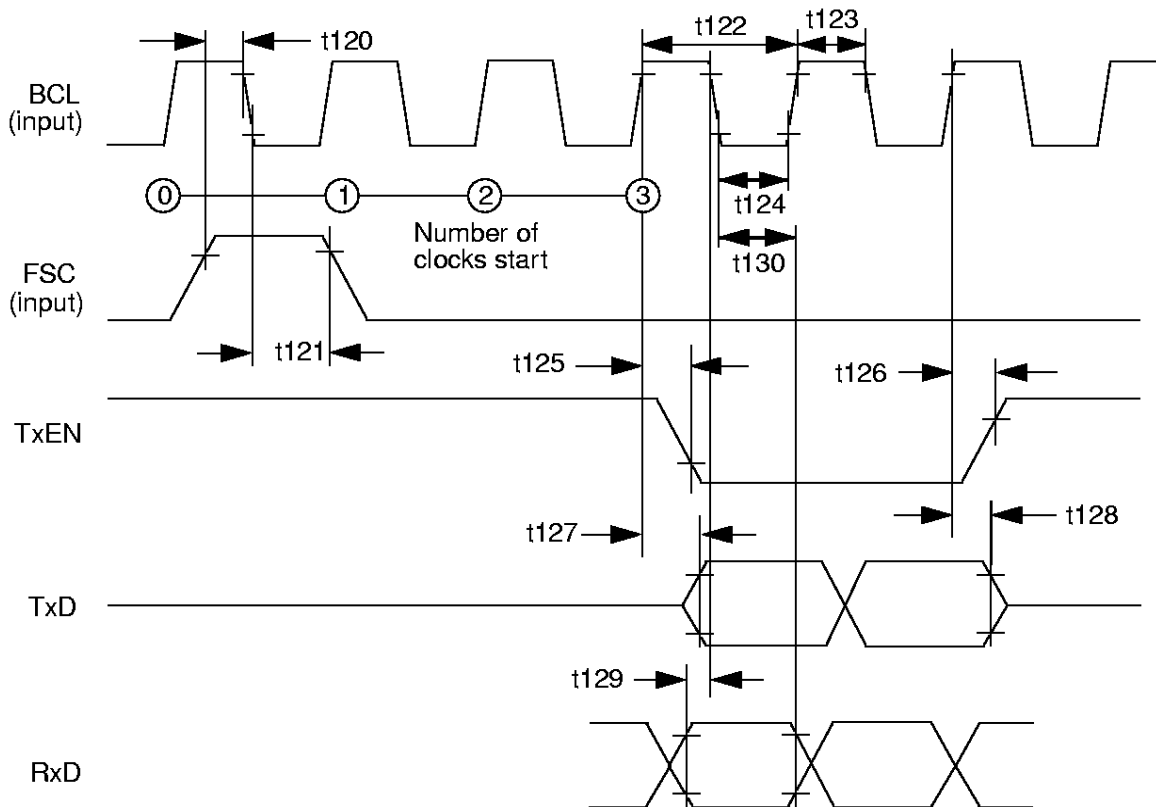


Figure 20. HDLC Timing - Non-GCI TDM Mode (Shown for Start = 3, Length = 2, Negative Edge RxD Sampling)

GCI/SCIT Timing - Slave Characteristics (See Figure 21)Specifications apply over Standard Operating Conditions unless otherwise noted. $C_L = 50$ pF for outputs.

Symbol	Parameter	Z80382		Z8L382		Units
		Min.	Max.	Min.	Max.	
t131	DCL Data Clock Rise/Fall Time		5		10	ns
t132	DCL Clock Period	50		50		ns
t133	DCL Pulse Width High and Low	15		15		ns
t134	FSC Setup to DCL Fall	30		30		ns
t135	FSC Hold from DCL Low	5		10		ns
t136	DCL High to DU/DD Transmit Data Valid		15		20	ns
t137	FSC High to DU/DD Transmit Data Valid		15		20	ns
t138	DU/DD Receive Data Setup to DCL Fall	15		20		ns
t139	DU/DD Receive Data Hold from DCL Low	0		0		ns

GCI/SCIT Timing - Master Characteristics (See Figure 21)Specifications apply over Standard Operating Conditions unless otherwise noted. $C_L = 50$ pF for outputs.

Symbol	Parameter	Z80382		Z8L382		Units
		Min.	Max.	Min.	Max.	
t131	DCL Data Clock Rise/Fall Time		5		10	ns
t132	DCL Clock Period	50		50		ns
t133	DCL Pulse Width High and Low	15		15		ns
t134	FSC Setup to DCL Fall	30		30		ns
t135	FSC Hold from DCL Low	5		10		ns
t136	DCL High to DU/DD Transmit Data Valid		15		20	ns
t137	FSC High to DU/DD Transmit Data Valid		15		20	ns
t138	DU/DD Receive Data Setup to DCL Fall	15		20		ns
t139	DU/DD Receive Data Hold from DCL Low	0		0		ns
t140	FSC High from DCL High	0		0		ns

AC CHARACTERISTICS (Continued)

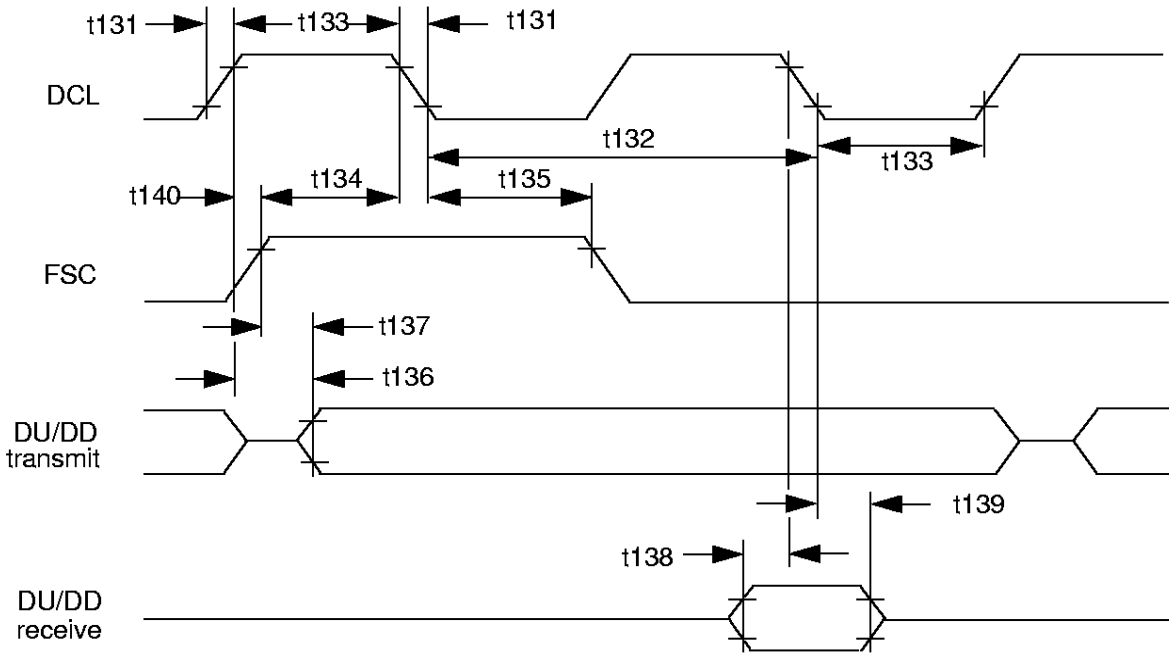


Figure 21. GCI/SCIT Slave and Master Timing

Z80382, SL1944 (DIE REVISION BB) ERROR REPORT - JUNE 23, 1997

The following includes all known anomalies in the Z80382, SL1944 as of the date above.

1. Decoding of the I/O Mailbox and Mimic addresses in ISA mode via the Plug-and-Play module is not functional. This version of the chip cannot be used in ISA bus applications. The cause of this problem has been determined and this anomaly will be corrected in the next die revision.
2. In the HDLC transmitter, "Request DMA service when the Transmit FIFO is half empty" functions like Request DMA service when one empty space is available in the Transmit FIFO". The cause of this problem has been determined and this anomaly will be corrected in the next die revision.
3. Long signal traces in routing the DCL input to the GCI module may cause signal reflections, which inadvertently trigger the internal logic and cause faulty operation. A 22-ohm series resistor at the DCL input appears to suppress the anomaly and is thus recommended.