# MH2M08BPNA-7,-8

## 16777216-BIT(2097152-WORD BY 8-BIT)PSEUDO-PSEUDO STATIC RAM

### DESCRIPTION

The MH2M08BPNA is 2097152-word × 8-bit PSEUDO-PSEUDO static RAM and consist of four industry standard 1M × 4 bit dynamic RAMs in SOJ, two data selector in SOP and one DRAM controller in SOP. The mounting of SOJ and SOP on a dual in-line package provides any application where high densities and large quantities of memory are required.

### FEATURES

| Type | Access time (max) Note 1 | power dissipation (typ) |
|---|---|---|
| MH2M08BPNA-7 | 106ns | 750mW |
| MH2M08BPNA-8 | 116ns | 650mW |

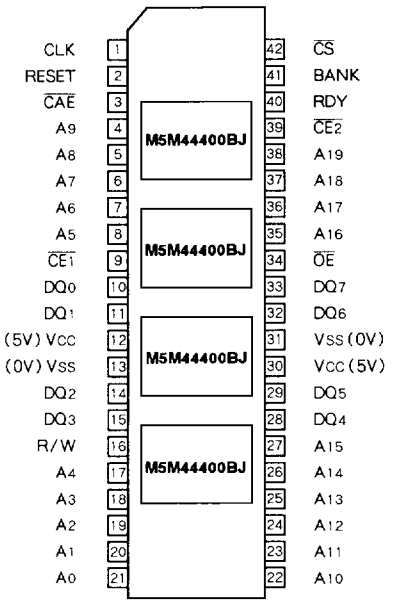
Note 1 : When Wait Operation, Access time is measured from end of T1 of clock.

- Single + 5V (± 10%) supply operation
- 42-pin 600 mil Dual in-line package
- No refresh
- All inputs and outputs are directly TTL compatible
- Includes (0.22 μF × 7) decoupling capacitors

### APPLICATION

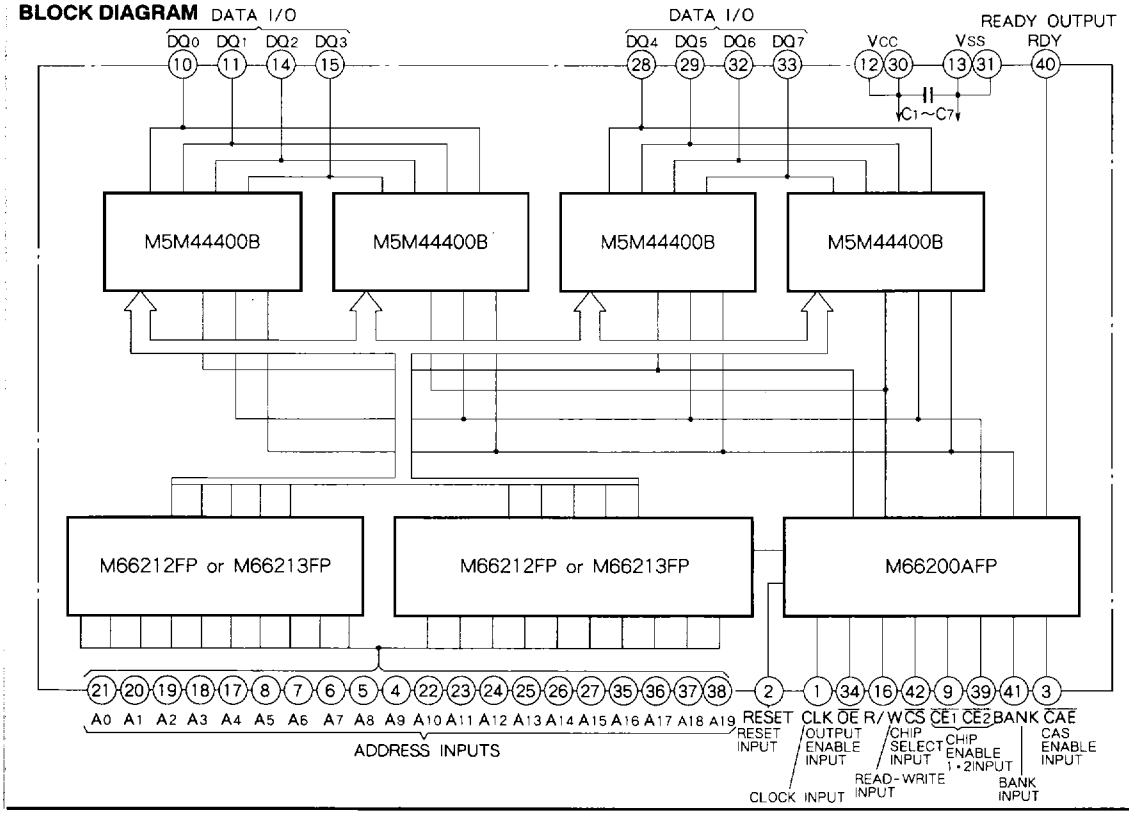
Small Capacity Memory Units

### PIN CONFIGURATION(TOP VIEW) [Both side]




Outline 42N1C

### BLOCK DIAGRAM



## 16777216-BIT(2097152-WORD BY 8-BIT)PSEUDO-PSEUDO STATIC RAM

### FUNCTION

MH2M08BPNA Series is 2097152 word by 8-bit. These devices operate on a single 5V supply, and all inputs and outputs are directly TTL compatible.

When DRAM centroller counted 117th clock pulse from CLK terminal, DRAM is automatically refreshed. Accordingly, Outside refreshing is not required.

Multiplexer enable to put separate address in as SRAM.

Internal action of the MH2M08BPNA is of the same period as clock pulse and 1 state(time of one read or write cycle) consists of 4 clock pulses.

A write cycle is executed whenever the low level $\overline{CE_1}$ overlaps with the low level $\overline{CS}$ at the last "H" → "L" edge of $T_1$(first clock pulse of write cycle). The address is determined by BANK and $A_0$~$A_{19}$.

The data is latched into a cell on the last "H" → "L" edge of $T_2$(second clock pulse of write cycle)requiring the set-up and hold time relative to this edge to be maintained.

A read cycle is executed whenever the low level $\overline{CE_2}$ overlaps with the low level $\overline{CS}$ at the last "H" → "L" edge of $T_1$. When address is determined by BANK and $A_0$~$A_{19}$ data situated on the address is read.

When setting $\overline{CS}$ at high level or $\overline{CE_1}$ and $\overline{CE_2}$ at the same time at high level, the chip is in a non-selectable mode in which both reading and writing are disabled. In this mode, the output stage is in floating state.

### DESCRIPTION OF PINS

| Symbol | I/O | Function |
|---|---|---|
| RESET | | Reset input<br>This input resets built-in flip and is active H. |
| CLK | | Clock input |
| $\overline{CS}$<br>$\overline{CE_1}$, $\overline{CE_2}$ | | Decode signal of CPU address<br>Status signal from CPU<br>The memory access cycle is started by $\overline{CS}$, $\overline{CE_1}$ and $\overline{CE_2}$ signals. |
| $\overline{OE}$ | | Read signal from CPU (assumed that read cycle finish) |
| R/W | | Write signal from CPU (assumed that write cycle finish) |
| BANK<br>$\overline{CAE}$ | | Determine the valid combination of $\overline{RAS}$, BANK change<br>Determine the valid combination of $\overline{CAS}$<br>$\overline{CAS}$ is output by active L. |
| $A_0$~$A_{19}$ | | Address signal |
| RDY | Output | Read signal to CPU |
| $DQ_0$~$_7$ | Input/Output | Data input/output signal |

| $\overline{CS}$ | $\overline{CE_1}$ | $\overline{CE_2}$ | Mode |
|---|---|---|---|
| H | Don't care | Don't care | No-access |
| L | L | L | Read |
| L | L | H | Write |
| L | H | L | Read |
| L | H | H | No-access |

| BANK | $\overline{CAE}$ | Memory area |
|---|---|---|
| Don't care | H | - |
| L | L | $BANK_0$ |
| H | L | $BANK_1$ |



MITSUBISHI ELECTRIC

## ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Condition | Ratings | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | With respect to $V_{SS}$ | −1~7.0 | V |
| $V_I$ | Input voltage | | −1~7.0 | V |
| $V_O$ | Output voltage | | −1~7.0 | V |
| $I_{IK}$ | Input protection diode current | $V_I$ < 0V | −20 | mA |
| | | $V_I$ > $V_{CC}$ | +20 | |
| $I_O$ | Output current | | 50 | mA |
| $P_d$ | Power dissipation | Ta = 25℃ | 3500 | mW |
| $T_{opr}$ | Operating temperature | | 0~70 | ℃ |
| $T_{stg}$ | Storage temperature | | −40~125 | ℃ |

## RECOMMENDED OPERATING CONDITIONS (Ta = 0~70℃ unless otherwise noted) (Note 2)

| Symbol | Parmeter | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| $V_{SS}$ | Supply voltage | | 0 | | V |
| $V_I$ | Input voltage | 0 | | $V_{CC}$ | V |
| $V_O$ | Output voltage | 0 | | $V_{CC}$ | V |

Note 2 : All voltage values are with respect to $V_{SS}$.

## ELECTRICAL CHARACTERISTICS (Ta = 0~70℃, $V_{CC}$ = 5V ± 10%, $V_{SS}$ = 0V, unless otherwise noted) (Note 3)

| Symbol | Parameter | | Test conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | |
| $V_{T+}$ | Threshold voltage (RESET) | | $V_O$ = 0.1, $V_{CC}$ − 0.1V, $I_O$ = 20 μA | | | 2.4 | V |
| $V_{T-}$ | Threshold voltage (RESET) | | $V_O$ = 0.1, $V_{CC}$ − 0.1V, $I_O$ = 20 μA | 0.6 | | | V |
| $V_{T+}$-$V_{T-}$ | Hysteresis width (RESET) | | $V_O$ = 0.1, $V_{CC}$ − 0.1V, $I_O$ = 20 μA | 0.2 | | 1.8 | V |
| $V_{IH}$ | High input voltage (other input) | | $V_O$ = 0.1, $V_{CC}$ − 0.1V, $I_O$ = 20 μA | 2.4 | | | V |
| $V_{IL}$ | Low input voltage (other input) | | $V_O$ = 0.1, $V_{CC}$ − 0.1V, $I_O$ = 20 μA | | | 0.8 | V |
| $V_{OH}$ | High output voltage | | $I_{OH}$ = − 5mA | 2.4 | | $V_{CC}$ | V |
| $V_{OL}$ | Low output voltage | | $I_{OL}$ = 4.2mA | 0 | | 0.4 | V |
| $I_{IH}$ | High input current | | $V_I$ = $V_{CC}$ | | | 1.0 | μA |
| $I_{IL}$ | Low input current | | $V_I$ = GND | | | 1.0 | μA |
| $I_{CC1(AV)}$ | Average supply current from $V_{CC}$ operating (Note 4, 5) | MH2M08BPNA-7 | Maximum repeating frequency, output open | | | 175 | mA |
| | | MH2M08BPNA-8 | | | | 155 | |
| $I_{CC2(1)}$ | Average supply current from $V_{CC}$, stand by | | $V_I$ = 2.4V, 0.4V, Output open (Note 6) | | | 16.7 | mA |
| $I_{CC2(2)(AV)}$ | | | $V_I$ = $V_{CC}$, GND, f = 10MHz, Output open (Note 4, 7) | | 7 | | mA |
| $I_{CC3(AV)}$ | Average supply current from VCC, $\overline{CAS}$ before $\overline{RAS}$ refreshing (Note 4) | MH2M08PNA-7 | Refresh cycling, output open (5 clock from 117th clock) | | | 175 | mA |
| | | MH2M08PNA-8 | | | | 155 | |
| $C_{I(A)}$ | Input capacitance, address inputs | | $V_I$ = $V_{SS}$, f = 1MHz $V_i$ = 25mVrms | | | 16 | pF |
| $C_I$ | Input capacitance (exept address inputs) | | | | | 17 | pF |
| $C_{(DQ)}$ | Input/output capacitance, Data input/output inputs | | | | | 25 | pF |
| $C_{O(RDY)}$ | Output capacitance, RDY inputs | | $V_o$ = $V_{SS}$, f = 1MHz, $V_i$ = 25mVrms | | | 10 | pF |

Note 3 : Current flowing into IC is positive, out is negative.
4 : $I_{CC1(AV)}$, $I_{CC2(2)(AV)}$, $I_{CC3(AV)}$ are dependent on frequency of clock pulse. Limits are measured at maximum frequency.
5 : $I_{CC1(AV)}$ is dependent on output loading specified values are obtained with the output open.
6 : Only one input set to this value, all other input fix $V_{CC}$ or GND.
7 : The value is setting to $I_{CC3}$, when it get in refresh cycle every 121 clock.

**SWITCHING CHARACTERISTICS** ($T_a$ = 0~70℃, $V_{CC}$ = 5V ± 10%, $V_{SS}$ = 0V, unless otherwise noted) (Note 8)

| Symbol | Parameter | Limits | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | MH2M08BPNA-7 | | | MH2M08BPNA-8 | | | |
| | | Min | Typ | Max | Min | Typ | Max | |
| f | Repeating frequency | 3.8 | | 16.7 | 3.8 | | 14.5 | MHz |
| $t_{PLH}$ | CLK, $\overline{OE}$, R/W-RDY propagation time (Note 9) | | | 36 | | | 36 | ns |
| $t_{PHL}$ | | | | 36 | | | 36 | ns |
| $t_{CKA}$ | CLK access time | | | 106 | | | 116 | ns |
| $t_{OFF}$ | Output disable time after $\overline{OE}$ high | 40 | | 60 | 40 | | 60 | ns |

Note 8 : After power-up an initial pause of 500 $\mu$s and dummy cycle (Read or Write cycle by 8 times degrees) followed by CLK, $\overline{CS}$, $\overline{CE1}$, $\overline{CE2}$, $\overline{OE}$, R/W cycles are required before proper device operation is achieved. It may add that cycle during the initial pause, but dummy cycle is required.

9 : The values are measured at loading capacitance $C_L$ = 50pF.

**TIMING REQUIREMENTS** ($T_a$ = 0~70℃, $V_{CC}$ = 5V ± 10%, $V_{SS}$ = 0V, unless otherwise noted) (Notes 10, 11)

**Read, Write, Refresh Mode Cycle**

| Symbol | Parameter | Limits | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | MH2M08BPNA-7 | | | MH2M08BPNA-8 | | | |
| | | Min | Typ | Max | Min | Typ | Max | |
| $t_{CKL}$ | CLK low pulse width | 25 | | 50 | 35 | | 60 | ns |
| $t_{CKH}$ | CLK high pulse width | 25 | | 50 | 35 | | 60 | ns |
| $t_{CSS}$ | CLK-$\overline{CS}$ setup time | 20 | | | 20 | | | ns |
| $t_{CSH}$ | CLK-$\overline{CS}$ hold time | 20 | | | 20 | | | ns |
| $t_{CE1S}$ | CLK-$\overline{CE_1}$ setup time | 20 | | | 20 | | | ns |
| $t_{CE1H}$ | CLK-$\overline{CE_1}$ hold time | 20 | | | 20 | | | ns |
| $t_{CE2S}$ | CLK-$\overline{CE_2}$ setup time | 20 | | | 20 | | | ns |
| $t_{CE2H}$ | CLK-$\overline{CE_2}$ hold time | 20 | | | 20 | | | ns |
| $t_{OES}$ | CLK-$\overline{OE}$ setup time | 20 | | | 20 | | | ns |
| $t_{OEH}$ | CLK-$\overline{OE}$ hold time | 1.5CK+10 | | 2.5CK-20 | 1.5CK+10 | | 2.5CK-20 | ns |
| $t_{RWS}$ | CLK-R/W setup time | 20 | | | 20 | | | ns |
| $t_{RWH}$ | CLK-R/W hold time | 1.0CK+10 | | 2.0CK-20 | 1.0CK+10 | | 2.0CK-20 | ns |
| $t_{AS}$ | CLK-ADDRESS setup time | 20 | | | 20 | | | ns |
| $t_{AH}$ | CLK-ADDRESS hold time (READ) (READ)<br>CLK-ADDRESS hold time (WRITE) (WRITE) | 50<br>0.5CK+50 | | | 50<br>0.5CK+50 | | | ns |
| $t_{BKS}$ | CLK-BANK setup time | 20 | | | 20 | | | ns |
| $t_{BKH}$ | CLK-BANK hold time | 20 | | | 20 | | | ns |
| $t_{CAS}$ | CLK-$\overline{CAE}$ setup time | 20 | | | 20 | | | ns |
| $t_{CAH}$ | CLK-$\overline{CAE}$ hold time | 20 | | | 20 | | | ns |
| $t_{DS}$ | CLK-DATA setup time | 0 | | | 0 | | | ns |
| $t_{DH}$ | CLK-DATA hold time | 50 | | | 50 | | | ns |
| $t_T$ | Transition time (Note12) | 1 | | 50 | 1 | | 50 | ns |
| $t_{REF}$ | Refresh cycle time (every 121 clocks) | 8.5 | | 15.7 | 9.7 | | 15.7 | $\mu$s |

Note 10 : The timing requirements are assumed $t_T$ = 5ns.

11 : $V_T$ = 1.3V is reference levels for measuring timing of input signals.

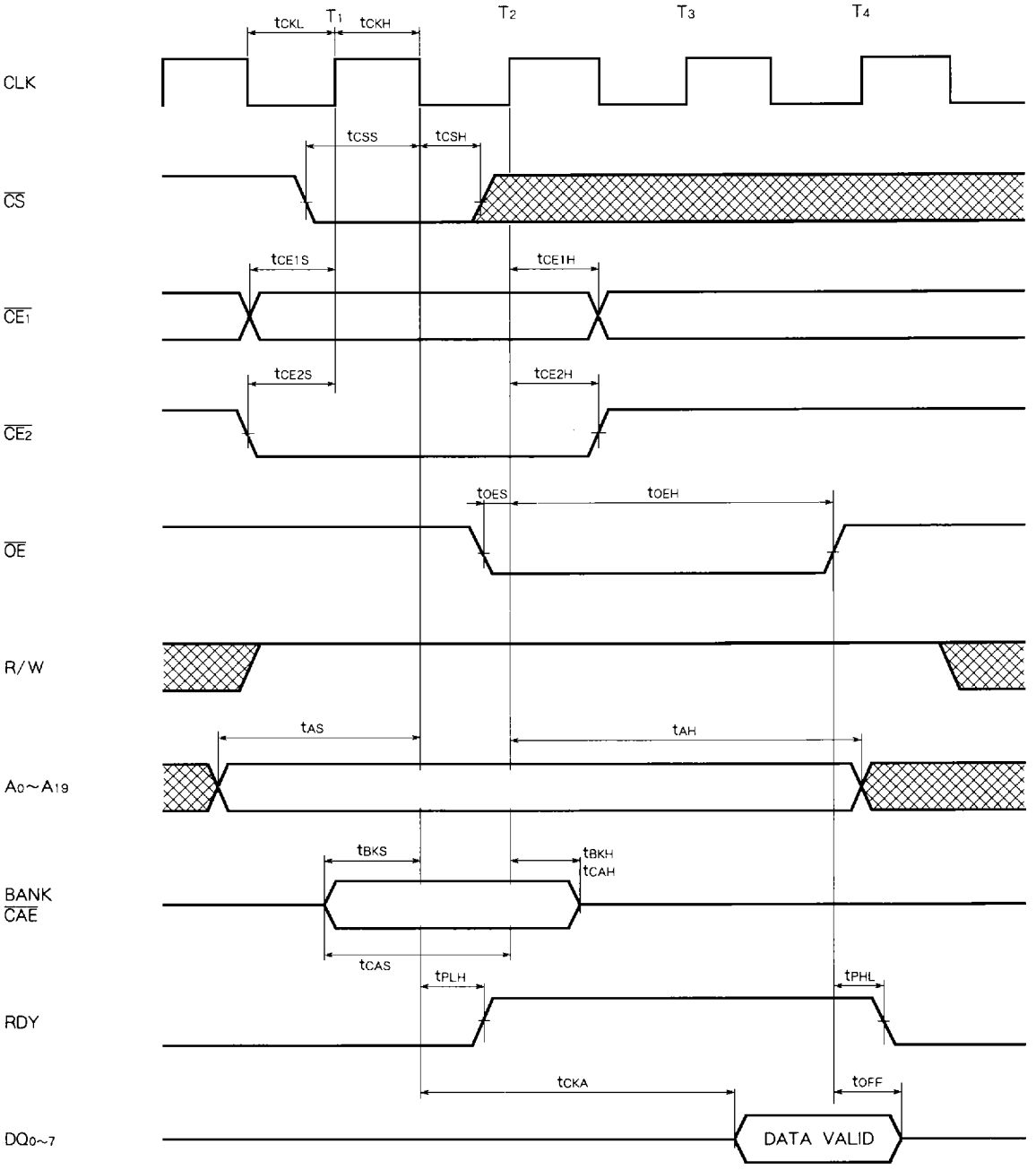
12 : $t_T$ is measured between $V_{IH}$ (min) and $V_{IL}$ (max).

**Reset-Mode-Cycle**

| Symbol | Parameter | Limits | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | MH2M08BPNA-7 | | | MH2M08BPNA-8 | | | |
| | | Min | Typ | Max | Min | Typ | Max | |
| $t_{REW}$ | RESET pulse width | 20 | | | 20 | | | ns |
| $t_{REC}$ | CLK-RESET recovery time | 20 | | | 20 | | | ns |

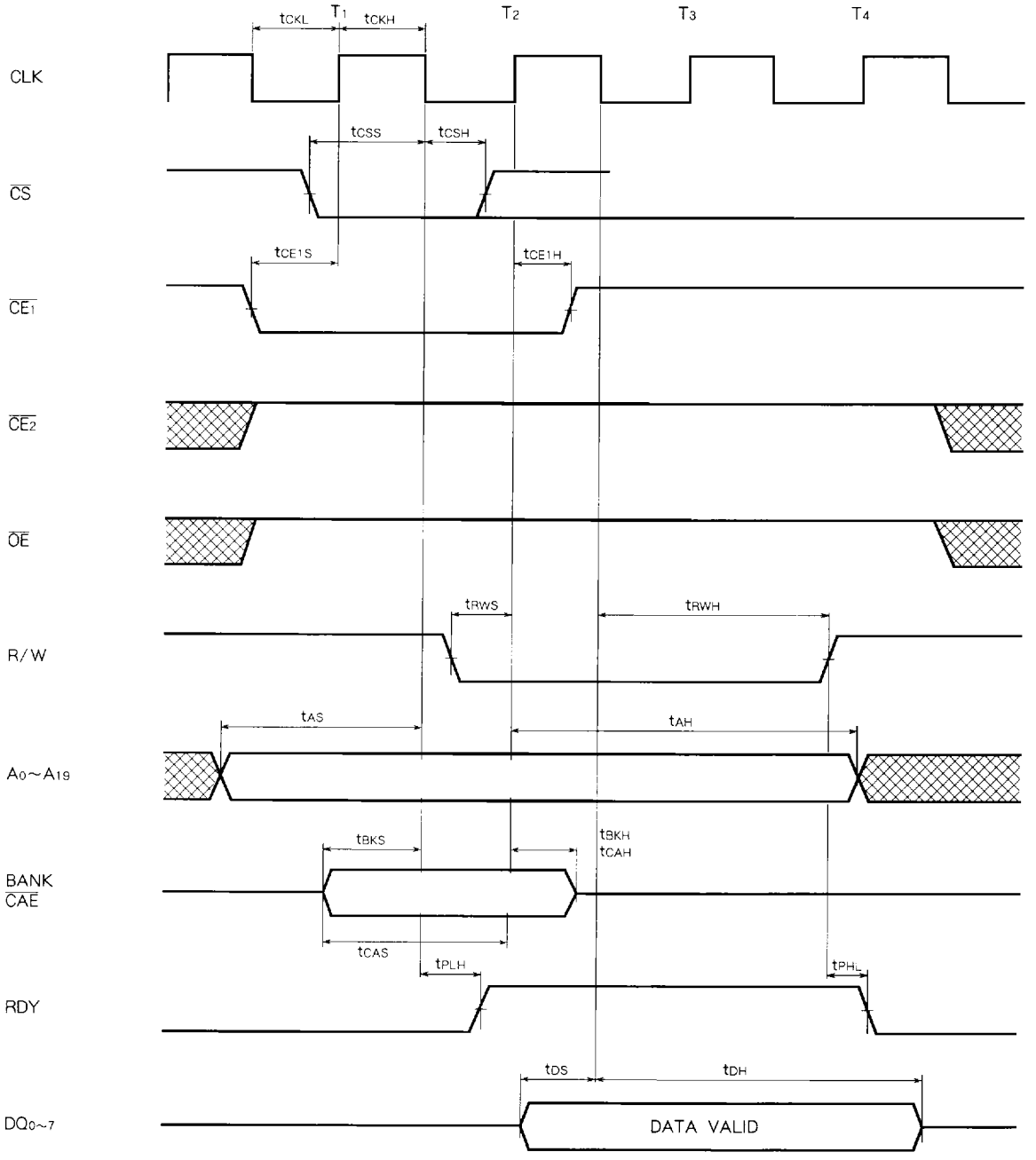
**TIMINNG DIAGRAM** (Note 13)

**Read Cycle**

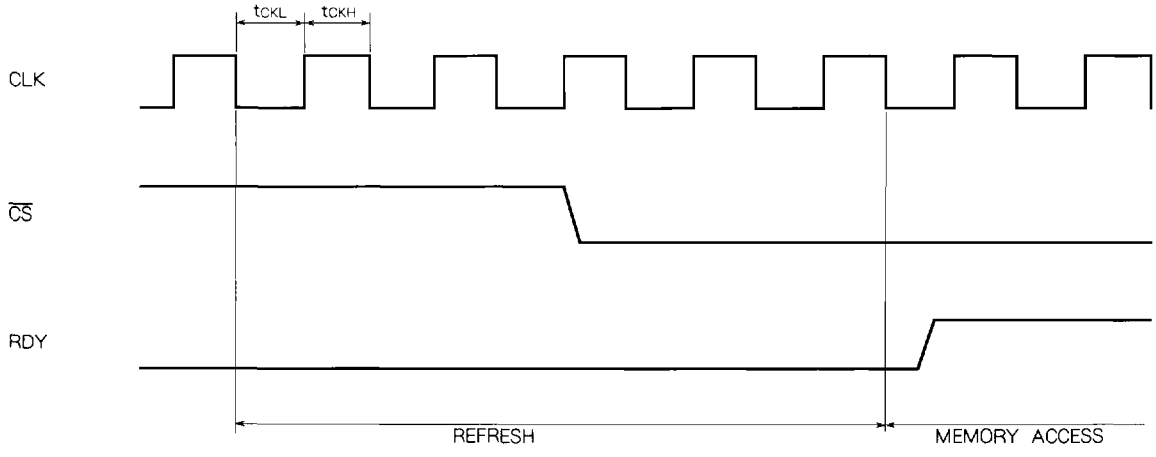



Note 13 Indicates the don't care input.

**Write Cycle**


T1
T2
T3
T4
tCKL
tCKH
CLK
tCSS
tCSH
CS
tCE1S
tCE1H
CE1
CE2
OE
tRWS
tRWH
R/W
tAS
tAH
A0~A19
tBKS
tBKH
tCAH
BANK
CAE
tCAS
tPLH
tPHL
RDY
tDS
tDH
DQ0~7
DATA VALID

**Refresh Cycle** (Note 14)




Note 14 : While refresh cycle, other input signal are waiting condition.

**Reset Cycle**