

Sound fader control circuit

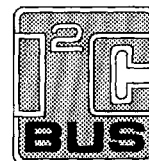
TEA6320

FEATURES

- Source selector for four stereo and one mono inputs
- Interface for noise reduction circuits
- Interface for external equalizer
- Volume, balance and fader control
- Special loudness characteristic automatically controlled in combination with volume setting
- Bass and treble control
- Mute control at audio signal zero crossing
- Fast mute control via I²C-bus
- Fast mute control via pin
- I²C-bus control for all functions
- Power supply with internal power-on reset

GENERAL DESCRIPTION

The sound fader control circuit TEA6320 is an I²C-bus controlled stereo preamplifier for car radio hi-fi sound applications.



QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V _{CC}	positive supply voltage		7.5	8.5	9.5	V
I _{CC}	supply current	V _{CC} = 8.5 V	–	26	–	mA
V _{O(RMS)}	maximum output voltage level	V _{CC} = 8.5 V; THD ≤ 0.1%	–	2000	–	mV
G _v	volume gain		–86	–	+20	dB
G _{step}	step resolution (volume)		–	1	–	dB
G _b	bass control		–15	–	+15	dB
G _t	treble control		–12	–	+12	dB
G _{step}	step resolution (bass, treble)		–	1.5	–	dB
(S+N)/N	signal-plus-noise to noise ratio	V _O = 2.0 V; G _v = 0 dB; unweighted	–	105	–	dB
RR ₁₀₀	ripple rejection	V _{r(RMS)} < 200 mV; f = 100 Hz; G _v = 0 dB	–	75	–	dB
α _{CS}	channel separation	250 Hz ≤ f ≤ 10 kHz; G _v = 0 dB	90	96	–	dB

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TEA6320	32	SDIL	plastic	SOT232AG
TEA6320T	32	SO	plastic	SOT287AH

Sound fader control circuit

TEA6320

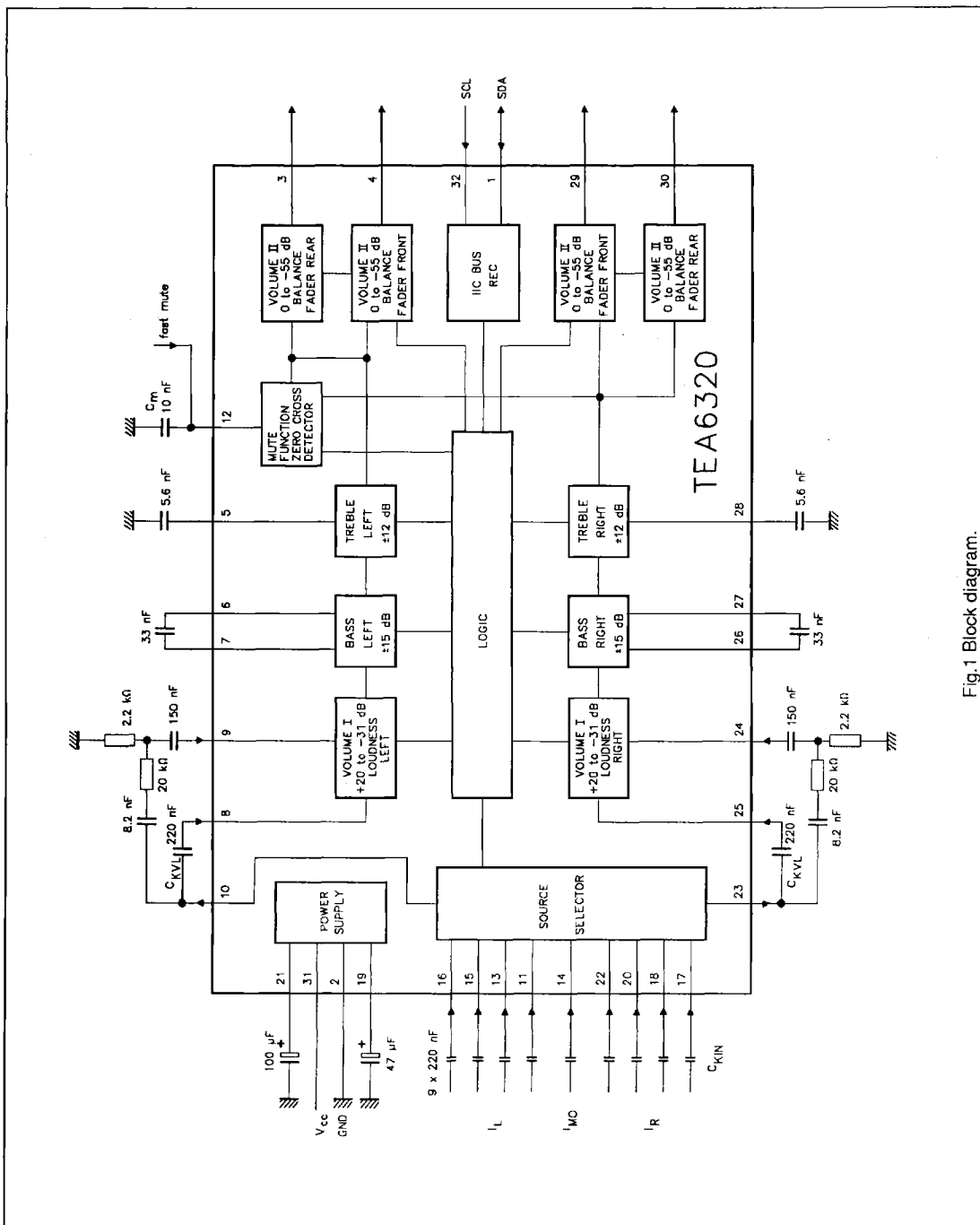


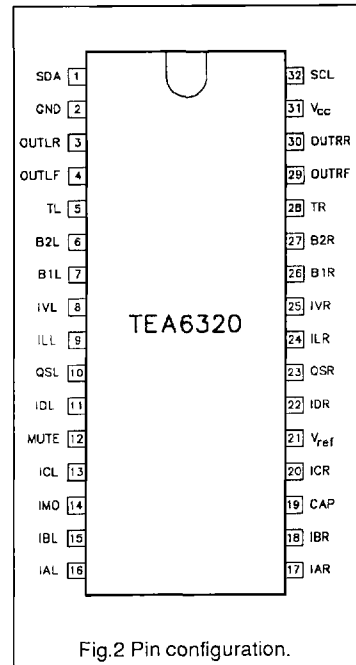
Fig.1 Block diagram.

Sound fader control circuit

TEA6320

PINNING

SYMBOL	PIN	DESCRIPTION
SDA	1	serial data input/output
GND	2	ground
OUTLR	3	output left rear
OUTLF	4	output left front
TL	5	treble control capacitor left channel or input from an external equalizer
B2L	6	bass control capacitor left channel or output to an external equalizer
B1L	7	bass control capacitor, left channel
IVL	8	input volume I, left control part
ILL	9	input loudness, left control part
QSL	10	output source selector, left channel
IDL	11	input D left source
MUTE	12	mute control
ICL	13	input C left source
IMO	14	input mono source
IBL	15	input B left source
IAR	17	input A right source
IBR	18	input B right source
CAP	19	electronic filtering for supply
ICR	20	input C right source
V _{ref}	21	reference voltage (0.5V _{CC})
IDR	22	input D right source
QSR	23	output source selector right channel
ILR	24	input loudness right channel
IVR	25	input volume I, right control part
B1R	26	bass control capacitor right channel
B2R	27	bass control capacitor right channel or output to an external equalizer
TR	28	treble control capacitor right channel or input from an external equalizer
OUTRF	29	output right front
OUTRR	30	output right rear
V _{CC}	31	supply voltage
SCL	32	serial clock input



Sound fader control circuit

TEA6320

FUNCTIONAL DESCRIPTION

The source selector selects one of 4 stereo inputs or the mono input. The maximum input signal voltage is $V_{i(RMS)} = 2$ V. The outputs of the source selector and the inputs of the following volume control parts are available at pins 8 and 10 for the left channel and pins 23 and 25 for the right channel. This offers the possibility of interfacing a noise reduction system.

The volume control function is split into two sections: volume I control block and volume II control block.

The control range of volume I is between +20 dB and -31 dB in steps of 1 dB. The volume II control range is between 0 dB and -55 dB in steps of 1 dB. Although the theoretical possible control range is 106 dB (+20 dB to -86 dB), in practice a range of 86 dB (+20 dB to -66 dB) is recommended. The gain/attenuation setting of the volume I control blocks is common for both channels.

The volume I control blocks operate in combination with the loudness control. The filter is linear when the maximum gain for the volume I control (+20 dB) is selected. The filter characteristic increases automatically over a range of 32 dB down to a setting of -12 dB. That means the maximum filter characteristic is obtained at -12 dB setting of volume I. Further reduction of the volume does not further influence the filter characteristic (see Fig.5). The maximum selected filter characteristic is determined by external components. The proposed application gives a maximum boost of 17 dB for bass and 4.5 dB for treble. The loudness may be switched on or off via I²C-bus control (Table 7).

The volume I control block is followed by the bass control block. A single external capacitor of 33 nF for each channel in combination with internal resistors, provides the frequency response of the bass control (see Fig.3). The adjustable range is between -15 dB and +15 dB in steps of 1.5 dB at 40 Hz.

Both, loudness and bass control result in a maximum bass boost of 32 dB for low volume settings.

The treble control block offers a control range between -12 dB and +12 dB in steps of 1.5 dB at 15 kHz. The filter characteristic is determined by a single capacitor of 5.6 nF for each channel in combination with internal resistors (see Fig.4).

The basic step width of bass and treble control is 3 dB. The intermediate steps are obtained by switching 1.5 dB boost and 1.5 dB attenuation steps.

The bass and treble control functions can be switched off via I²C-bus. In this event the internal signal flow is disconnected. The connections B2L / B2R are outputs and TL / TR are inputs for inserting an external equalizer.

The last section of the circuit is the volume II block. The balance and fader functions are performed using the same control blocks. This is realized by 4 independently controllable attenuators, one for each output. The control range of these attenuators is 55 dB in steps of 1 dB with an additional mute step.

The circuit provides 3 mute modes.

- 1) Zero crossing mode mute via I²C-bus using 2 independent zero crossing detectors (ZCM, see Tables 2 and 9 and Fig.15).
- 2) Fast mute via mute pin (see Fig.9).

- 3) Fast mute via I²C-bus either by general mute (GMU see Tables 2 and 9) or volume II block setting (see Table 4).

The mute function is performed immediately if ZCM is cleared (ZCM = 0). If the bit is set (ZCM = 1) the mute is activated after changing the GMU bit. The actual mute switching is delayed until the next zero crossing of the audio frequency signal. As the two audio channels (left and right) are independent, two comparators (window detectors) are required to control independent mute switches.

To avoid a large delay of the muting switching when very low frequencies are processed, the maximum delay time is limited to typically 100 ms by an integrated timing circuit and an external capacitor ($C_m = 10$ nF, see Fig.9). This timing circuit is triggered by reception of a new data word for the switch function which includes the GMU bit. After a discharge and charge period of an external capacitor the muting switch follows the GMU bit if no zero crossing was detected during that time.

The mute function can also be controlled externally. If the mute pin is switched to ground all outputs are muted immediately (hardware mute). This mute request overwrites all mute controls via the I²C-bus for the time the pin is held low. The hardware mute position is not stored in the TEA6320.

For the turn on/off behaviour the following explanation is generally valid. To avoid AF output caused by the input signal coming from preceding stages, which produce output during drop of V_{CC} . The mute has to be set, before the V_{CC} will drop. This can be achieved by I²C-bus control or by grounding the mute pin.

Sound fader control circuit

TEA6320

For use where there is no mute in the application before turn off, a supply voltage drop of more than $1 \times V_{BE}$ will result in a mute during the voltage drop.

The power supply should include a V_{CC} buffer capacitor, which provides a discharging time constant. If the input signal does not disappear after turn off the input will become audible after a certain time. A $4.7 \text{ k}\Omega$ resistor discharges the V_{CC} buffer capacitor, because the internal current of the IC does not discharge it completely.

The hardware mute function is favourable for use in RDS (Radio Data System) applications. The zero crossing mute avoids modulation plops. This feature is an advantage for mute during changing presets and/or sources (e. g. traffic announcement during cassette playback).

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage		0	10	V
T_{amb}	operating ambient temperature range		-40	+85	°C
T_{stg}	storage temperature range		-65	+150	°C
V_{es}	electrostatic handling	see note 1			
V_n	voltage at pins: pin 1 to 2 and 3 - 32 to 2		0	V_{CC}	V

Note to the limiting values

- Human body model: $C = 100 \text{ pF}$; $R = 1.5 \text{ k}\Omega$; $V \geq 2 \text{ kV}$
Charge device model: $C = 200 \text{ pF}$; $R = 0 \text{ }\Omega$; $V \geq 500 \text{ V}$

Sound fader control circuit

TEA6320

CHARACTERISTICS

$V_{CC} = 8.5 \text{ V}$; $R_S = 600 \ \Omega$, $R_L = 10 \text{ k}\Omega$, $C_L = 2.5 \text{ nF}$, AC coupled; $f = 1 \text{ kHz}$; $T_{amb} = +25 \text{ }^\circ\text{C}$; gain control $G_v = 0 \text{ dB}$; bass linear; treble linear; fader off; balance in mid position; loudness off; unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage		7.5	8.5	9.5	V
I_{CC}	supply current		–	26	33	mA
V_{DC}	internal DC voltage at inputs and outputs		3.83	4.25	4.68	V
V_{ref}	internal reference voltage at pin 21		–	4.25	–	V
G_v	maximum voltage gain	$R_S = 0 \ \Omega$; $R_L = \infty$	19	20	21	dB
$V_{O(RMS)}$	output voltage level for P_{max} at the power output stage start of clipping	THD $\leq 0.1\%$; see Fig.10 THD = 1% $R_L = 2 \text{ k}\Omega$; $C_L = 10 \text{ nF}$; THD = 1%	– 2300 2000	2000 – –	– – –	mV mV mV
$V_{i(RMS)}$	input sensitivity	$V_o = 2000 \text{ mV}$; $G_v = 20 \text{ dB}$	–	200	–	mV
B	roll-off frequencies	$C_{KIN} = 220 \text{ nF}$; $C_{KVL} = 220 \text{ nF}$; $Z_i = Z_{i \text{ min}}$ low frequency (–1 dB) low frequency (–3 dB) high frequency (–1 dB) $C_{KIN} = 470 \text{ nF}$; $C_{KVL} = 100 \text{ nF}$; $Z_i = Z_{i \text{ typ}}$ low frequency (–3 dB)	60 30 20000 17	– – – –	– – – –	Hz Hz Hz Hz
α_{CS}	channel separation	$V_i = 2 \text{ V}$; frequency range 250 Hz to 10 kHz	90	96	–	dB
THD	total harmonic distortion	frequency range 20 Hz to 12.5 kHz $V_i = 100 \text{ mV}$; $G_v = 20 \text{ dB}$ $V_i = 1000 \text{ mV}$; $G_v = 0 \text{ dB}$ $V_i = 2000 \text{ mV}$; $G_v = 0 \text{ dB}$ $V_i = 2000 \text{ mV}$; $G_v = -10 \text{ dB}$	– – – –	0.1 0.05 0.1 0.1	– tbn – –	% % % %
RR	ripple rejection	$V_{i(RMS)} < 200 \text{ mV}$ $f = 100 \text{ Hz}$ $f = 40 \text{ Hz to } 12.5 \text{ kHz}$	tbn –	76 66	– –	dB dB
(S+N)/N	signal-plus-noise to noise ratio	unweighted; 20 Hz to 20 kHz RMS; $V_o = 2.0 \text{ V}$; see Fig.6 CCIR 468-2 weighted; quasi peak; $V_o = 2.0 \text{ V}$ $G_v = 0 \text{ dB}$ $G_v = 12 \text{ dB}$ $G_v = 20 \text{ dB}$	– – – –	105 95 88 81	– – – –	dB dB dB dB

Sound fader control circuit

TEA6320

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$P_{no(RMS)}$	noise output power (RMS value) only contribution of TEA6320; power amplifier for 6 W	mute position; note 1	–	–	10	nW
α_B	crosstalk ($20 \log V_{bus(p-p)} / V_o(RMS)$) between bus inputs and signal outputs	note 2	–	110	–	dB
Source selector						
Z_i	input impedance		25	35	45	k Ω
α_S	input isolation of one selected source to any other input	f = 1 kHz f = 12.5 kHz	–	105 95	–	dB dB
$V_i(RMS)$	maximum input voltage (RMS value)	THD < 0.5%; $V_{CC} \approx 8.5$ V THD < 0.5%; $V_{CC} \approx 7.5$ V	–	2.15 1.8	–	V V
$V_{DC OFF}$	DC offset voltage at source selector out by selection of any inputs		–	–	10	mV
Z_o	output impedance		–	80	120	Ω
R_L	output load resistance		10	–	–	k Ω
C_L	output load capacity		0	–	2500	pF
G_v	voltage gain, source selector		–	0	–	dB
Control part (source selector disconnected; source resistance 600 Ω)						
Z_i	input impedance volume input input impedance loudness input		100 25	150 33	200 40	k Ω k Ω
Z_o	output impedance		–	80	120	Ω
R_L	output load resistance		2	–	–	k Ω
C_L	output load capacity		0	–	10	nF
$V_i(RMS)$	maximum input voltage (RMS value)	THD < 0.5%	–	2.15	–	V
V_{no}	noise output voltage	CCIR 468-2 weighted; quasi peak $G_v = 20$ dB $G_v = 0$ dB $G_v = -66$ dB mute position	– – – –	110 33 13 10	220 50 22 –	μ V μ V μ V μ V
G_c	total continuous control range recommended control range		– –	106 86	– –	dB dB
G_{step}	step resolution step error between any adjoining step		– –	1 –	– 0.5	dB dB
ΔG_a	attenuator set error	$G_v = +20$ to -50 dB $G_v = -51$ to -66 dB	– –	– –	2 3	dB dB
ΔG_t	gain tracking error	$G_v = +20$ to -50 dB	–	–	2	dB
α_m	mute attenuation	see Fig.8	100	110	–	dB
$V_{DC OFF}$	DC step offset between any adjoining step between any step to mute	$G_v = 0$ to -66 dB $G_v = 20$ to 0 dB $G_v = 0$ to -66 dB	– – –	0.2 tbn –	10 15 10	mV mV mV

Sound fader control circuit

TEA6320

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Volume I control and loudness						
G_c	continuous volume control range		–	51	–	dB
G_v	volume gain		–31	–	20	dB
G_{step}	step resolution		–	1	–	dB
L_B	maximum loudness boost	loudness on; referred to loudness off; boost is determined by external components $f = 40$ Hz $f = 10$ kHz	– –	17 4.5	– –	dB dB
Bass control						
G_b	bass control, maximum boost	$f = 40$ Hz	14	15	16	dB
	maximum attenuation	$f = 40$ Hz	14	15	16	dB
G_{step}	step resolution (toggle switching)	$f = 40$ Hz	–	1.5	–	dB
	step error between any adjoining step	$f = 40$ Hz	–	–	0.5	dB
$V_{DC\ OFF}$	DC step offset in any bass position		–	–	20	mV
Treble control						
G_t	treble control, maximum boost	$f = 15$ kHz	11	12	13	dB
	maximum attenuation	$f = 15$ kHz	11	12	13	dB
	maximum boost	$f > 15$ kHz	–	–	15	dB
G_{step}	step resolution (toggle switching)	$f = 15$ kHz	–	1.5	–	dB
	step error between any adjoining step	$f = 15$ kHz	–	–	0.5	dB
$V_{DC\ OFF}$	DC step offset in any treble position		–	–	10	mV
Volume II, balance and fader control						
G_f	continuous attenuation fader and volume control range		53.5	55	56.5	dB
G_{step}	step resolution		–	1	2	dB
	attenuation set error		–	–	1.5	dB
Mute function (see Fig.9)						
a) Hardware mute						
V_{sw}	mute switch level ($2 \times V_{BE}$)		–	1.45	–	V
mute active:						
$V_{sw\ LOW}$	input level		–	–	1.0	V
I_{ch}	input current	$V_{sw\ LOW} = 1$ V	–300	–	–	μ A
mute passive: level internally defined						
$V_{sw\ HIGH}$	saturation voltage		–	–	V_{CC}	V
t_{DMU}	delay until mute passive		–	–	0.5	ms
b) Zero crossing mute						
I_D	discharge current		0.3	0.6	1.2	μ A
I_{CH}	charge current		–300	–150	–	μ A
V_{SWDEL}	delay switch level ($3 \times V_{BE}$)		–	2.2	–	V
t_{DEV}	delay time	$C_m = 10$ nF	–	100	–	ms
V_{WIND}	window for audio signal zero crossing detection		–	30	40	mV

Sound fader control circuit

TEA6320

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Muting at power supply drop						
V _{CC-DROP}	supply drop for mute active		–	V ₁₉ – 0.7	–	V
Power on reset (when reset is active the GMU-bit (general mute) is set and the I²C-bus receiver is in reset position)						
V _{CC}	increasing supply voltage start of reset		–	–	2.5	V
	end of reset		5.2	6.0	6.8	V
	decreasing supply voltage start of reset		4.2	5.0	5.8	V
Digital part						
I ² C-bus pins; see note 3						
V _{IH}	HIGH level input voltage		3	–	9.5	V
V _{IL}	LOW level input voltage		–0.3	–	+1.5	V
I _{IH}	HIGH level input current		–10	–	+10	μA
I _{IL}	LOW level input current		–10	–	+10	μA
V _{OL}	LOW level output voltage	I _L = 3 mA	–	–	0.4	V

Notes to the characteristics

- The indicated values for output power assume a 6 W power amplifier at 4 Ω with 20 dB gain and a fixed attenuator of 12 dB in front of it. Signal-to-noise ratios exclude noise contribution of the power amplifier.
- The transmission contains: total initialization with MAD and Subaddress for volume and 8 data words, see also definition of characteristics, clock frequency = 50 kHz, repetition burst rate = 400 Hz, maximum bus signal amplitude = 5 V_{p-p}
- The AC characteristics are in accordance with the I²C-bus specification. Full specification of I²C-bus will be supplied on request.

I²C-BUS PROTOCOL**I²C-bus format**

S	SLAVE ADDRESS	A	SUBADDRESS	A	DATA	A	P
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Where:

S	= start condition
SLAVE ADDRESS (MAD)	= 1000 0000
A	= acknowledge, generated by the slave
SUBADDRESS (SAD)	= see Table 1
DATA	= see Table 1
P	= STOP condition

If more than 1 byte of DATA is transmitted, then auto-increment of the significant subaddress is performed.

Sound fader control circuit

TEA6320

Subaddress

Table 1 Second byte after MAD

FUNCTION	BIT	MSB								LSB
		7	6	5	4	3	2	1	0	
volume/loudness	V	0	0	0	0	0	0	0	0	0
fader front right	FFR	0	0	0	0	0	0	0	0	1
fader front left	FFL	0	0	0	0	0	0	0	1	0
fader rear right	FRR	0	0	0	0	0	0	0	1	1
fader rear left	FRL	0	0	0	0	0	0	1	0	0
bass	BA	0	0	0	0	0	0	1	0	1
treble	TR	0	0	0	0	0	0	1	1	0
switch	S	0	0	0	0	0	0	1	1	1
									significant subaddress	

Definition of third byte

Table 2 Third byte after MAD and SAD

FUNCTION	BIT	MSB								LSB
		7	6	5	4	3	2	1	0	
volume/loudness	V	ZCM	LOFF	V5	V4	V3	V2	V1	V0	
fader front right	FFR	X	X	FFR5	FFR4	FFR3	FFR2	FFR1	FFR0	
fader front left	FFL	X	X	FFL5	FFL4	FFL3	FFL2	FFL1	FFL0	
fader rear right	FRR	X	X	FRR5	FRR4	FRR3	FRR2	FRR1	FRR0	
fader rear left	FRL	X	X	FRL5	FRL4	FRL3	FRL2	FRL1	FRL0	
bass	BA	X	X	X	BA4	BA3	BA2	BA1	BA0	
treble	TR	X	X	X	TR4	TR3	TR2	TR1	TR0	
switch	S	GMU	X	X	X	X	SC2	SC1	SC0	

Function of the bits:

V0 to V5	volume control
LOFF	switch loudness on/off
FRR0 to FRR5	fader control front right
FFL0 to FFL5	fader control front left
FRR0 to FRR5	fader control rear right
FRL0 to FRL5	fader control rear left
BA0 to BA4	bass control
TR0 to TR4	treble control
SC0 to SC2	source selector control
GMU	mute control for all outputs (general mute)
ZCM	zero crossing mode
X	don't care bits (logic 1 during testing)

Sound fader control circuit

TEA6320

Table 3 Volume setting

G _v (dB)	DATA					
	V5	V4	V3	V2	V1	V0
20	1	1	1	1	1	1
19	1	1	1	1	1	0
18	1	1	1	1	0	1
17	1	1	1	1	0	0
16	1	1	1	0	1	1
15	1	1	1	0	1	0
14	1	1	1	0	0	1
13	1	1	1	0	0	0
12	1	1	0	1	1	1
11	1	1	0	1	1	0
10	1	1	0	1	0	1
9	1	1	0	1	0	0
8	1	1	0	0	1	1
7	1	1	0	0	1	0
6	1	1	0	0	0	1
5	1	1	0	0	0	0
4	1	0	1	1	1	1
3	1	0	1	1	1	0
2	1	0	1	1	0	1
1	1	0	1	1	0	0
0	1	0	1	0	1	1
-1	1	0	1	0	1	0
-2	1	0	1	0	0	1
-3	1	0	1	0	0	0
-4	1	0	0	1	1	1
-5	1	0	0	1	1	0
-6	1	0	0	1	0	1
-7	1	0	0	1	0	0
-8	1	0	0	0	1	1
-9	1	0	0	0	1	0
-10	1	0	0	0	0	1
-11	1	0	0	0	0	0

Loudness on: the increment of the loudness characteristic is linear at every volume step in the range from +20 dB to -11 dB.

Sound fader control circuit

TEA6320

Table 3 Volume setting (continued)

G _v (dB)	DATA					
	V5	V4	V3	V2	V1	V0
-12	0	1	1	1	1	1
-13	0	1	1	1	1	0
-14	0	1	1	1	0	1
-15	0	1	1	1	0	0
-16	0	1	1	0	1	1
-17	0	1	1	0	1	0
-18	0	1	1	0	0	1
-19	0	1	1	0	0	0
-20	0	1	0	1	1	1
-21	0	1	0	1	1	0
-22	0	1	0	1	0	1
-23	0	1	0	1	0	0
-24	0	1	0	0	1	1
-25	0	1	0	0	1	0
-26	0	1	0	0	0	1
-27	0	1	0	0	0	0
-28	0	0	1	1	1	1
-29	0	0	1	1	1	0
-30	0	0	1	1	0	1
-31	0	0	1	1	0	0

Loudness characteristic is constant in a range from -11 dB to -31 dB.

Table 3 Volume setting (continued)

G _v (dB)	DATA					
	V5	V4	V3	V2	V1	V0
-28	0	0	1	0	1	1
.
-31	0	0	0	0	0	0

Repetition of steps in a range from -28 dB to -31 dB.

Sound fader control circuit

TEA6320

Table 4 Fader setting

G _v (dB)	DATA					
	FRR5	FRR4	FRR3	FRR2	FRR1	FRR0
	FRL5	FRL4	FRL3	FRL2	FRL1	FRL0
	FFL5	FFL4	FFL3	FFL2	FFL1	FFL0
	FFR5	FFR4	FFR3	FFR2	FFR1	FFR0
0	1	1	1	1	1	1
-1	1	1	1	1	1	0
-2	1	1	1	1	0	1
-3	1	1	1	1	0	0
-4	1	1	1	0	1	1
-5	1	1	1	0	1	0
-6	1	1	1	0	0	1
-7	1	1	1	0	0	0
-8	1	1	0	1	1	1
-9	1	1	0	1	1	0
-10	1	1	0	1	0	1
-11	1	1	0	1	0	0
-12	1	1	0	0	1	1
-13	1	1	0	0	1	0
-14	1	1	0	0	0	1
-15	1	1	0	0	0	0
-16	1	0	1	1	1	1
-17	1	0	1	1	1	0
-18	1	0	1	1	0	1
-19	1	0	1	1	0	0
-20	1	0	1	0	1	1
-21	1	0	1	0	1	0
-22	1	0	1	0	0	1
-23	1	0	1	0	0	0
-24	1	0	0	1	1	1
-25	1	0	0	1	1	0
-26	1	0	0	1	0	1
-27	1	0	0	1	0	0
-28	1	0	0	0	1	1
-29	1	0	0	0	1	0
-30	1	0	0	0	0	1
-31	1	0	0	0	0	0
-32	0	1	1	1	1	1
-33	0	1	1	1	1	0
-34	0	1	1	1	0	1
-35	0	1	1	1	0	0
-36	0	1	1	0	1	1
-37	0	1	1	0	1	0
-38	0	1	1	0	0	1

Sound fader control circuit

TEA6320

G _v (dB)	DATA					
	FRR5	FRR4	FRR3	FRR2	FRR1	FRR0
	FRL5	FRL4	FRL3	FRL2	FRL1	FRL0
	FFL5	FFL4	FFL3	FFL2	FFL1	FFL0
	FFR5	FFR4	FFR3	FFR2	FFR1	FFR0
-39	0	1	1	0	0	0
-40	0	1	0	1	1	1
-41	0	1	0	1	1	0
-42	0	1	0	1	0	1
-43	0	1	0	1	0	0
-44	0	1	0	0	1	0
-45	0	1	0	0	1	0
-46	0	1	0	0	0	1
-47	0	1	0	0	0	0
-48	0	0	1	1	1	1
-49	0	0	1	1	1	0
-50	0	0	1	1	0	1
-51	0	0	1	1	0	0
-52	0	0	1	0	1	1
-53	0	0	1	0	1	0
-54	0	0	1	0	0	1
-55	0	0	1	0	0	0
mute	0	0	0	1	1	1
mute	0	0	0	1	1	0
mute	0	0	0	1	0	1
mute	0	0	0	1	0	0
mute	0	0	0	0	1	1
mute	0	0	0	0	1	0
mute	0	0	0	0	0	1
mute	0	0	0	0	0	0

For a particular range the data is always the same, only the subaddress changes.

Sound fader control circuit

TEA6320

Table 5 Bass setting

G _v (dB)	DATA				
	BA4	BA3	BA2	BA1	BA0
15	1	1	1	1	1
13.5	1	1	1	1	0
15	1	1	1	0	1
13.5	1	1	1	0	0
15	1	1	0	1	1
13.5	1	1	0	1	0
12	1	1	0	0	1
10.5	1	1	0	0	0
9	1	0	1	1	1
7.5	1	0	1	1	0
6	1	0	1	0	1
4.5	1	0	1	0	0
3	1	0	0	1	1
1.5	1	0	0	1	0
0*	1	0	0	0	1
0**	1	0	0	0	0
-1.5	0	1	1	1	1
-3	0	1	1	1	0
-4.5	0	1	1	0	1
-6	0	1	1	0	0
-7.5	0	1	0	1	1
-9	0	1	0	1	0
-10.5	0	1	0	0	1
-12	0	1	0	0	0
-13.5	0	0	1	1	1
-15	0	0	1	1	0
-13.5	0	0	1	0	1
-15	0	0	1	0	0
***	0	0	0	1	1
***	0	0	0	1	0
***	0	0	0	0	1
*** ****	0	0	0	0	0

* Recommended data word for step 0 dB.

** Result of 1.5 dB boost and 1.5 dB attenuation.

*** The last four bass control data words mute the bass response.

**** The last bass control and treble control data words (00000) enable the external equalizer connection.

Sound fader control circuit

TEA6320

Table 6 Treble setting

G _v (dB)	DATA				
	TR4	TR3	TR2	TR1	TR0
12	1	1	1	1	1
10.5	1	1	1	1	0
12	1	1	1	0	1
10.5	1	1	1	0	0
12	1	1	0	1	1
10.5	1	1	0	1	0
12	1	1	0	0	1
10.5	1	1	0	0	0
9	1	0	1	1	1
7.5	1	0	1	1	0
6	1	0	1	0	1
4.5	1	0	1	0	0
3	1	0	0	1	1
1.5	1	0	0	1	0
0*	1	0	0	0	1
0**	1	0	0	0	0
-1.5	0	1	1	1	1
-3	0	1	1	1	0
-4.5	0	1	1	0	1
-6	0	1	1	0	0
-7.5	0	1	0	1	1
-9	0	1	0	1	0
-10.5	0	1	0	0	1
-12	0	1	0	0	0
***	0	0	1	1	1
***	0	0	1	1	0
***	0	0	1	0	1
***	0	0	1	0	0
***	0	0	0	1	1
***	0	0	0	1	0
***	0	0	0	0	1
*** ****	0	0	0	0	0

* Recommended data word for step 0 dB.

** Result of 1.5 dB boost and 1.5 dB attenuation.

*** The last eight treble control data words select treble cut.

**** The last treble control and bass control data words (00000) enable the external equalizer connection.

Sound fader control circuit

TEA6320

Table 7 Loudness setting

CHARACTERISTIC	DATA L OFF
with loudness	0
linear	1

Table 8 Selected inputs

INPUTS	DATA		
	SC2	SC1	SC0
IAL, IAR stereo	1	1	1
IBL, IBR stereo	1	1	0
ICC, ICR stereo	1	0	1
IDL, IDR stereo	1	0	0
IMO, mono	0	X	X

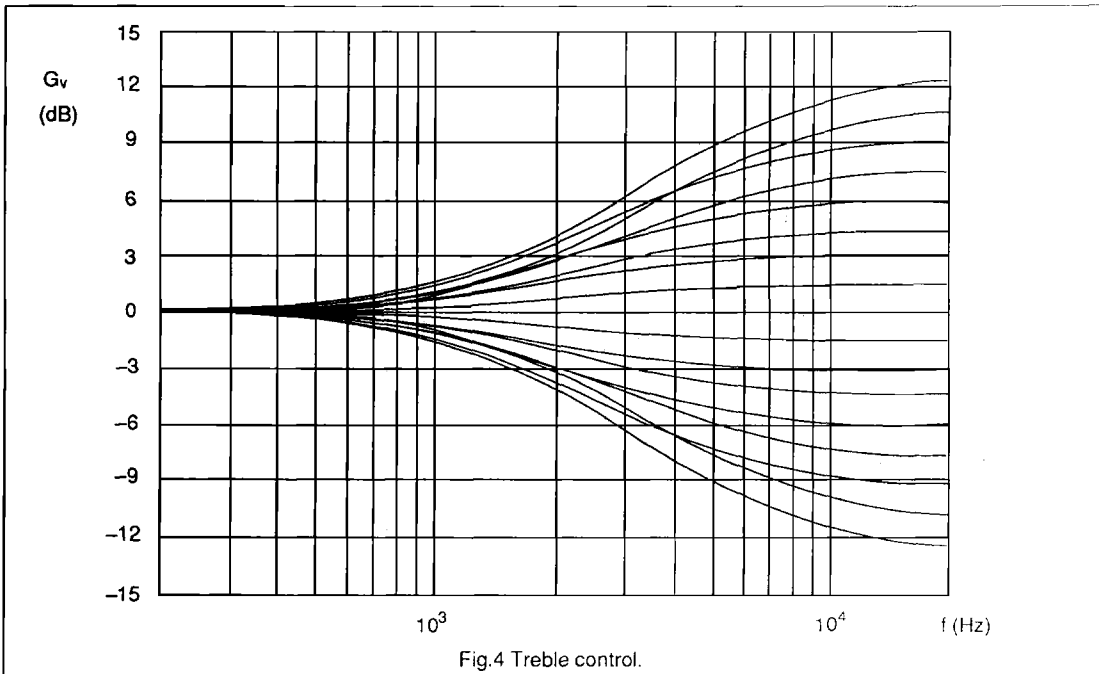
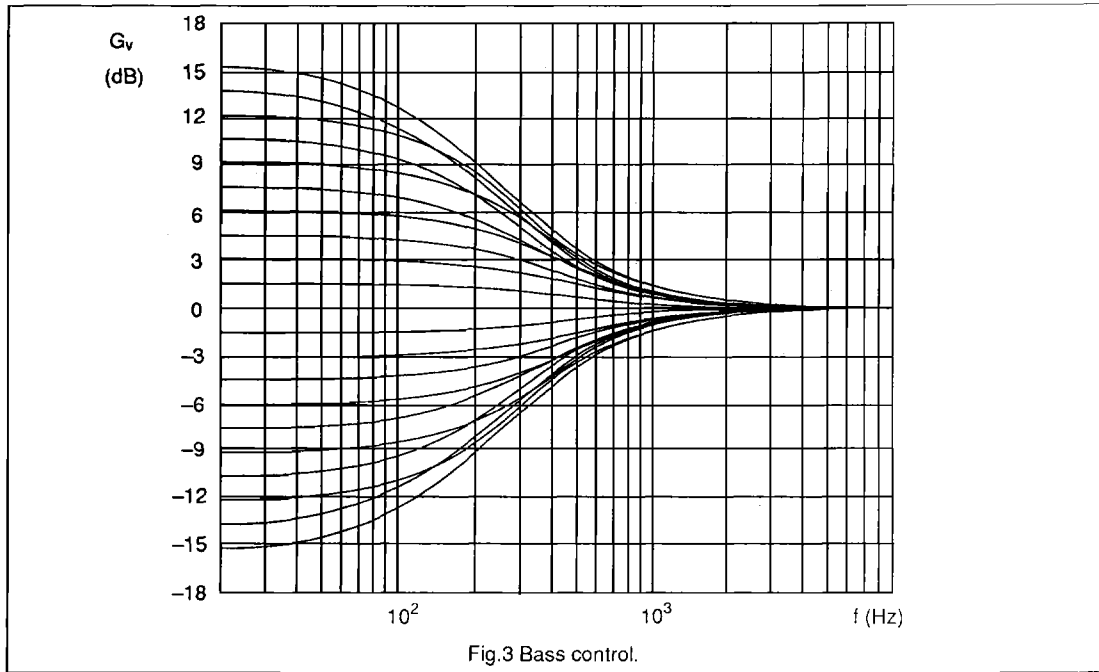
Table 9 Mute mode

GMU	ZCM	mode
0	0	direct mute off
0	1	mute off delayed until the next zero crossing
1	0	direct mute
1	1	mute delayed until the next zero crossing

X = don't care bits (logic 1 during testing)

Sound fader control circuit

TEA6320



Sound fader control circuit

TEA6320

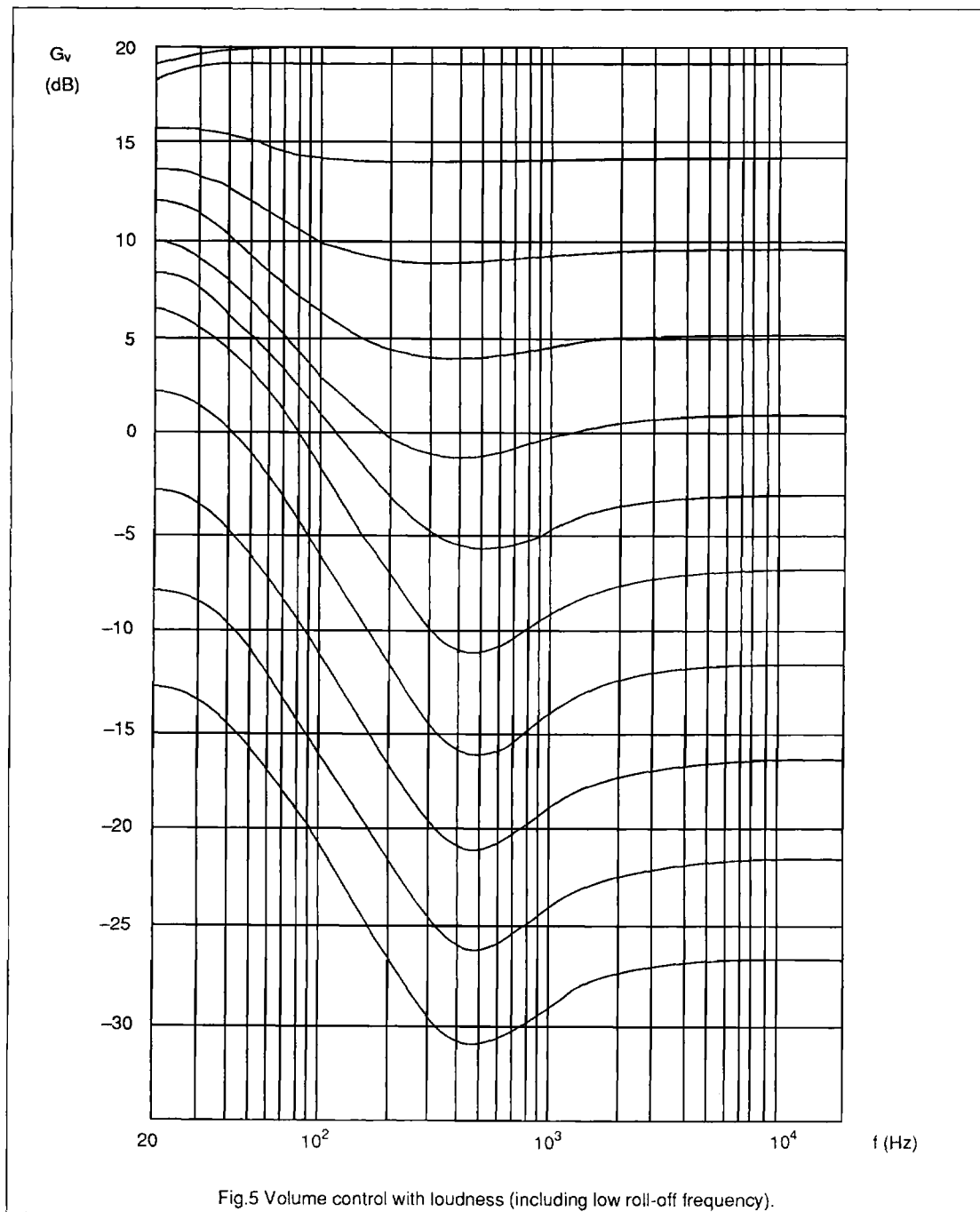
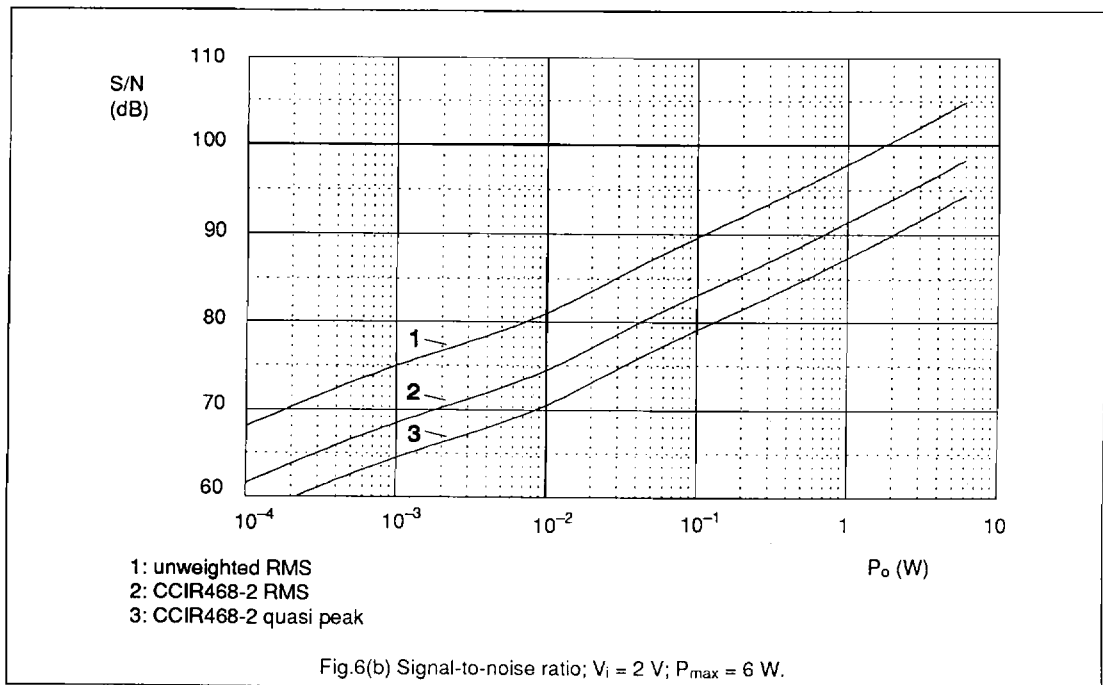
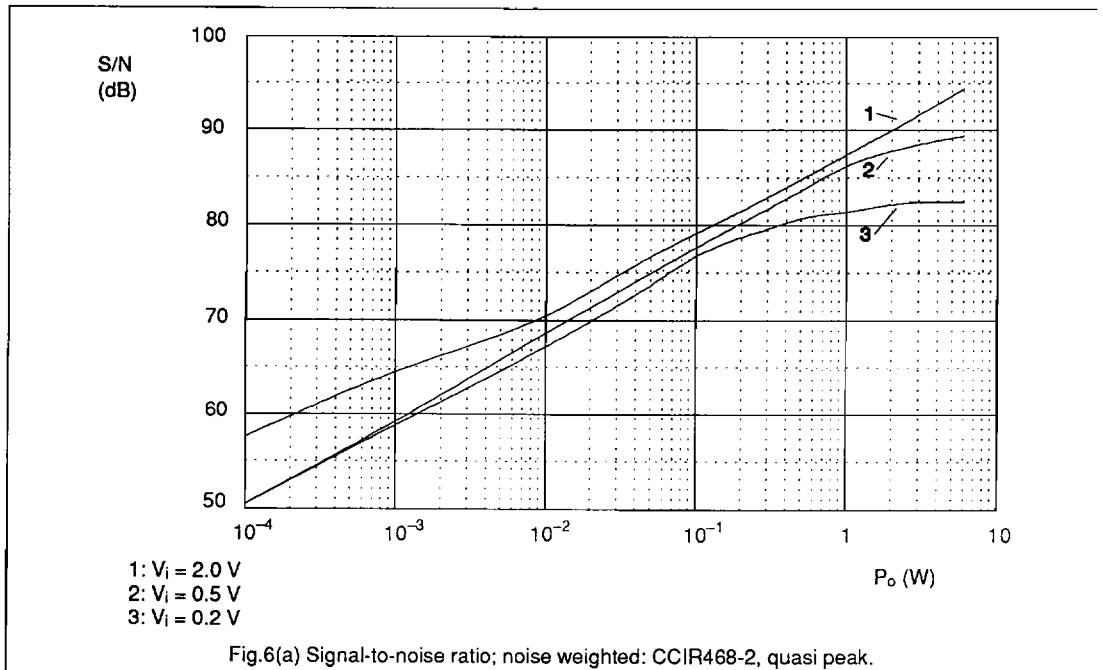


Fig.5 Volume control with loudness (including low roll-off frequency).

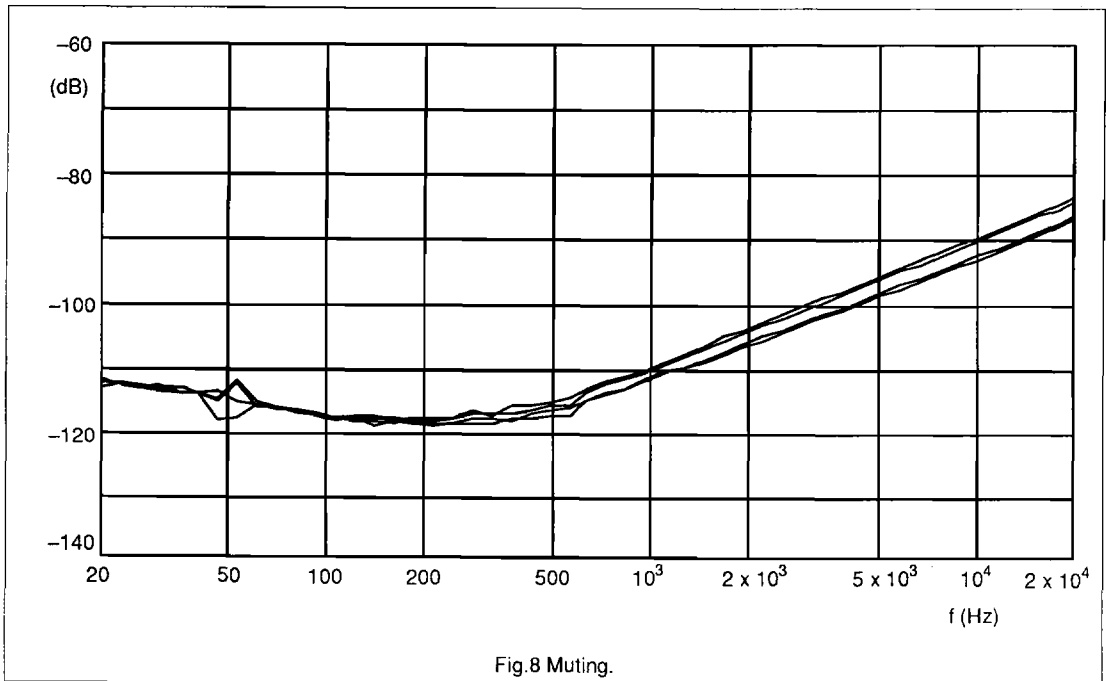
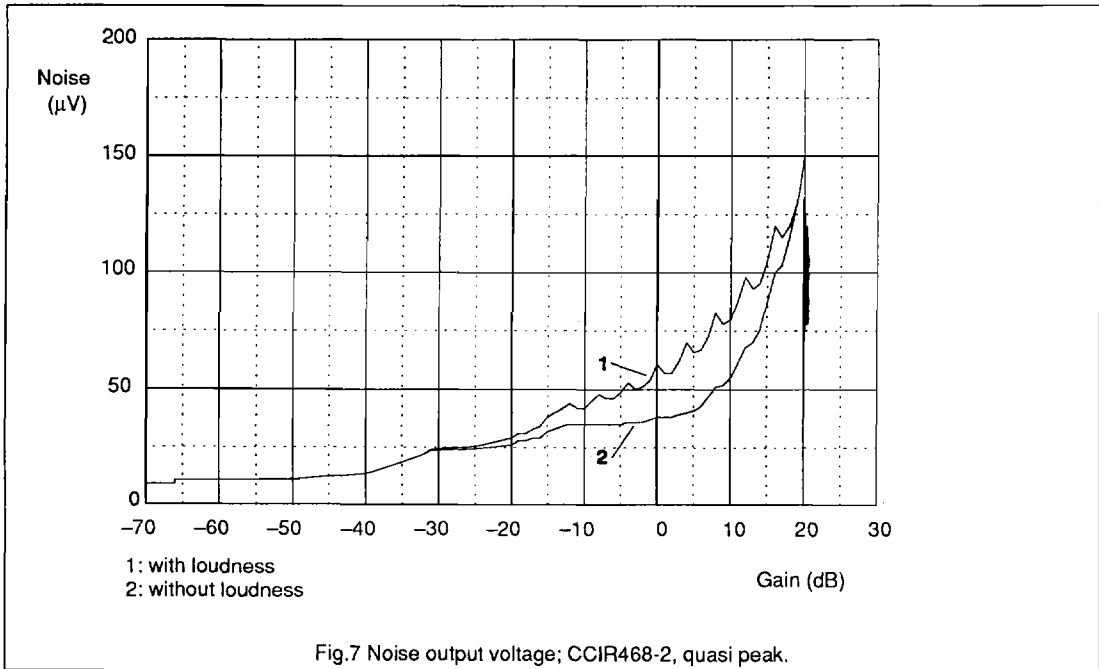
Sound fader control circuit

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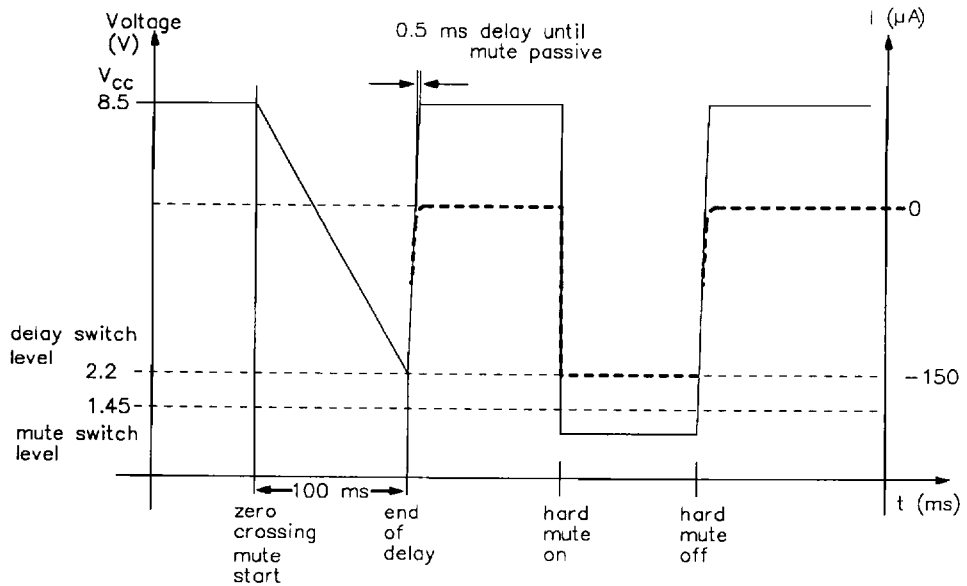
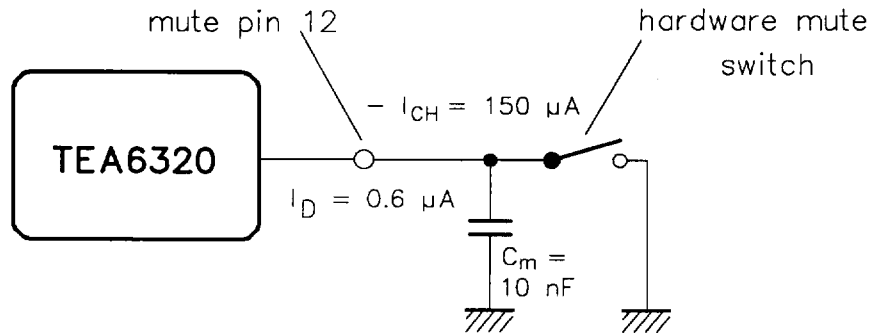
Sound fader control circuit

TEA6320



Sound fader control circuit

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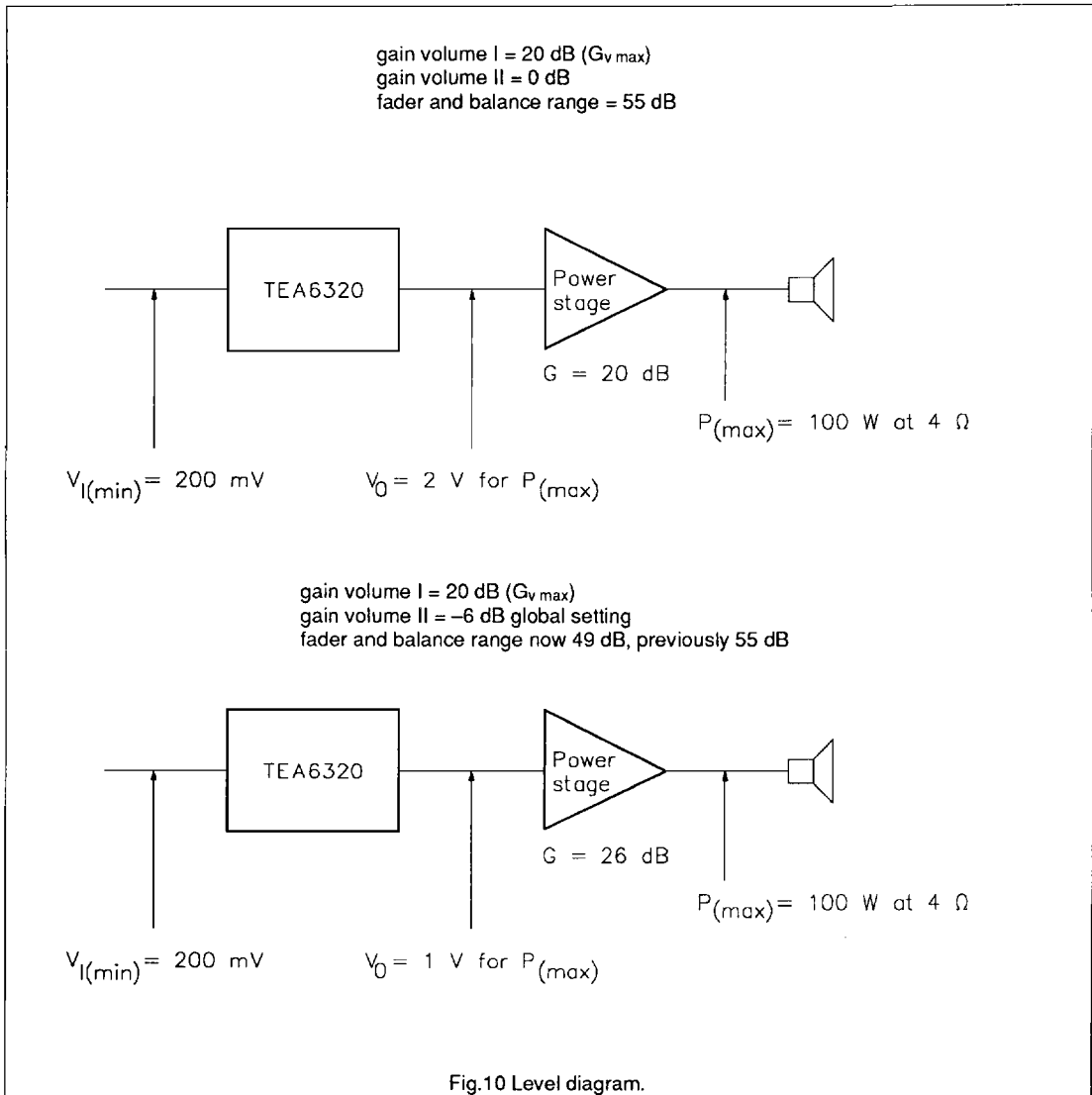
delay switch level voltage is typically 2.2 V and is referenced to $3 \times V_{BE}$

Fig.9 Mute function diagram.

Sound fader control circuit

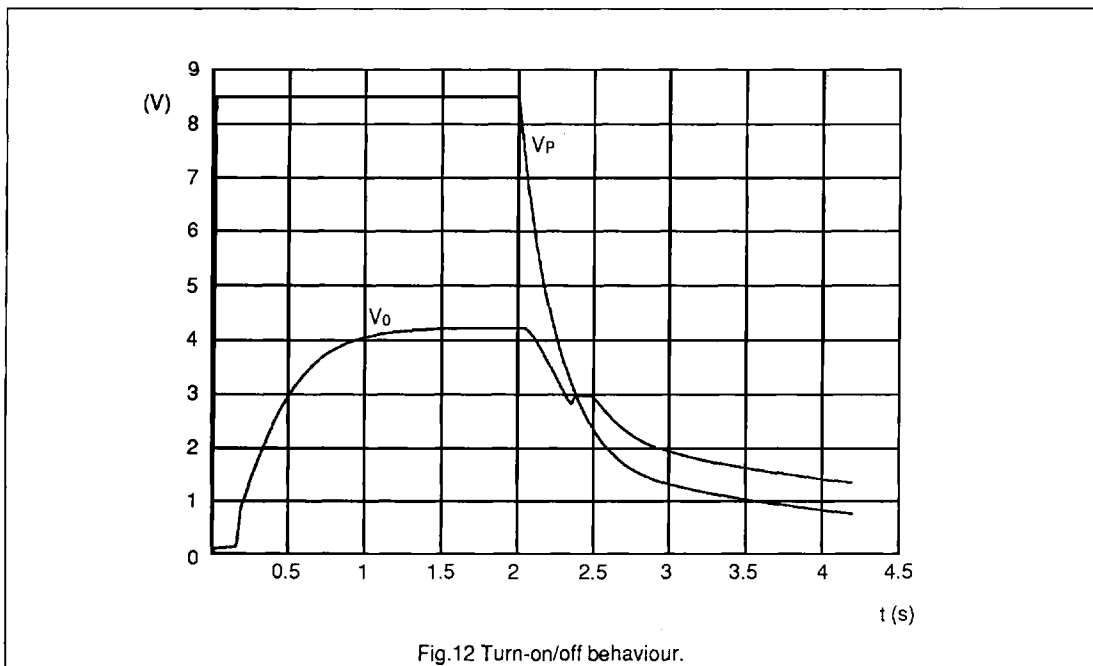
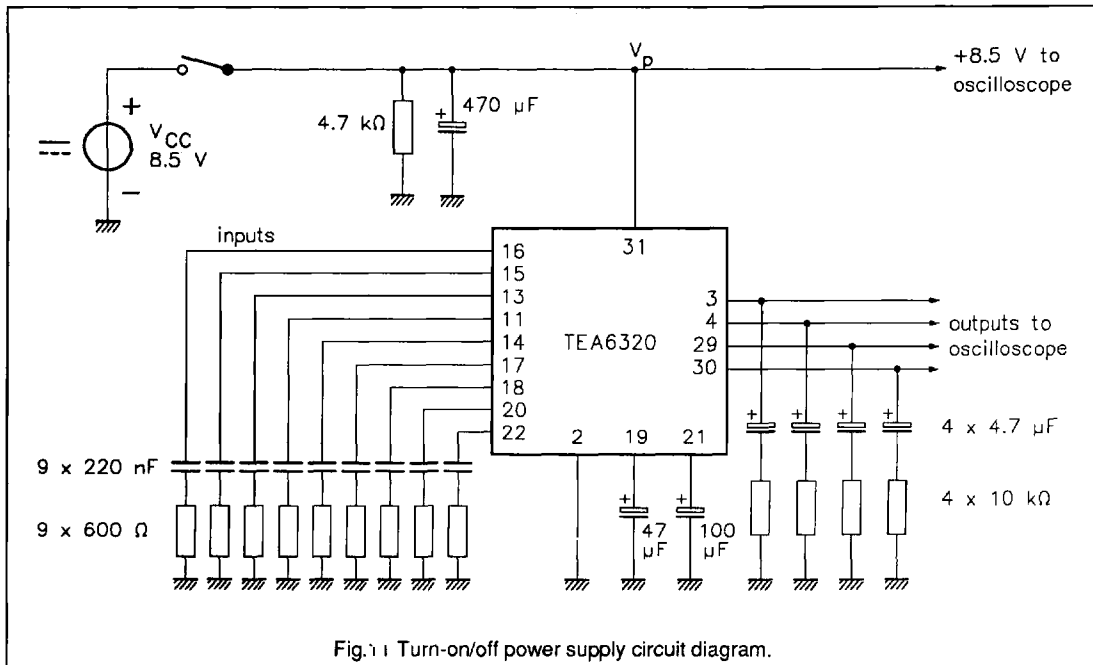
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If the 20 dB gain is not required for the maximum volume position, it will be an advantage to use the maximum boost gain and then increased attenuation in the last section, Volume II. Therefore the loudness will be at the correct place and a lower noise and offset voltage will be achieved.



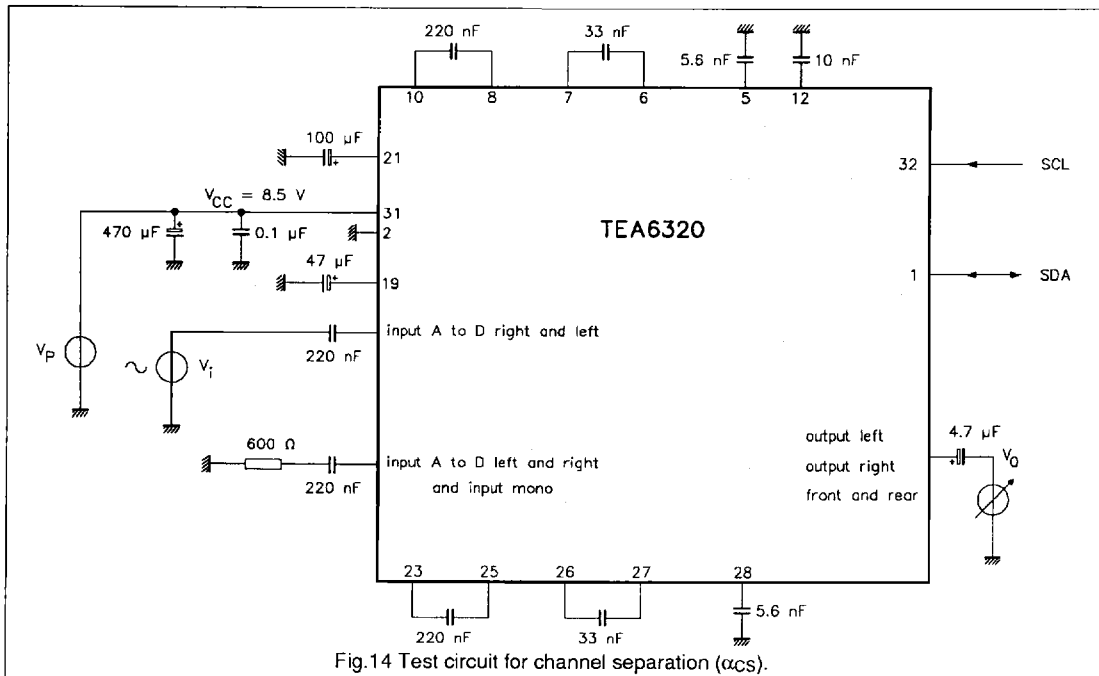
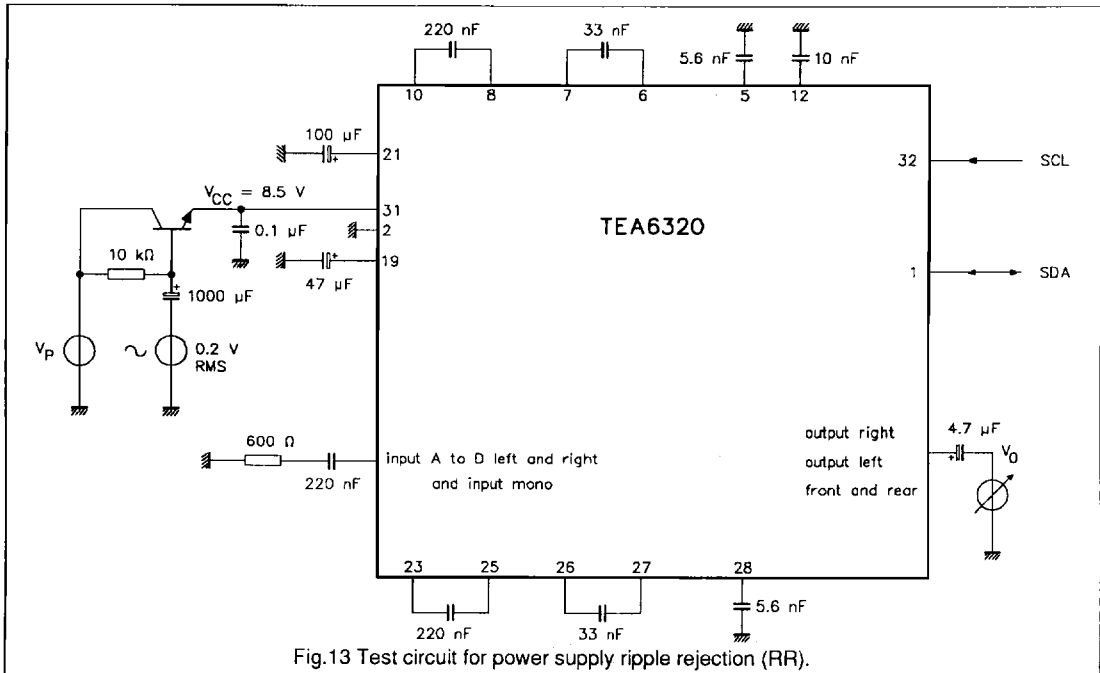
Sound fader control circuit

TEA6320



Sound fader control circuit

TEA6320



Sound fader control circuit

TEA6320

Selection of input signals by using the zero crossing mute mode

A selection from input A (IAL) to input B (IBL) left sources produces a modulation click depending on the difference of the signal values at the time of switching.

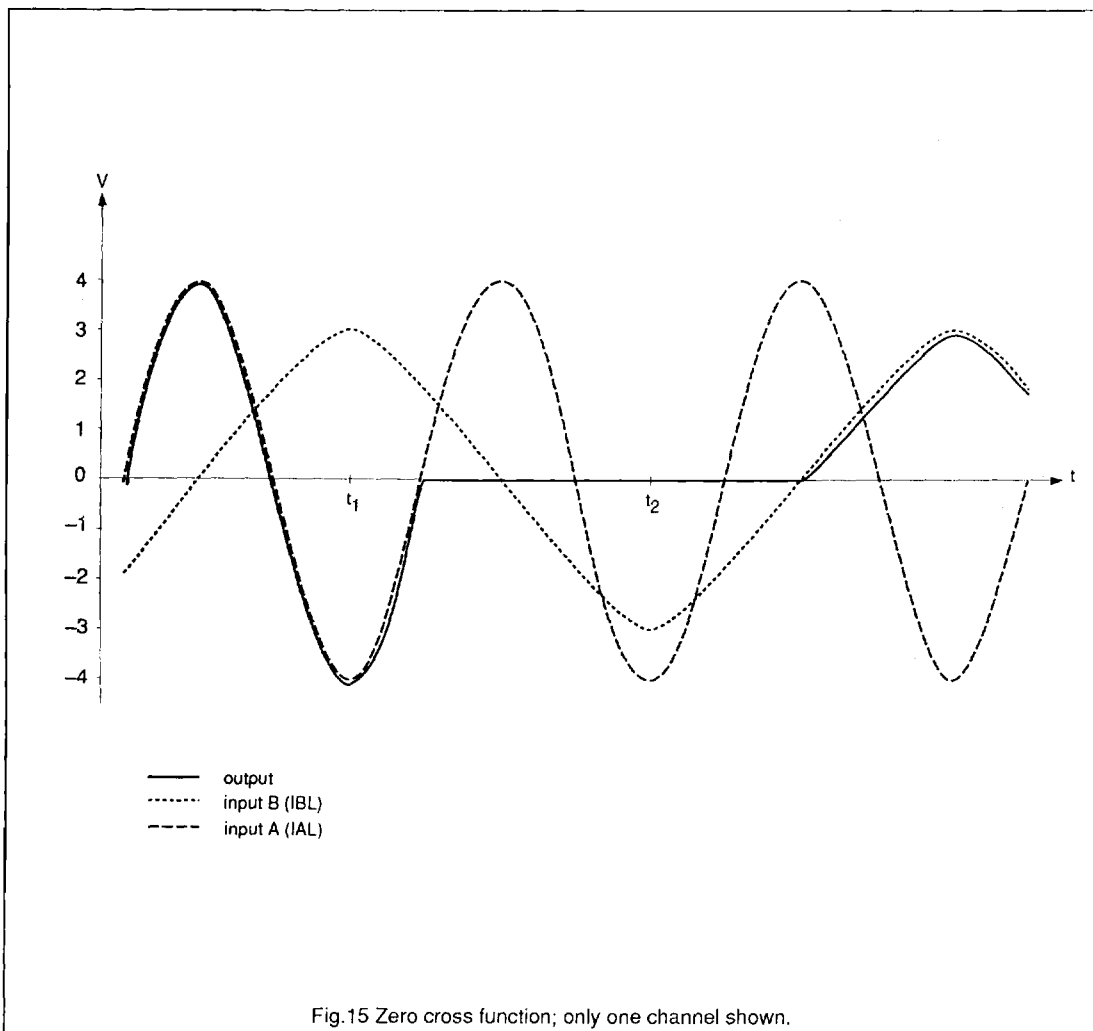
At t_1 the maximum possible difference between signals is $7 V_{(p-p)}$ and gives a large click. Using the zero cross detector no modulation click is audible.

For example: The selection is enabled at t_1 , the microcontroller sets the zero cross bit ($ZCM = 1$) and then the mute bit ($GMU = 1$) via the I^2C -bus. The output signal follows the input A signal, until the next zero crossing occurs and then activates mute.

After a fixed delay time at t_2 , the microcontroller sends the bits for input switching and mute inactive.

The output signal remains muted until the next signal zero crossing of input B (IBL) occurs, and then follows that signal.

The delay time $t_2 - t_1$ is e. g. 40 ms. Therefore is the capacity $CM = 3.3 \text{ nF}$. The zero cross function is working at the lowest frequency of 40 Hz determined by the CM capacitor.



Sound fader control circuit

TEA6320

Loudness filter calculation example

Fig.16 shows the basic loudness circuit with an external low pass filter application. R_1 allows an attenuation range of 21 dB while the boost is determined by the gain stage V_2 . Both result in a loudness control range of +20 dB to -12 dB.

Defining $f_{reference}$ as the frequency where the level does not change while switching loudness on/off. The external resistor R_3 for $f_{reference} \rightarrow \infty$ can be calculated as

$$R_3 = R_1 \frac{10^{G_v/20}}{1 - 10^{G_v/20}}$$

with $G_v = -21$ dB and $R_1 = 33$ k Ω
 $R_3 = 3.2$ k Ω is generated.

For the low pass filter characteristic the value of the external capacitor C_1 can be determined by setting a specific boost for a defined frequency and referring the gain to G_v at $f_{reference}$ as indicated above.

$$\left| \frac{1}{j\omega C_1} \right| = \frac{(R_1 + R_3) \times 10^{G_v/20} - R_3}{1 - 10^{G_v/20}}$$

For example: 3 dB boost at $f = 1$ kHz
 $G_v = G_{v reference} + 3$ dB = -18 dB;
 $f = 1$ kHz and $C_1 = 100$ nF

If a loudness characteristic with additional high frequency boost is desired, an additional high pass section has to be included in the external filter circuit as indicated in the block diagram. A filter configuration that provides AC coupling avoids offset voltage problems.

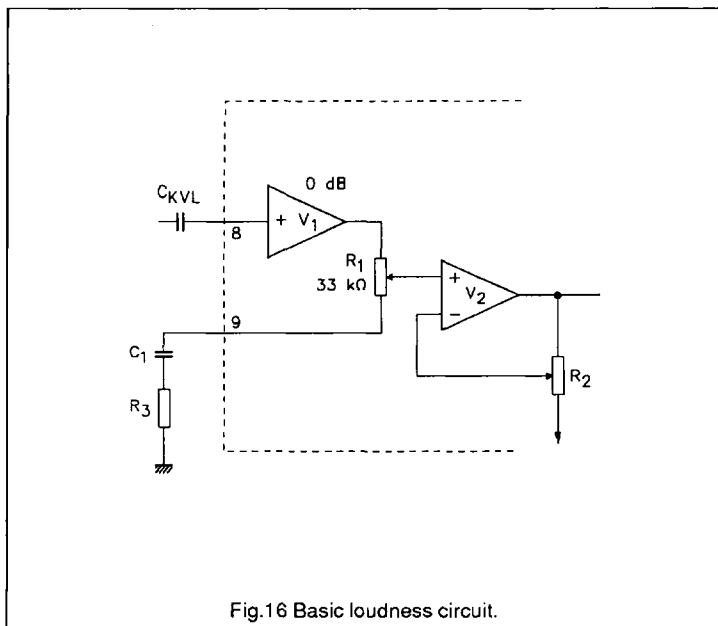
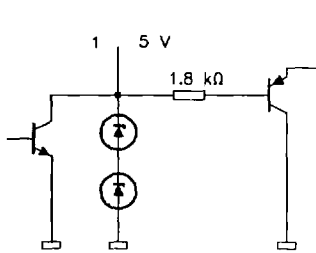


Fig.16 Basic loudness circuit.

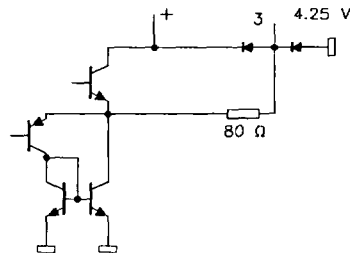
Sound fader control circuit

TEA6320

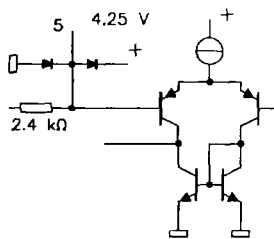
INTERNAL PIN CONFIGURATIONS



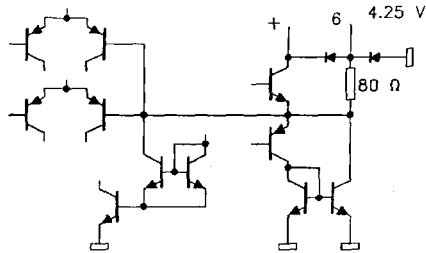
Pin 1: SDA (I²C-bus data)



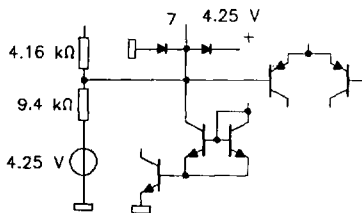
Pin 3: Output left, rear
Pin 4: Output left, front
Pin 29: Output right, front
Pin 30: Output right, rear



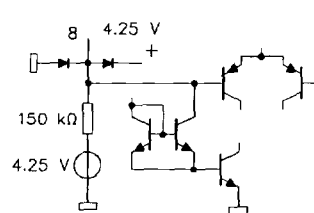
Pin 5: Treble control capacitor, left channel
Pin 28: Treble control capacitor, right channel



Pin 6: Bass control capacitor output, left channel
Pin 27: Bass control capacitor output, right channel



Pin 7: Bass control capacitor input, left channel
Pin 27: Bass control capacitor input, right channel



Pin 8: Input volume 1 left, control part
Pin 25: Input volume 1 right, control part

Pin equivalent circuits

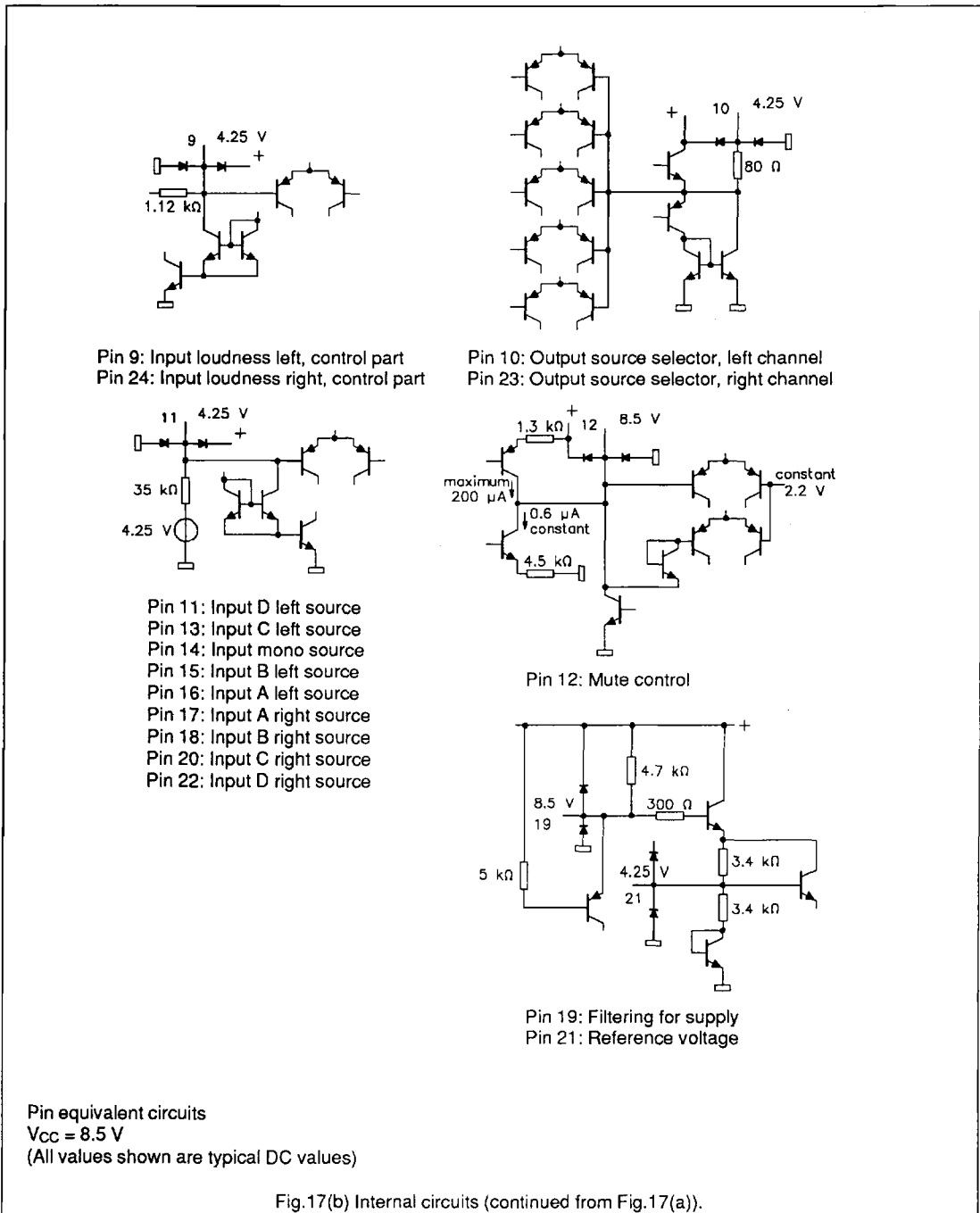
V_{CC} = 8.5 V

(All values shown are typical DC values)

Fig.17(a) Internal circuits (continued in Fig.17(b)).

Sound fader control circuit

TEA6320



Sound fader control circuit

TEA6320

