AMI

A Subsidiary of Gould Inc.

S2743/S2742

ENCODER/DECODER REMOTE CONTROL 2-CHIP SET

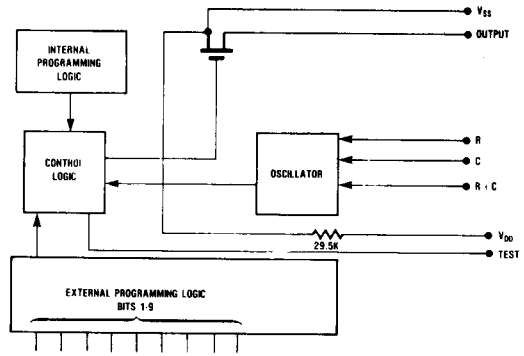
Features

- ☐ RC Oscillator Used—No Crystal Required
- ☐ Phase Locked Loop on Decoder for Reliable Operation
- ☐ 512 User Selectable Address Codes
- ☐ Encoder Operates on a Single Rail 9 Volt Supply — Suitable for Inexpensive and Convenient Battery Operation
- ☐ User can Determine the Type of Transmission Medium to Use

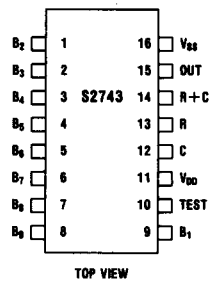
Applications

- ☐ Entry Access Systems
- ☐ Remote Engine Starting for Vehicles and Standby Generators
- ☐ Security Systems
- ☐ Traffic Control
- ☐ Paging Systems
- ☐ Remote Control of Domestic Appliances

Block Diagram 2743 Encoder

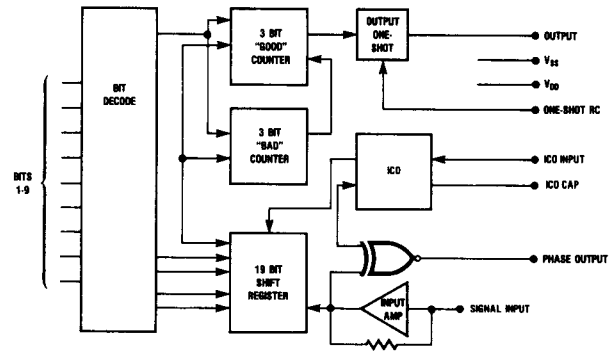


Pin Configuration 2743

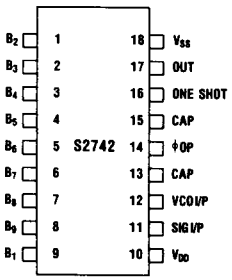


TOP VIEW

Block Diagram 2742 Decoder



Pin Configuration 2742



TOP VIEW

General Description—Encoder/Decoder

This two-chip PMOS set includes a user-programmable serial data encoder for use in a simple low-power transmitter and a serial data decoder for use in a user addressable receiver. The user can select the transmission medium (RF, infrared, or hardwire). The externally selectable message allows up to 512 codes or addresses; this is done with the nine binary inputs on each device. An additional 3 bits of address can be programmed on chip as a fixed preamble.

The serial data encoder encodes by means of a frequency-shift-keyed trinary data pattern composed of 16 data bits. Each data bit will have a length equivalent to 32 cycles of high frequency clock (20kHz typical). Each trinary data pattern will be 512 cycles of 1/2 the oscillator frequency length. The encoder frequency oscillator reference is controlled with an external RC network. The encoder transmitter can be powered by a single 9 volt battery so that a single momentary push button will activate the encoder and transmitter. In the off position there is no current flow.

The serial data decoder in conjunction with a receiver amplifier decodes the transmitted 16-bit coded signal. The on-chip phase-locked-loop locks in on the 20kHz signal even if the transmitted frequency differs from the receiver by up to ± 15%. The coded signal input is compared with the externally selected code. The serial decoder looks at the transmitted signal a minimum of three times before validating a good message. A 3-bit "good" code counter or a 3-bit "bad" code counter accumulates the number of successive good and bad codes being received.

The decoder has an on-chip one-shot which is user programmed by an external RC combination. Whenever three complete good codes are received in the "good" counter a signal enables the one-shot which controls the signal valid output. If a series of three sequential bad codes enter the "bad" code counter the "bad" counter resets the "good" code counter and one-shot period and will not allow an active output until the end of the one-shot period. Any "good" code resets the "bad" code counter. If the "good" counter has accumulated three good codes and activated the output one shot, any occasional "good" code (occurring within the one-shot period) will maintain the output by retriggering the one-shot. The output appears like a single switch, on when "good" codes are received, off when not, with the minimum total period being determined by twice the one-shot period. The one-shot can be used to prevent the output from switching on and off too rapidly due to system noise. The typical RC components shown in the block diagram give a period of about one second.

Functional Description—Serial Data Encoder

The AMI serial data encoder is comprised of three sections: Oscillator, Programming Logic, and Control Logic. Specifically it will provide logical ones "1", logical zeroes "0", and synchronization pulses "S" and arrange them into a trinary data pattern composed of 16 data bits. Each data bit will be 32 cycles of the high frequency (HF-1/2 Oscillator Frequency) in length. Each trinary data pattern will be 512 cycles of 1/2 the Oscillator Frequency length.

A logical "1" is represented by 32 cycles of the high frequency.

A logical "0" is represented by 16 cycles of the high frequency followed directly by 8 cycles of the low frequency (LF = 1/2 HF).

A synchronization pulse "S" is represented by 16 cycles of the low frequency.

A 16-bit data pattern will be encoded in the device in such a manner as to have three (3) bits programmed internally and nine (9) bits programmed externally.

The Oscillator Frequency equals twice that of the High Frequency, and the High Frequency equals twice that of the Low Frequency.

The Oscillator circuit will require a maximum of three (3) external components.

External programming inputs connected to the device $-V_{DD}$ supply will be considered as a logical "1". The bit programming current will not exceed 50μA. The programming resistance should not exceed 1kΩ. Unconnected external bit programming inputs will be considered at a logical "0".

A "1" ($-5V \leqslant$ "1" $\leqslant V_{DD}$) presented to the "Test" input sets the Internal counter and maintains the output of the device "On." The input impedance of the test input is greater than 5MΩ.

For portable operation a 9V transistor battery can be used for the DC voltage supply. Proper circuit polarity must be observed ($-V_{DD}$, $+V_{SS}$).

S2743 Absolute Maximum Ratings

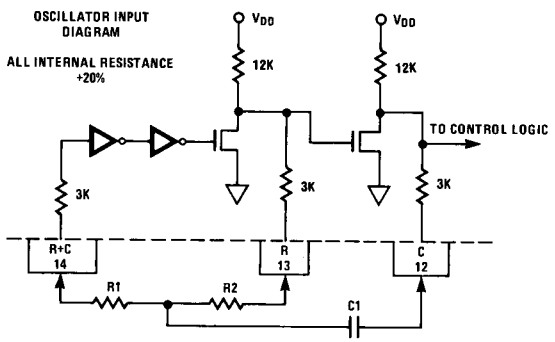
DC Supply Voltage ..... −15V
Input Voltage ..... V_{SS} + .3V to V_{SS} − 15V
Operating Temperature Range ..... −40°C to +100°C
Storage Temperature Range ..... −65°C to +150°C
Lead Temperature (During Soldering) ..... 300°C for Max. 10sec.

S2743 Electrical Characteristics (25°C Air Temperature Unless Otherwise Specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
	Operating Supply Voltage	−6.65	−9.5	−15	V	V_{DD}; V_{SS} = 0V
	Operating Power Dissipation		27	40	MW	−8V, −5mA, Max.
	Operating Frequency	2	40	60	kHz	Oscillator
	Programming Bits 1-9, Current			50	μA	Programming Input, R 1kΩ
	External Programming Resistance			1	kΩ	Bits 1-9
	(DC Bits 1-9) Program Logical "1"	V_{SS} − 5V		V_{DD}	V	
	Input Levels Logical "0"	V_{SS} − 1V		V_{SS}	V	
	Bits 1-9 Current		55		μA	Input R 9V>1.5M @ 5V
	Test and R + C Input Impedance	5		75	MΩ	
	(DC) Test Input Levels Test ON	V_{SS} − 5V		V_{DD}	V	Maintains Output Device ON
	Test OFF (See Note 1)	V_{SS} − 1V		V_{SS}	V	Permits Normal Operation
	R, C Resistance Logical "1"		12		kΩ	Resistance to V_{DD}, ± 20%
	R, C Resistance Logical "0" (See Figure 1)		3		kΩ	Resistance to V_{SS} + 20% − 30%
	Output Current (See Note 2)	5			mA	Output Voltage = .8V W/V_{DD} = −7V

Notes: 1. Effect noted at Pin 15 to V_{SS}. 2. Output Voltage Pin 15 to V_{SS}. 3. All Voltages measured with respect to V_{SS}.

Figure 1. Serial Data Encoder



CONSUMER PRODUCTS