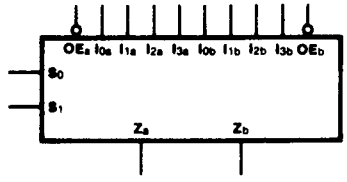
HD74AC253/HD74ACT253 • Dual 4-Input Multiplexer with 3-State Outputs.

Description

The HD74AC253/HD74ACT253 is a dual 4-input multiplexer with 3-state outputs. It can select two bits of data from four sources using common select inputs. The outputs may be individually switched to a high impedance state with a High on the respective Output Enable ($\overline{OE}$) inputs, allowing the outputs to interface directly with bus oriented systems.

- Multifunction Capability
- Noninverting 3-State Outputs
- Outputs Source/Sink 24 mA
- HD74ACT253 has TTL-Compatible Inputs

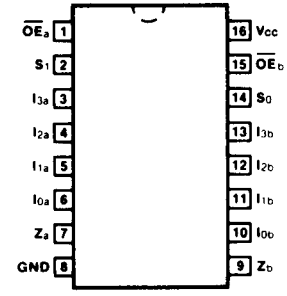
Logic Symbol



Pin Names

I_{0a}—I_{3a}	Side A Data Inputs
I_{0b}—I_{3b}	Side B Data Inputs
S_0, S_1	Common Select Inputs
$\overline{OE}_a$	Side A Output Enable Input
$\overline{OE}_b$	Side B Output Enable Input
Z_a, Z_b	3-State Outputs

Pin Assignment



(Top View)

Functional Description

The HD74AC253/HD74ACT253 contains two identical 4-input multiplexers with 3-state outputs. They select two bits from four sources selected by common Select inputs (S_0, S_1). The 4-input multiplexers have individual Output Enable ($\overline{OE}_a$, $\overline{OE}_b$) inputs which, when High, force the outputs to a high impedance (High Z) state. This device is the logic implementation of a 2-pole, 4-position switch, where the position of the switch is determined by the logic levels supplied to the two select inputs. The logic equations for the outputs are shown:

$$Z_a = \overline{OE}_a \cdot (I_{0a} \cdot \overline{S}_1 \cdot \overline{S}_0 + I_{1a} \cdot \overline{S}_1 \cdot S_0 + I_{2a} \cdot S_1 \cdot \overline{S}_0 + I_{3a} \cdot S_1 \cdot S_0)$$

$$Z_b = \overline{OE}_b \cdot (I_{0b} \cdot \overline{S}_1 \cdot \overline{S}_0 + I_{1b} \cdot \overline{S}_1 \cdot S_0 + I_{2b} \cdot S_1 \cdot \overline{S}_0 + I_{3b} \cdot S_1 \cdot S_0)$$

If the outputs of 3-state devices are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure that Output Enable signals to 3-state devices whose outputs are tied together are designed so that there is no overlap.

Truth Table

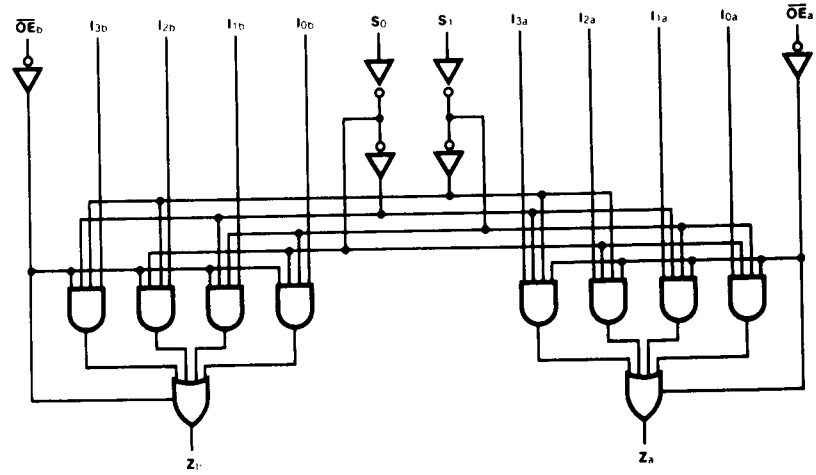
Select Inputs		Data Inputs				Output Enable	Outputs
S_0	S_1	I_0	I_1	I_2	I_3	$\overline{OE}$	Z
X	X	X	X	X	X	H	Z
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
H	L	X	L	X	X	L	L
H	L	X	H	X	X	L	H
L	H	X	X	L	X	L	L
L	H	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

H = High Voltage Level
L = Low Voltage Level
X = Immaterial
Z = High Impedance

Address inputs S_0 and S_1 are common to both sections.

HITACHI
Hitachi America Ltd. • 2210 O'Toole Ave. • San Jose, CA 95131 • (408) 435-8300

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics (unless otherwise specified)

Symbol	Parameter	Max	Unit	Condition
I_{CC}	Maximum Quiescent Supply Current	80	μA	V_{IN} = V_{CC} or Ground, V_{CC} = 5.5V, Ta = Worst Case
I_{CC}	Maximum Quiescent Supply Current	8.0	μA	V_{IN} = V_{CC} or Ground, V_{CC} = 5.5V, Ta = 25°C
I_{CCT}	Maximum Additional I_{CC}/Input (HD74ACT253)	1.5	mA	V_{IN} = V_{CC} − 2.1V, V_{CC} = 5.5V, Ta = Worst Case

AC Characteristics: HD74AC253

Symbol	Parameter	V_{CC}* (V)	Ta = +25°C, C_L = 50pF			Ta = −40°C to +85°C, C_L = 50pF		Unit
			Min	Typ	Max	Min	Max	
t_{PLH}	Propagation Delay Sn to Zn	3.3 5.0	1.0 1.0	8.5 6.5	15.5 11.0	1.0 1.0	17.5 12.5	ns
t_{PHL}	Propagation Delay Sn to Zn	3.3 5.0	1.0 1.0	9.5 7.0	16.0 11.5	1.0 1.0	18.0 13.0	ns
t_{PLH}	Propagation Delay In to Zn	3.3 5.0	1.0 1.0	7.0 5.5	14.5 10.0	1.0 1.0	17.0 11.5	ns
t_{PHL}	Propagation Delay In to Zn	3.3 5.0	1.0 1.0	7.5 5.5	13.0 9.5	1.0 1.0	15.0 11.0	ns
t_{PZH}	Output Enable Time	3.3 5.0	1.0 1.0	4.5 3.5	8.0 6.0	1.0 1.0	8.5 6.5	ns
t_{PZL}	Output Enable Time	3.3 5.0	1.0 1.0	5.0 3.5	8.0 6.0	1.0 1.0	9.0 7.0	ns
t_{PHZ}	Output Disable Time	3.3 5.0	1.0 1.0	5.5 5.0	9.5 8.0	1.0 1.0	10.0 8.5	ns
t_{PLZ}	Output Disable Time	3.3 5.0	1.0 1.0	5.0 4.0	8.0 7.0	1.0 1.0	9.0 7.5	ns

*Voltage Range 3.3 is 3.3V ± 0.3V
Voltage Range 5.0 is 5.0V ± 0.5V

AC Characteristics: HD74ACT253

Symbol	Parameter	V_{CC}* (V)	Ta = +25°C, C_L = 50pF			Ta = −40°C to +85°C, C_L = 50pF		Unit
			Min	Typ	Max	Min	Max	
t_{PLH}	Propagation Delay Sn to Zn	5.0	1.0	7.0	11.5	1.0	13.0	ns
t_{PHL}	Propagation Delay Sn to Zn	5.0	1.0	7.5	13.0	1.0	14.5	ns
t_{PLH}	Propagation Delay In to Zn	5.0	1.0	5.5	10.0	1.0	11.0	ns
t_{PHL}	Propagation Delay In to Zn	5.0	1.0	6.5	11.0	1.0	12.5	ns
t_{PZH}	Output Enable Time	5.0	1.0	4.5	7.5	1.0	8.5	ns
t_{PZL}	Output Enable Time	5.0	1.0	5.0	8.0	1.0	9.0	ns
t_{PHZ}	Output Disable Time	5.0	1.0	6.0	9.5	1.0	10.0	ns
t_{PLZ}	Output Disable Time	5.0	1.0	4.5	7.5	1.0	8.5	ns

*Voltage Range 5.0 is 5.0V ± 0.5V

Capacitance

Symbol	Parameter	Typ	Unit	Condition
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.5V
C_{PD}	Power Dissipation Capacitance	50.0	pF	V_{CC} = 5.0V

Package Information

In the HD74AC series of Advanced CMOS logic, either plastic DIP and small outline packages can be selected.
To order, please refer to the following package code.

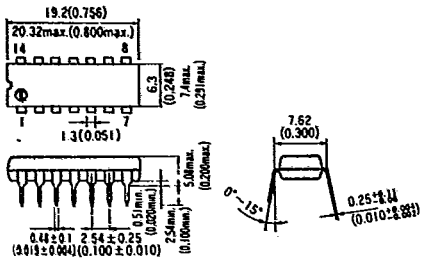
• Package code of Advanced CMOS Logic

HD74AC XXXX P

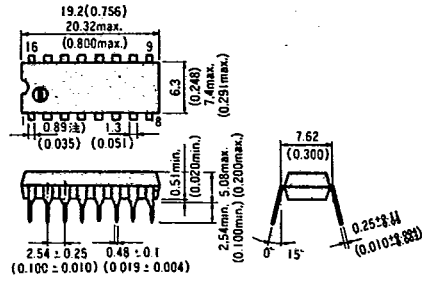
- Package code
  - P: Plastic DIP,
  - FP: Small outline package
- Individual device code
- 74AC: Commercial FACT
- 74ACT: Commercial TTL-Compatible Advanced CMOS
- Initial cad of Hitachi digital IC

Plastic DIP Package [Unit: mm (inch)]

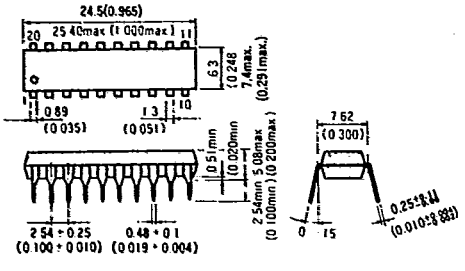
14 Pin type



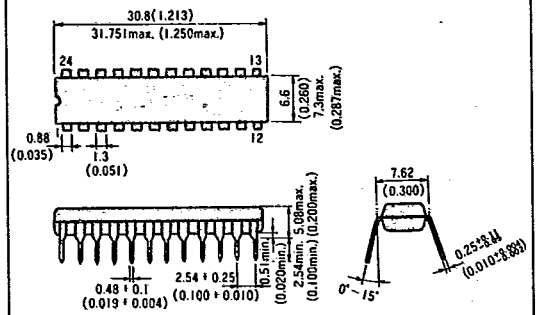
16 Pin type



20 Pin type



24 Pin type

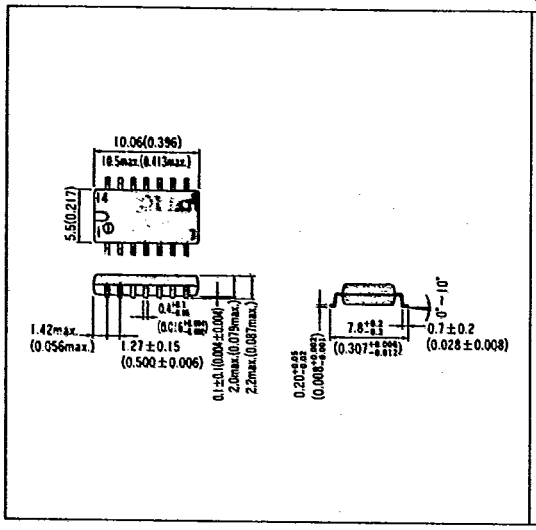


Hitachi America Ltd. • 2210 O'Toole Ave. • San Jose, CA 95131 • (408) 435-8300

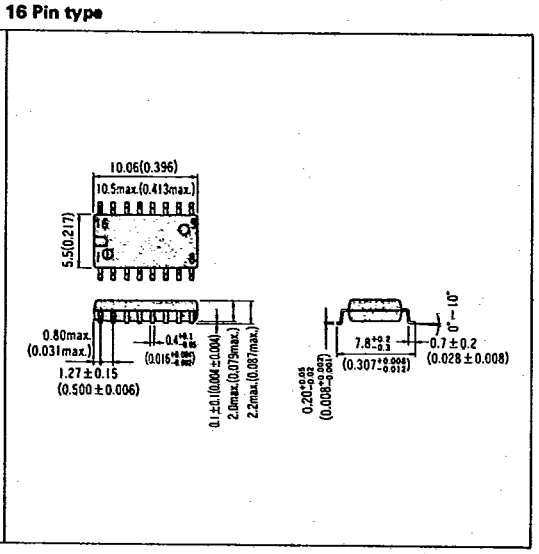
Package Information

Small Outline Package [Unit: mm (inch)]

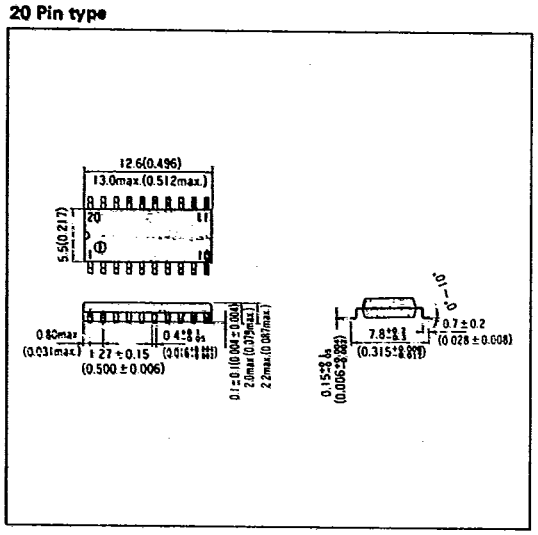
14 Pin type



16 Pin type



20 Pin type



HITACHI
Hitachi America Ltd. • 2210 O'Toole Ave. • San Jose, CA 95131 • (408) 435-8300