

Deserializer

UT54LVDS218

Features

- 15 to 75MHz shift clock support
- 50% duty cycle on receiver output clock
- Low power consumption
- Cold sparing all pins
- $\pm 1V$ common mode range (around +1.2V)
- Narrow bus reduces cable size and cost
- Up to 1.575 Gbps throughput
- Up to 197 Megabytes/sec bandwidth
- 325 mV (typ) swing LVDS devices for low EMI
- PLL requires no external components
- Rising edge strobe
- Operational Environment; total dose irradiation testing to MIL-STD-883 Method 1019
 - Total dose: 300 krad(Si) and 1 Mrad(Si)
 - Latchup immune (LET > 100 MeV-cm²/mg)
- Packaging options:
 - 48-lead flatpack (1.4 grams)
- Standard Microcircuit Drawing 5962-01535
 - QML Q and V compliant part
- Compatible with TIA/EIA-644 LVDS Standard

Introduction

The UT54LVDS218 Deserializer converts the three LVDS data streams back into 21 bits of CMOS/TTL data. At a transmit clock frequency of 75MHz, 21 bits of TTL data are transmitted at a rate of 525Mbps per LVDS data channel. Using a 75MHz clock, the data throughput is 1.575 Gbit/s (197 Mbytes/sec).

The UT54LVDS218 Deserializer allows the use of wide, high speed TTL interfaces while reducing overall EMI and cable size.

All pins have Cold Spare buffers. These buffers will be high impedance when V_{DD} is tied to V_{SS} .

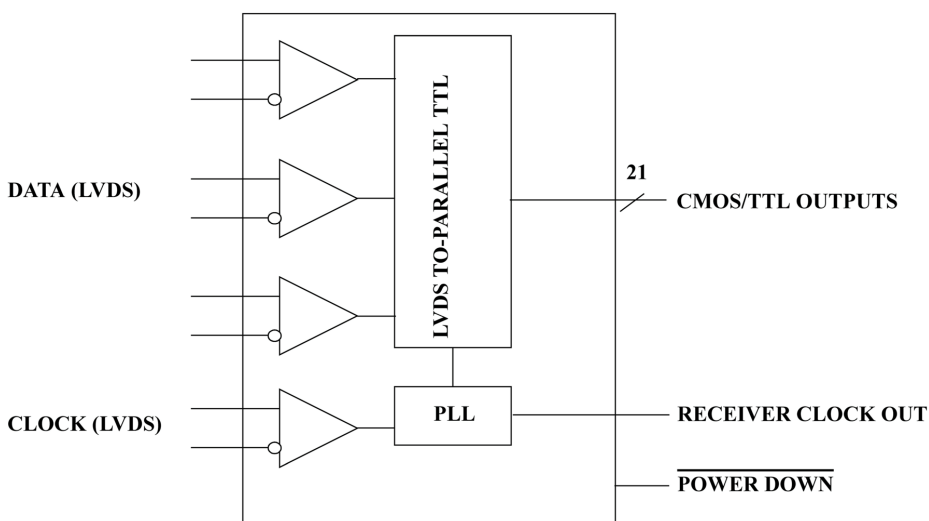


Figure 1. UT54LVDS218 Deserializer Block Diagram

UT54LVDS218

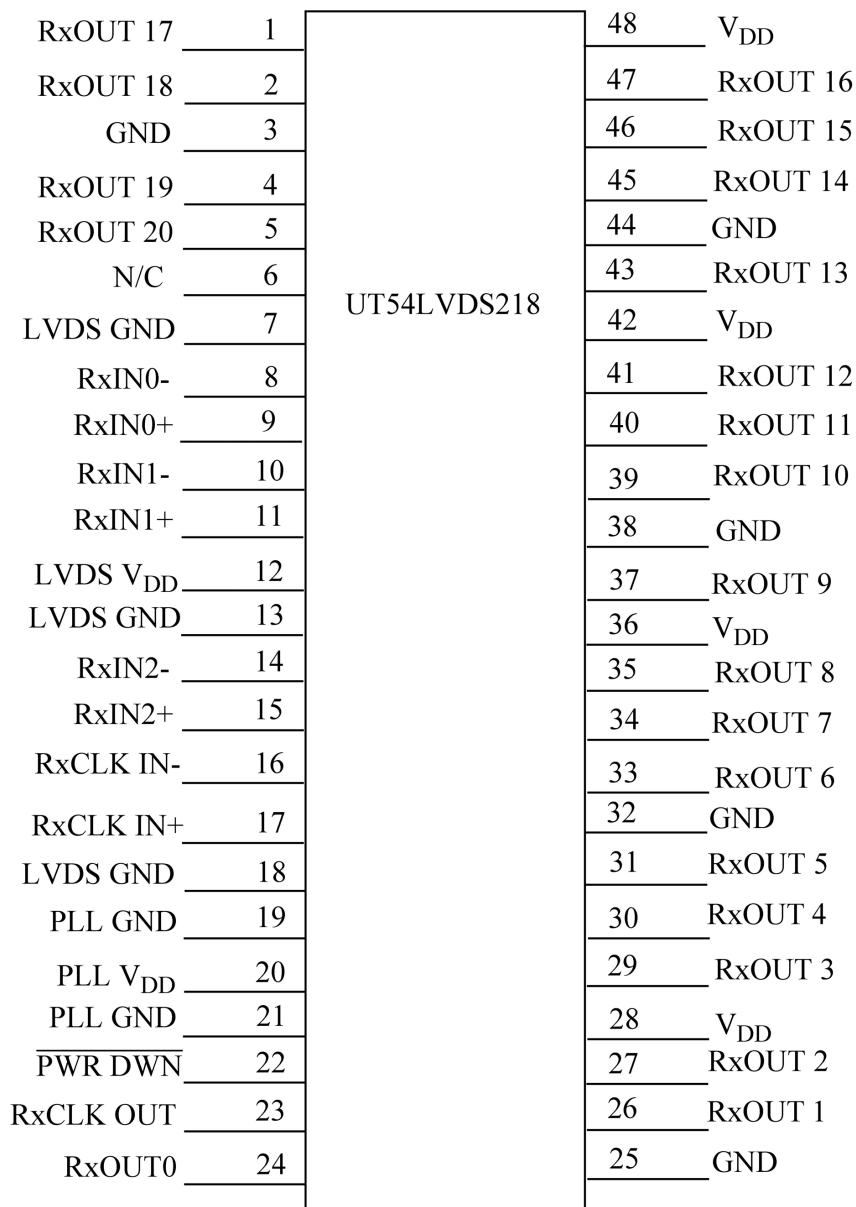


Figure 2. UT54LVDS218 Pinout

UT54LVDS218

Pin Description

| Pin Name | I/O | No. | Description |
|-----------------------------|-----|-----|--|
| RxIN+ | I | 3 | Positive LVDS differential data inputs ¹ |
| RxIN- | I | 3 | Negative LVDS differential data output ¹ |
| RxOUT | O | 21 | TTL level data outputs |
| RxCLK IN+ | I | 1 | Positive LVDS differential clock input |
| RxCLK IN- | I | 1 | Negative LVDS differential clock input |
| RxCLK OUT | O | 1 | TTL level clock output. The rising edge acts as data strobe. Pin name RxCLK OUT. |
| $\overline{\text{PWR DWN}}$ | I | 1 | TTL level input. When asserted (low input) the receiver outputs are low |
| V _{DD} | I | 4 | Power supply pins for TTL outputs and logic |
| GND | I | 5 | Ground pins for TTL outputs and logic |
| PLL V _{DD} | I | 1 | Power supply for PLL |
| PLL GND | I | 2 | Ground pin for PLL |
| LVDS V _{DD} | I | 1 | Power supply pin for LVDS pins |
| LVDS GND | I | 3 | Ground pins for LVDS inputs |

Notes:

- 1) These receivers have input fail-safe bias circuitry to guarantee a stable receiver output for floating or terminated receiver inputs. Under these conditions receiver inputs will be in a HIGH state. If a clock signal is present, data outputs will all be HIGH; if the clock input is also floating/terminated outputs will remain in the last valid state. A floating/terminated clock input will result in a LOW clock output.

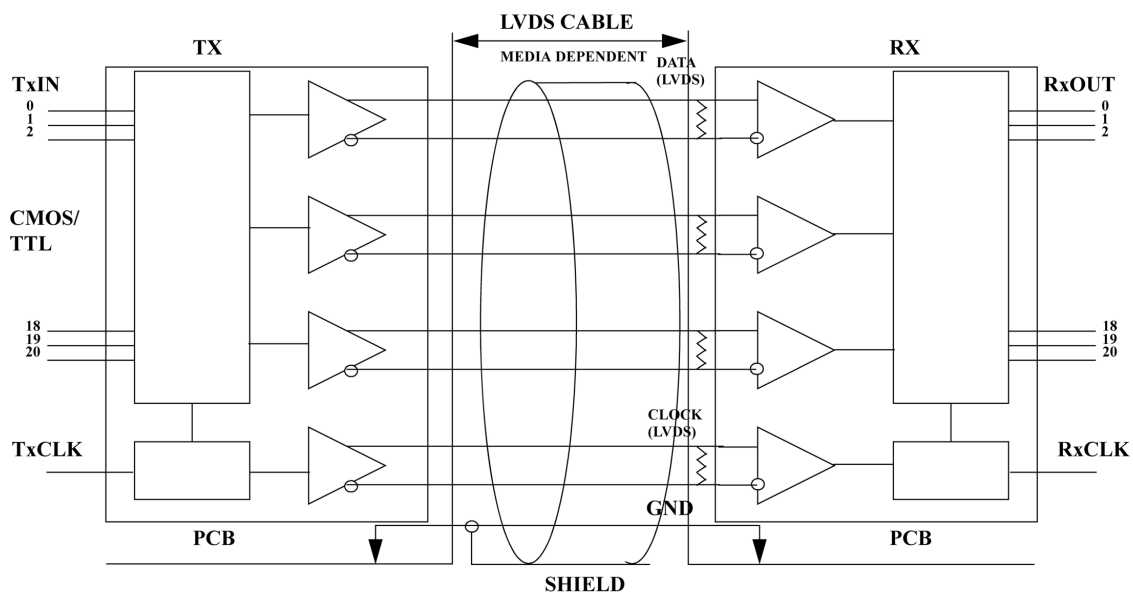


Figure 3. UT54LVDS218 Typical Application

Deserializer

UT54LVDS218

Operational Environment

| Parameter | Limit | Units |
|------------------------------|--------|-------------------------|
| Total Ionizing Dose (TID) | 1.0E6 | rad(Si) |
| Single Event Latchup (SEL) | >100 | MeV-cm ² /mg |
| Neutron Fluence ¹ | 1.0E13 | n/cm ² |

Notes:

- 1) Guaranteed but not tested.

Absolute Maximum Ratings ¹

(Referenced to V_{SS})

| Symbol | Parameter | Limits |
|------------------|---|----------------------------------|
| V _{DD} | DC supply voltage | -0.3 to 4.0V |
| V _{I/O} | Voltage on any pin | -0.3 to (V _{DD} + 0.3V) |
| T _{STG} | Storage temperature | -65 to +150°C |
| P _D | Maximum power dissipation | 1.25 W |
| T _J | Maximum junction temperature ² | +150°C |
| Θ _{JC} | Thermal resistance, junction-to-case ³ | 10°C/W |
| I _I | DC input current | ±10mA |

Notes:

- 1) Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, functional operation of the device at these or any other conditions beyond limits indicated in the operational sections is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability and performance.
- 2) Maximum junction temperature may be increased to +175°C during burn-in and steady-static life.
- 3) Test per MIL-STD-883, Method 1012.
- 4) For cold spare mode (V_{DD} = V_{SS}), V_{I/O} may be -0.3V to the maximum recommended operating V_{DD} +0.3V.

Recommended Operating Conditions

| Symbol | Parameter | Limits |
|-----------------|-------------------------|-----------------------|
| V _{DD} | Positive Supply voltage | 3.0 to 3.6V |
| T _C | Case temperature range | -55 to +125°C |
| V _{IN} | DC input voltage | 0V to V _{DD} |

Deserialzer

UT54LVDS218

DC Electrical Characteristics *1

($V_{DD} = 3.3V$ to $0.3V$; $-55^{\circ}C < T_C < +125^{\circ}C$); Unless otherwise noted, T_C is per the temperature noted.

| Symbol | Parameter | Condition | MIN | MAX | Unit |
|--|-----------------------------------|--|------|----------|---------|
| CMOS/TTL DC Specifications (PWR DWN, RXOUT) | | | | | |
| V_{IH} | High-level input voltage | | 2.0 | V_{DD} | V |
| V_{IL} | Low-level input voltage | | GND | 0.8 | V |
| V_{OL} | Low-level input voltage | $I_{OL} = 2mA$ | | 0.3 | V |
| V_{OH} | High-level input voltage | $I_{OL} = -0.4mA$ | 2.7 | | V |
| I_{IH} | High-level input current | $V_{IN}=3.6V$; $V_{DD} = 3.6V$ | -10 | +10 | μA |
| I_{IL} | Low-level input current | $V_{IN}=0V$; $V_{DD} = 3.6V$ | -10 | +10 | μA |
| V_{CL} | Input clamp voltage | $I_{CL} = -18mA$ | | -1.5 | V |
| I_{CS} | Cold Spare Leakage current | $V_{IN}=3.6V$; $V_{DD} = V_{SS}$ | -20 | +20 | μA |
| $I_{OS}^{2,3}$ | Output short circuit current | $V_{OUT} = 0V$ | -15 | -130 | mA |
| LVDS Receiver DC Specifications (IN+, IN-) | | | | | |
| V_{TH}^3 | Differential input high threshold | $V_{CM} = +1.2V$ | | +100 | mV |
| V_{T3}^4 | Differential input low threshold | $V_{CM} = +1.2V$ | -100 | | mV |
| V_{CMR}^4 | Common mode voltage range | $V_{ID}=210mV$ | 0.2 | 2.00 | V |
| I_{IN} | Input current | $V_{IN} = +2.4V$, $V_{DD} = 3.6V$ | -10 | +10 | μA |
| | | $V_{ID} = 0V$, $V_{DD} = 3.6V$ | -10 | +10 | μA |
| I_{CSIN} | Cold Spare Leakage Current | $V_{IN} = 3.6V$, $V_{DD} = V_{SS}$ | -20 | +20 | μA |
| Supply Current | | | | | |
| I_{CC}^3 | Active supply current | $CL=8pF$ (see Figure 5) | | 105 | mA |
| I_{CCPD} | Power down supply current | $\overline{PWR\ DWN} = Low$, LVDS inputs = logic low, $V_{DD} = 3.6V$ | | 2.0 | mA |

Notes:

*For devices procured with a total ionizing dose tolerance guarantee, the post-irradiation performance is guaranteed at $25^{\circ}C$ per MIL-STD-883 Method 1019, Condition A up to the maximum TID level procured.

- 1) Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground.
- 2) Output short circuit current (I_{OS}) is specified as magnitude only, minus sign indicates direction only. Only one output should be shorted at a time, for a maximum duration of one second.
- 3) Guaranteed by characterization.
- 4) Tested functionally.

UT54LVDS218

Receiver Switching Characteristics *1

($V_{DD} = 3.0V$ to $3.6V$; $T_c = -55^{\circ}C$ to $+125^{\circ}C$); Unless otherwise noted, T_c is per the temperature ordered.

| Symbol | Parameter | | MIN | MAX | Unit |
|---------------------|--|---------|-------|-------|---------|
| CLHT ³ | CMOS/TTL Low-to-High Transition Time (Figure 5) | | | 3.5 | ns |
| CHLT ³ | CMOS/TTL High-to-Low Transition Time (Figure 5) | | | 3.5 | ns |
| RSPos0 ³ | Receiver Input Strobe Position for Bit 0 (Figure 10) | | 0.50 | 1.24 | ns |
| RSPos1 ³ | Receiver Input Strobe Position for Bit 1 (Figure 10) | | 2.41 | 3.15 | ns |
| RSPos2 ³ | Receiver Input Strobe Position for Bit 2 (Figure 10) | f=75MHz | 4.31 | 5.05 | ns |
| RSPos3 ³ | Receiver Input Strobe Position for Bit 3 (Figure 10) | f=75MHz | 6.22 | 6.96 | ns |
| RSPos4 ³ | Receiver Input Strobe Position for Bit 4 (Figure 10) | f=75MHz | 8.12 | 8.86 | ns |
| RSPos5 ³ | Receiver Input Strobe Position for Bit 5 (Figure 10) | f=75MHz | 10.03 | 10.77 | ns |
| RSPos6 ³ | Receiver Input Strobe Position for Bit 6 (Figure 10) | f=75MHz | 11.93 | 12.67 | ns |
| RCOP ³ | RxCLK OUT Period (Figure 6) | f=75MHz | 13.3 | 66.7 | ns |
| RCOH ³ | RxCLK OUT High Time (Figure 6) | f=75MHz | 3.6 | | ns |
| RCOL ³ | RxCLK OUT Low Time (Figure 6) | f=75MHz | 3.6 | | ns |
| RSRC ⁴ | RxOUT Setup to RxCLK OUT (Figure 6) | f=75MHz | 3.5 | | ns |
| RHRC ⁴ | RxOUT Hold to RxCLK OUT (Figure 6) | f=75MHz | 3.5 | | ns |
| RCCD ² | RxCLK IN to RxCLK OUT Delay (Figure 7) | f=75MHz | 3.4 | 8.3 | ns |
| RPLLS ⁵ | Receiver Phase Lock Loop Set (Figure 8) | f=75MHz | | 10 | ms |
| RPDD | Receiver Powerdown Delay (Figure 9) | f=75MHz | | 2 | μ s |

Notes:

*For devices procured with a total ionizing dose tolerance guarantee, the post-irradiation performance is guaranteed at 25°C per MIL-STD-883 Method 1019, Condition A up to the maximum TID level procured.

- 1) Receiver Skew Margin is defined as the valid data sampling region at the receiver inputs. This margin takes into account the transmitter pulse positions (min and max) and the receiver input setup and hold time (internal data sampling window). This margin allows LVDS interconnect skew, inter-symbol interference (both dependent on type/length of cable), and source clock jitter less than 250 ps (calculated from $T_{POS} - R_{POS}$) - see Figure 11.
- 2) Total latency for the channel link chipset is a function of clock period and gate delays through the transmitter (TCCD) and receiver (RCCD). The total latency for LVDS217 Serializer and the LVDS218 Deserializer is $(T + TCCD) + 2*T + RCCD$, where $T =$ Clock period.
- 3) Guaranteed by characterization.
- 4) Guaranteed by design.
- 5) Tested functionally.

UT54LVDS218

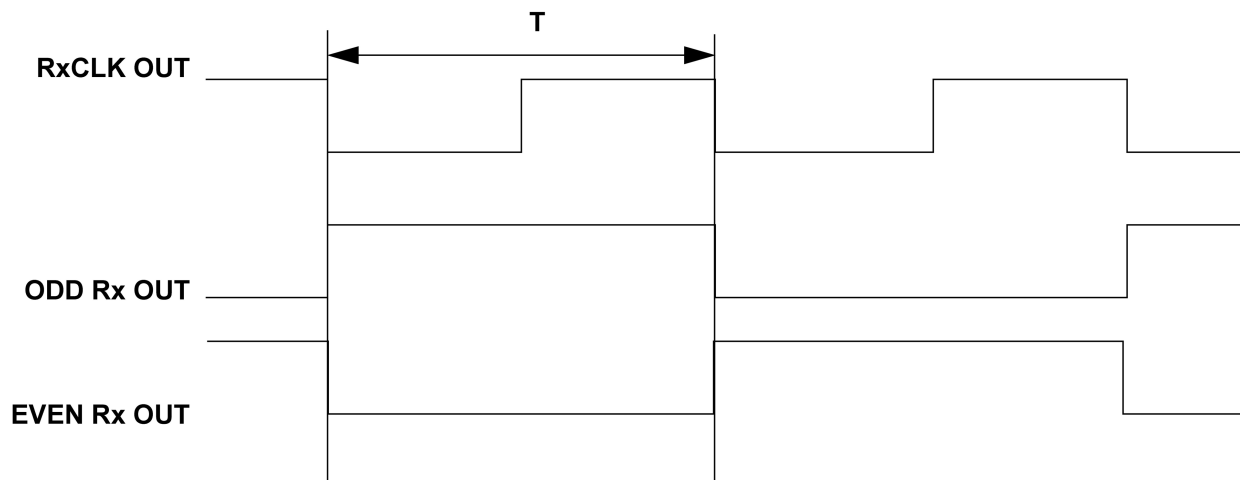


Figure 4. Test Pattern

AC Timing Diagrams

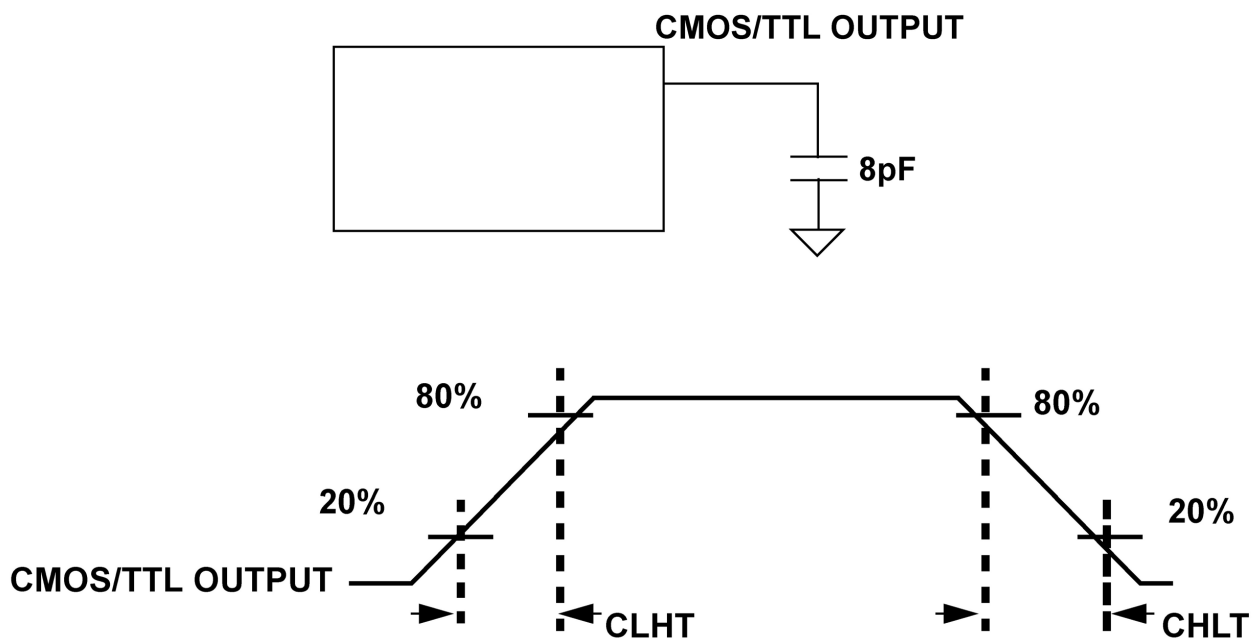


Figure 5. UT54LVDS218 Output Load and Transition Times

UT54LVDS218

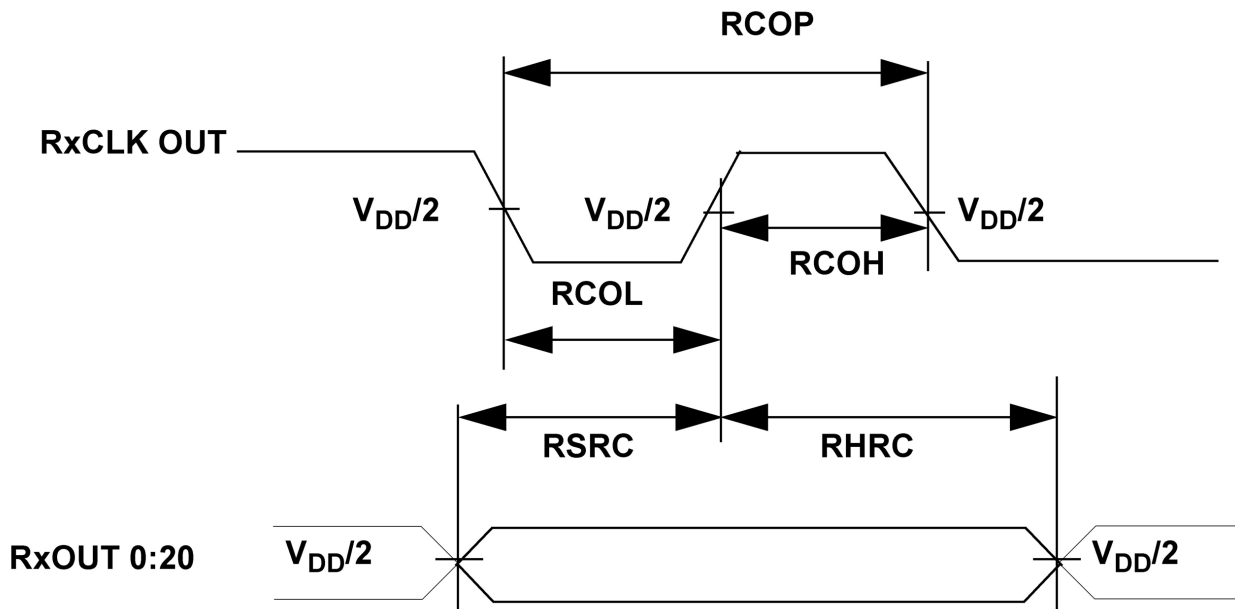


Figure 6. UT54LVDS218 Setup/Hold and High/Low Times

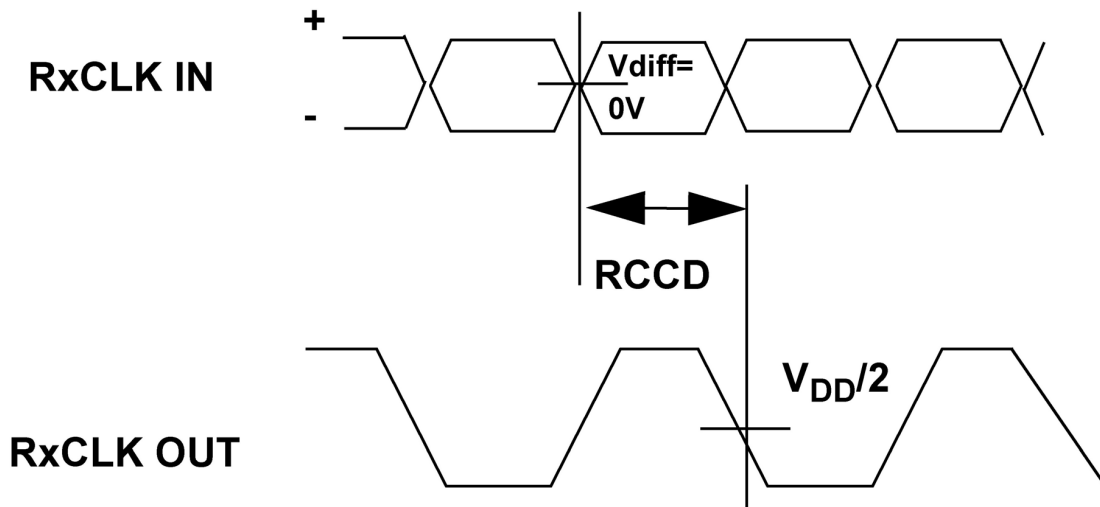


Figure 7. UT54LVDS218 Clock-to-Clock Out Delay

UT54LVDS218

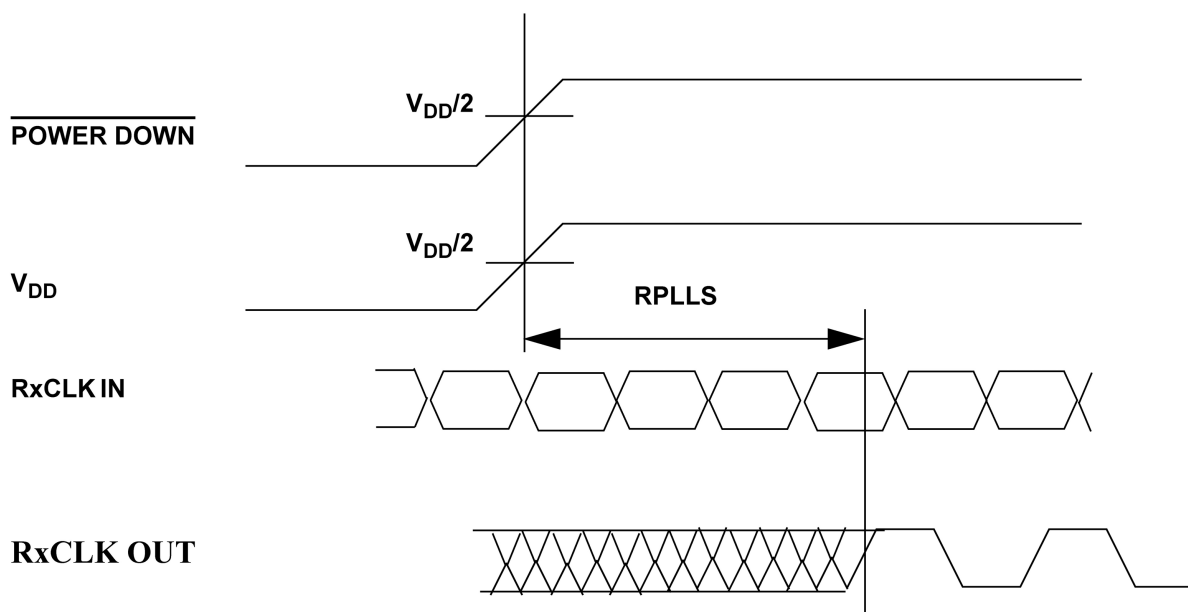


Figure 8. UT54LVDS218 Phase Lock Loop Set Time

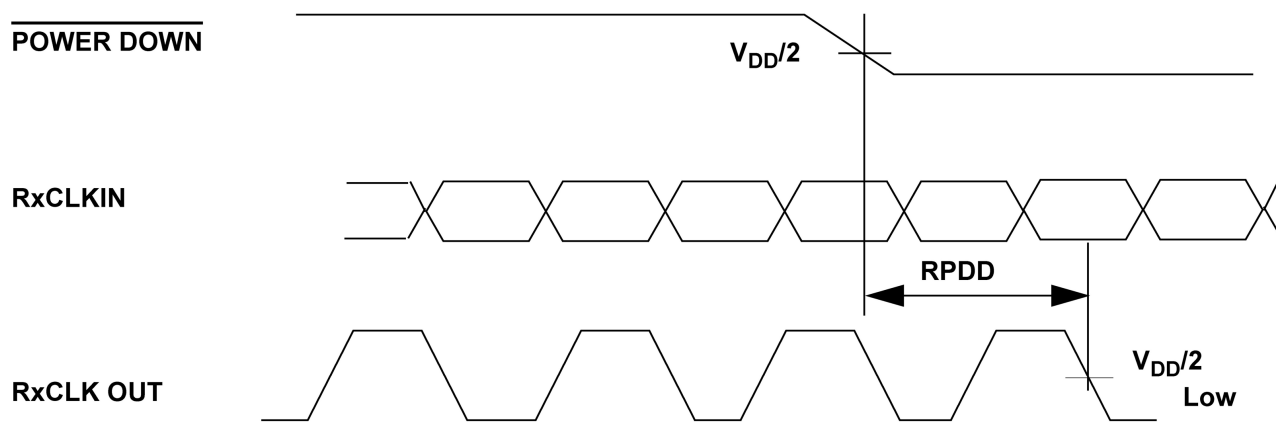


Figure 9. Receiver Powerdown Delay

UT54LVDS218

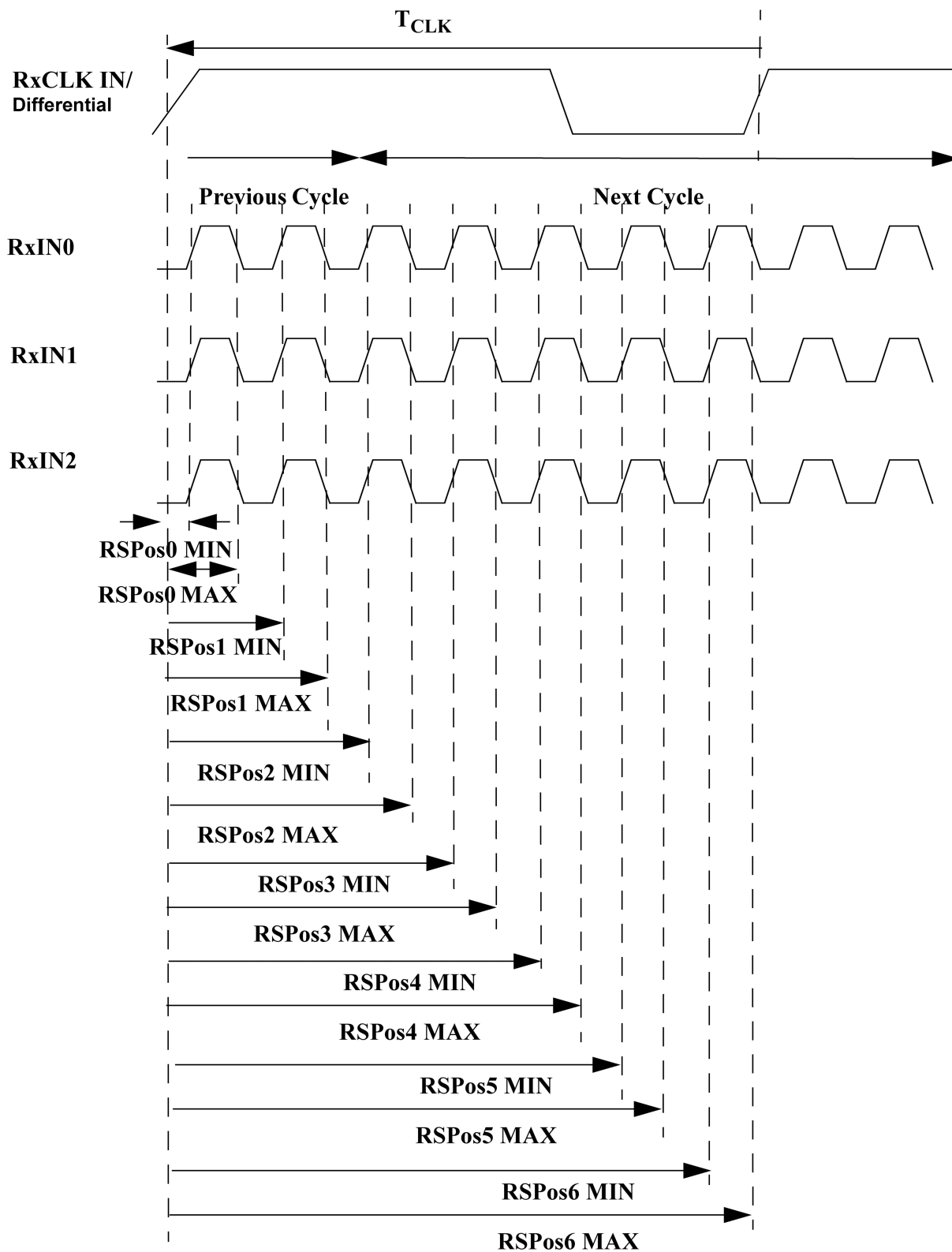
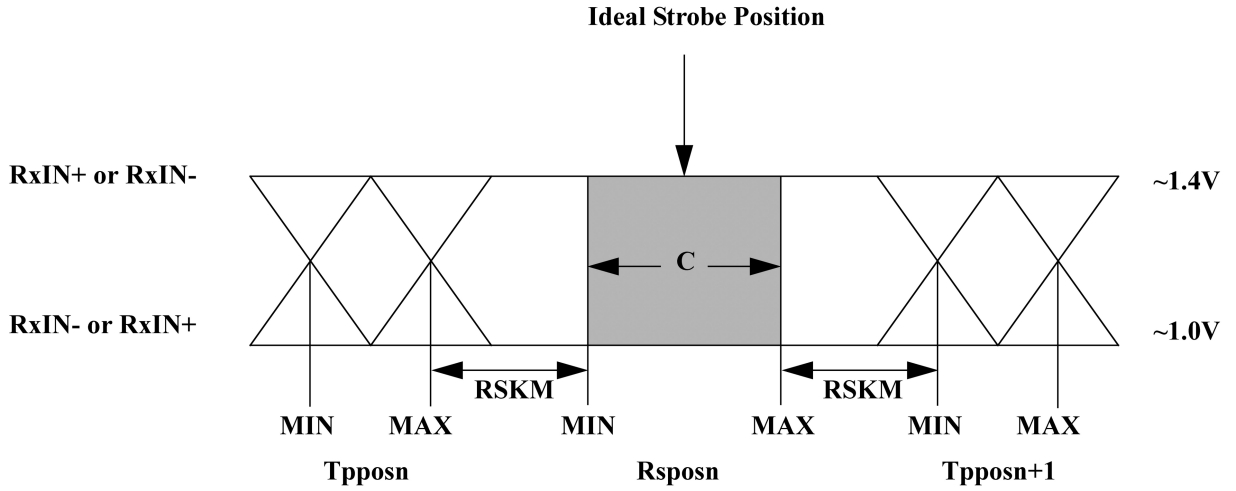


Figure 10. Receiver LVDS Input Strobe Position

UT54LVDS218



C - Setup and Hold Time (Internal data sampling window) defined by **RSPosN** (receiver input strobe position min and max)

TPPosN - Transmitter output pulse position (min and max)

Cable Skew – based on type and length, typically 10 ps-40 ps per foot, media dependent

Source Clock Jitter - Cycle-to-cycle jitter is less than 250 ps at 75MHz.

ISI - Inter-symbol interference, dependent on interconnect length, may be zero.

$$RSKM(Side) > \frac{\text{Cable Skew}}{2} + \frac{\text{Source Clock Jitter}}{2} + \frac{ISI}{2}$$

Figure 11. Receiver LVDS Skew Margin

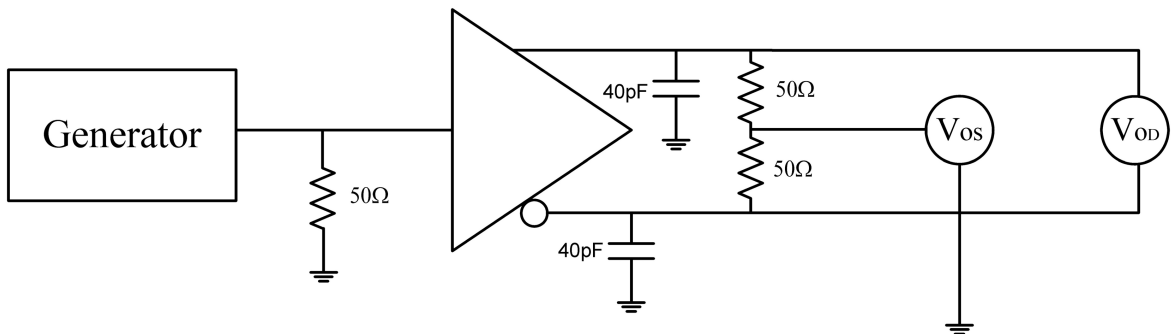


Figure 12. Driver **V_{OD}** and **V_{OS}** Test Circuit or Equivalent Circuit

UT54LVDS218

Packaging

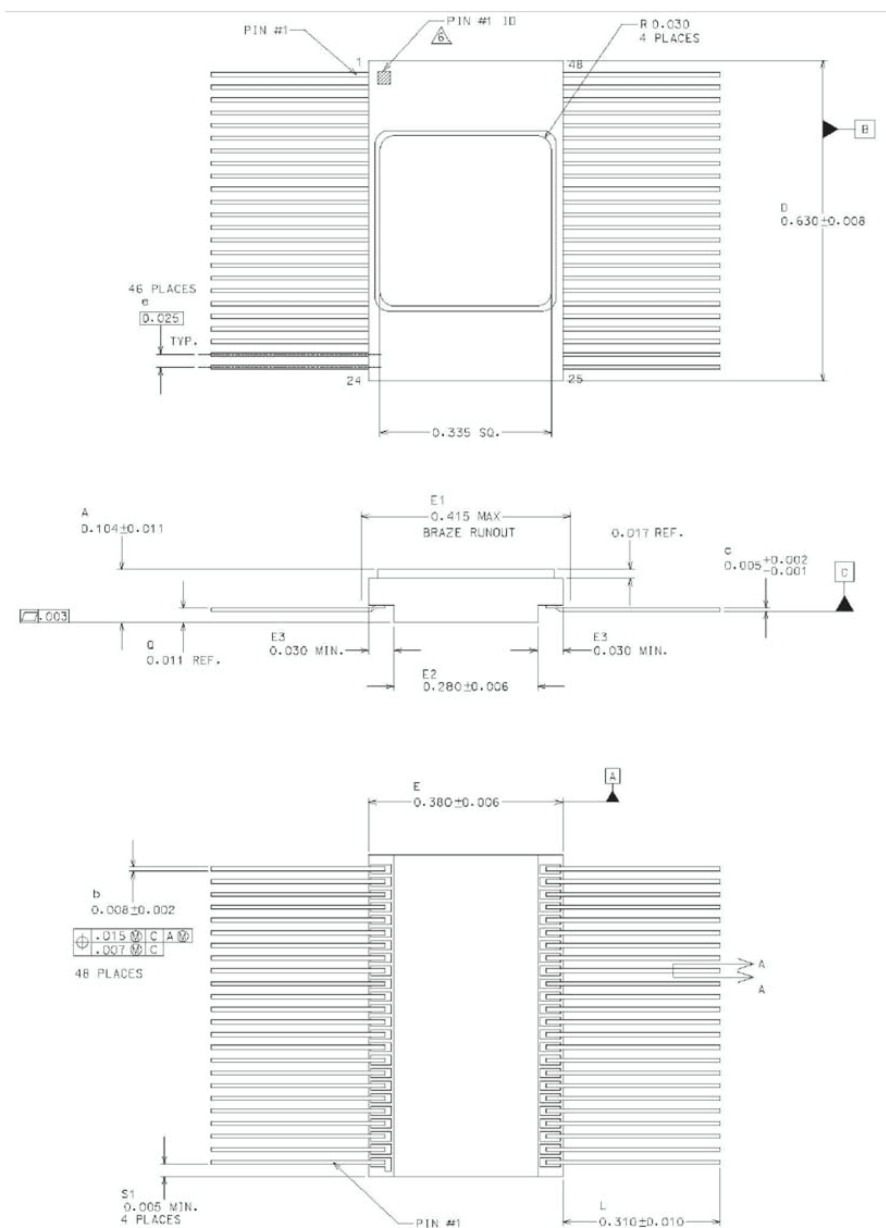


Figure 12. 48-Lead Flatpack

Notes:

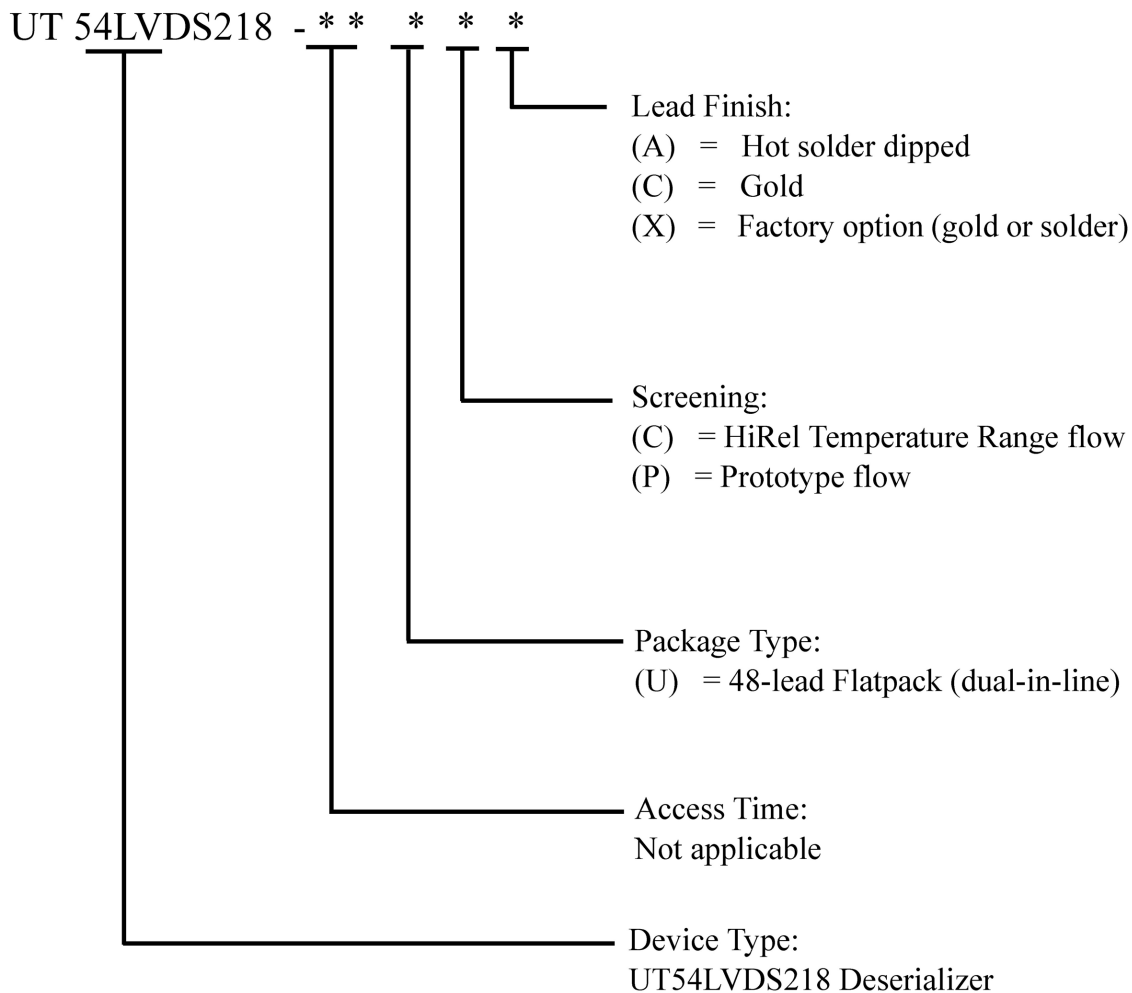
- 1) All exposed metalized areas are gold plated over electroplated nickel per MIL-PRF-38535.
- 2) The lid is electrically connected to VSS.
- 3) Lead finishes are in accordance with MIL-PRF-38535.
- 4) Lead position and colanarity are not measured.
- 5) ID mark symbol is vendor option.
- 6) With solder, increase maximum by 0.003.

Deserializer

UT54LVDS218

Ordering Information

UT54LVDS218 Deserializer:



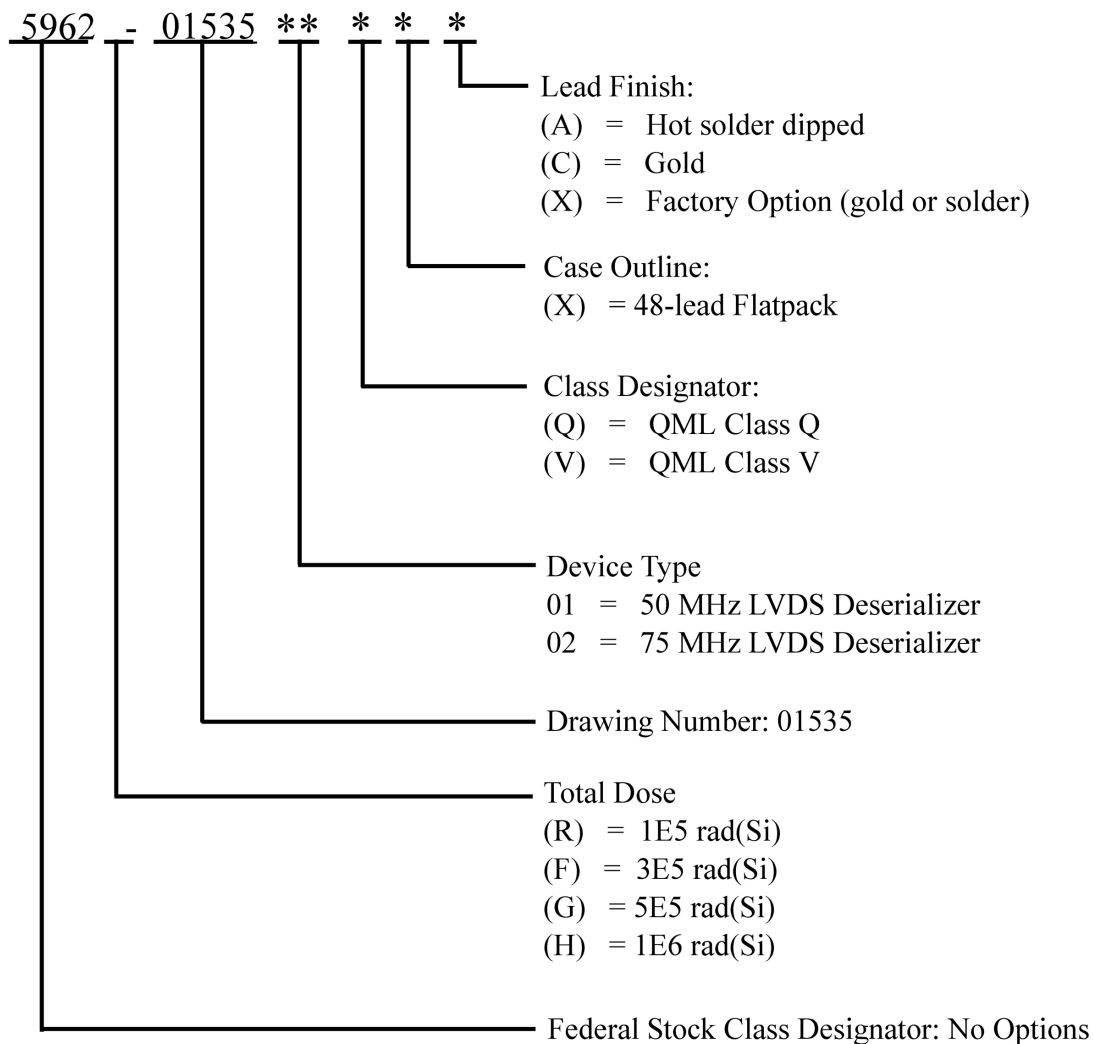
Notes:

- 1) Lead finish (A,C, or X) must be specified.
- 2) If an "X" is specified when ordering, then the part marking will match the lead finish and will be either "A" (solder) or "C" (gold).
- 3) Prototype flow per CAES Manufacturing Flows Document. Tested at 25°C only. Lead finish is GOLD ONLY. Radiation neither tested nor guaranteed.
- 4) HiRel Temperature Range flow per CAES Manufacturing Flows Document. Devices are tested at -55°C, room temp, and 125°C. Radiation neither tested nor guaranteed.

Deserializer

UT54LVDS218

UT54LVDS218 Deserializer: SMD



Notes:

- 1) Lead finish (A,C, or X) must be specified.
- 2) If an "X" is specified when ordering, then the part marking will match the lead finish and will be either "A" (solder) or "C" (gold).
- 3) Total dose radiation must be specified when ordering. QML Q and QML V not available without radiation hardening.

UT54LVDS218

Data Sheet Revision History

| REV | Revision Date | Description of Change | Author |
|-------|---------------|--|--------|
| 1.0.0 | 10-08 | Last official release | MM |
| 1.0.1 | 9-17-15 | Page 1, added package weight. Applied new CAES Data Sheet template to the document. | MM |

Datasheet Definitions

| | DEFINITION |
|-----------------------|---|
| Advanced Datasheet | CAES reserves the right to make changes to any products and services described herein at any time without notice. The product is still in the development stage and the datasheet is subject to change . Specifications can be TBD and the part package and pinout are not final . |
| Preliminary Datasheet | CAES reserves the right to make changes to any products and services described herein at any time without notice. The product is in the characterization stage and prototypes are available. |
| Datasheet | Product is in production and any changes to the product and services described herein will follow a formal customer notification process for form, fit or function changes. |

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