2.5 Gbit/s Clock and Data Recovery Circuit GD16506

Advance Information

General Description

The GD16506 is a high performance monolithic integrated 2.2 to 2.7 Gbit/s *Clock and Data Recovery* (CDR) device applicable for optical communication systems including:

- SDH STM-16
- SONET OC-48.

The CDR contains all circuits needed for reliable acquisition and lock of the VCO phase onto the incoming data.

The electrical input sensitivity is better than 20 mV. Optical receivers with sensitivity better than -34 dBm have been obtained without optical pre-amplification.

The device meets all ITU-T jitter requirements when used with the recommended loop filter (jitter tolerance, -transfer and -generation).

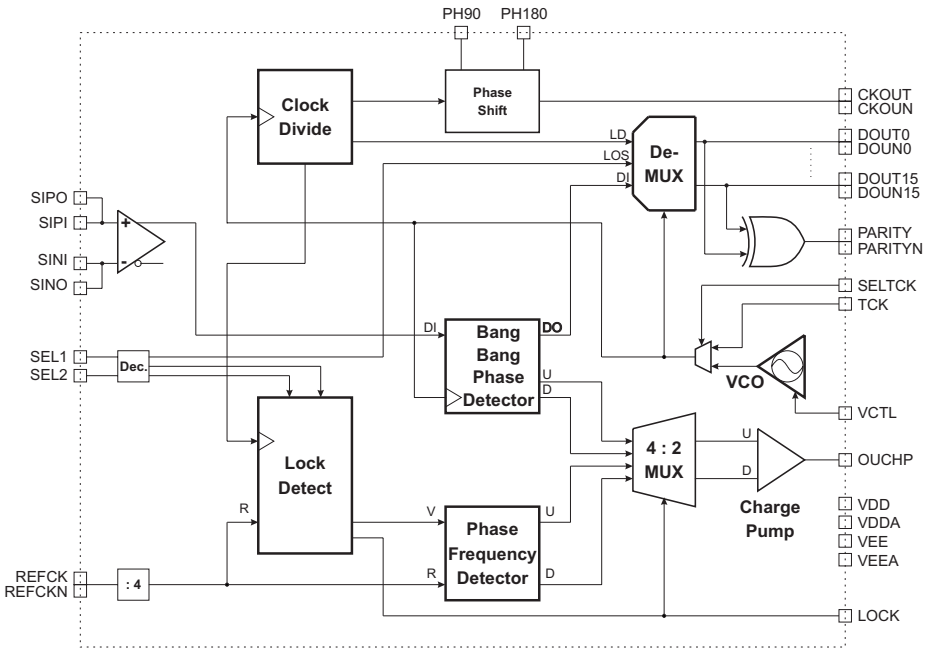
The integrated 1:16 demultiplexer with differential ECL outputs ensures a simple and universal interface to the system CMOS ASICs.

The 155 MHz output clock is maintained within 500 ppm tolerance even in absence of data.

All high speed I/O levels are 50 Ω true ECL compatible. The data input has improved sensitivity and is connected via a 50 Ω loop through transmission line to minimize stub related reflections. All ECL level signal outputs are differential, allowing either single ended or differential operation.

The power dissipation is approximately 2.0 W.

It is packed in a plastic fpBGA with internal 50 Ω transmission lines, heat transport to PCB, reduced mechanical stress and removed requirement for a heat sink. All signals are available in two outher ring for easy routing.



Features

- Clock and Data Recovery covering 2.2 up to 2.7 Gbit/s.
- SDH STM-16, SONET OC-48 compatible.
- Differential Data inputs with 20 mV sensitivity.
- Differential ECL Data and Clock outputs.
- Acquisition time < 500 µs
- Few external passive components needed.
- 50 Ω Loop-Through data inputs for higher sensitivity.
- Single supply operation.
- Power dissipation: approx. 2.0 W
- Available in:
  - 144 lead fpBGA
  - 68 pin MLC

Applications

- Clock and Data Recovery for:
  - SDH STM-16
  - SONET OC-48 systems

The main application of the GD16506 is as Clock and Data Recovery in optical communication systems including:

- SDH STM-16
- SONET OC-48

It integrates:

- a Voltage Controlled Oscillator (VCO)
- a Lock Detect Circuit
- a Frequency Detector (PFD)
- a 1:16 DeMUX.
- a Bang-Bang Phase Detector

into a clock and data recovery circuit followed by a 1:16 demultiplexer with differential ECL data and clock outputs.

VCO

The VCO is a low noise LC-type differential oscillator with a tuning range from 2.2 to 2.7 GHz. Tuning is done by applying a voltage to the VCTL pin.

Lock Detect Circuit

The Lock Detect Circuit continuously monitors the difference between the reference clock, which is at 1/16 of the data rate, and the divided VCO clock. If the reference clock and the divided VCO frequency differs by more than 500 ppm (or 2000 ppm, selectable), it switches the PFD into the PLL in order to pull the VCO back inside the lock-in range. This mode is called **the acquisition mode.** Once the VCO is inside the lock-range the lock-detection circuit switches the Bang-Bang phase detector into the PLL in order to lock to the data signal. This mode is called **CDR mode**. The status of the lock-detection circuit is given by output pin LOCK. In acquisition mode LOCK is low.

When the CDR has acquired lock the Frame Detection/ Alignment circuit search for a framing pattern and when found the parallel data output are aligned on a 16 bit boundary.

In acquisition mode a PFD is used to ensure predictable lock up conditions for the GD16506 by locking the VCO to an external reference clock source. It is only used during acquisition and pulls the VCO into the lock range where the Bang-Bang phase detector is capable of acquiring lock. The PFD is made with digital set/reset cells giving it a true phase and frequency characteristic. The reference clock input, REFCK, to the PFD is at 1/16 of the data rate.

Bang-Bang Phase Detector

The Bang-Bang phase detector is used in **CDR mode** as a true digital type detector, producing a binary output. It samples the incoming data twice each bit period, once on the transition of the previous bit period and once in the middle of the bit period. When a transition occurs between 2 consecutive bits - the value of the sample in the transition between the bits determines whether the VCO clock leads or lags the data. Hence the *Phase Locked Loop* (PLL) is controlled by the bit transition point, thereby ensuring that data is sampled in the middle of the eye, once the system is in CDR mode. The external loop filter controls the characteristics of the PLL.

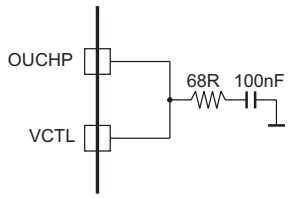


Figure 1. *Loop Filter*

The binary output of either the PFD or the Bang-Bang phase detector (depending of the mode of the lock-detection circuit) is fed to a charge pump capable of sinking or sourcing current or tristating. The output of the charge pump is filtered through the loop filter and controls the tuning-voltage of the VCO.

A result of the continuous lock-detect monitoring circuit is that the VCO frequency never deviates more than 500 ppm (2000 ppm) from the reference clock before the PLL is considered to be 'Out of Lock'. Hence the acquisition time is predictable and short and the output clock CKOUT is always kept within the 500 ppm (2000 ppm) limits ensuring safe clocking of down stream circuitry.

The LOCK Signal

The LOCK output may be used to generate *Loss of Signal* (LOS). The time for LOCK to assert is predictable and short, equal to the time to go into lock, but the time for LOCK to de-assert must be considered. When the line is down (i.e. no information received) the optical receiver circuit may produce random noise. It is possible that this random noise will keep the GD16506 within the 500 ppm (2000 ppm) range of the line frequency, hence LOCK will remain asserted for a non-deterministic time. This may be prevented by injecting a small current at the loop filter node, which actively pulls the PLL out of the lock range when the output of the phase detector acts randomly. The negligible penalty paid is a static phase error. However, due to the nature of the phase detector the error will be small (few degrees), forcing the loop to be at one edge of the error-function shaped transfer characteristic of the detector.

If the LOS is generated by the optical circuitry, the SEL1 and SEL2 may be configured to force the PLL to use the Frequency Detector regardless of Lock Detect status and at the same time force all outputs to logic low.

Configuration signals, SEL1 and SEL2 may be tied to VDD or VEE directly. A special design of these input buffers allow this option. The combination resets all Flip Flops, and sets both Up and Down active at the input of the Charge Pump, leaving the output in the middle of its output range. Since the circuit is self synchronizing, reset need not be asserted during power up.

Data Input

The input amplifier (pins SIPI / SINI and SIPO / SINO) is designed as a limiting amplifier with a sensitivity better than ±20 mV (differential). The inputs may be either AC or DC coupled. In either case input termination is made through pins SIPO / SINO. If the inputs are AC-coupled the amplifier features an internal offset cancelling DC feedback. All four AC coupling capacitors should be identical for optimum perfomance. Notice that the offset cancellation will only work when the input is differential and AC-coupled as shown in the Figure below.

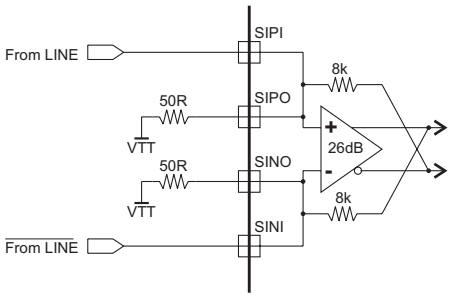


Figure 2. *DC Coupled Input (Ignoring internal offset compensation)*

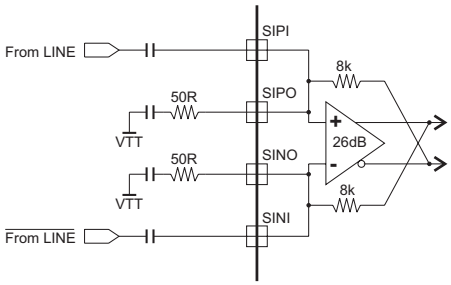


Figure 3. *AC Coupled Input (Using internal offset compensation)*

Data Outputs

Following the CDR block the data is 1:16 demultiplexed, and output together with a 155 MHz clock. The data and clock outputs are differential ECL outputs that should be terminated via 50 Ω to -2 V. A phase selector is includes, to enable the user to select the phase between 155 MHz clock and 155 Mbit data, in four stages, with 90º steps.

Pin List

Mnemonic:	Pin No.: 144 ld.	68 pin	Pin Type:	Description:
SIP, SIPO	E1, F1	62, 61	Anl. IN	Loop-through serial positive differential input. Optimised for max. sensitivity; may be used as ECL input.
SIN, SINO	D1, C1	63, 64	Anl. IN	Loop-through serial negative differential input. Optimised for max. sensitivity; may be used as ECL input.
PH90, PH180	J1, H1	58, 59	CML OUT	Phase select (90° and180°). Between DOUTx/DOUNx and CKOUT
DOUT0, DOUN0 DOUT1, DOUN1 DOUT2, DOUN2 DOUT3, DOUN3 DOUT4, DOUN4 DOUT5, DOUN5 DOUT6, DOUN6 DOUT7, DOUN7 DOUT8, DOUN8 DOUT9, DOUN9 DOUT10, DOUN10 DOUT11, DOUN11 DOUT12, DOUN12 DOUT13, DOUN13 DOUT14, DOUN14 DOUT15, DOUN15	A11, A10 B12, A12 D11, C12 D12, E11 F12, F11 G12, G11 H12, H11 J12, J11 L12, K12 M11, M12 M9, M10 L8, L9 M7, M8 M6, L7 M4, M5 L3, M3	12, 11 15, 13 19, 16 22, 20 24, 23 27, 25 29, 28 32, 30 36, 33 39, 37 41, 40 44, 42 46, 45 49, 47 53, 50 56, 54	ECL OUT	Retimed differential data output from DeMUX, bit 15 is the first received. After frame synchronisation, the data is byte-aligned with the first A2 byte placed at bit 15 through 8. When LOCK = “0" or SEL1= ”1" and SEL2 = “0" (LOS), all outputs will be logic low
REFCK, REFCKN	A6, A7	6, N/A	ECL IN	155 MHz reference clock input. Both biased to -1.3 V in 68BA version
CKOUT, CKOUN	A9, B9	10, 8	ECL OUT	Regenerated differential output clock, 155 MHz.
SEL1, SEL2	A1, E12	67, 18	ECL IN	Single-ended inputs, PLL set-up of Internal/ External switch mode and LOCK: SEL1 SEL2 0 0 Auto lock, 500ppm. 0 1 Global Reset for test purpose only. 1 0 Manual, Phase/ Freq. det, 500 ppm,LOS mode. 1 1 Manual, Phase detector, 2000 ppm. The LOS mode cause all 16 data outputs, FP and LOCK into logic low.
LOCK	B6	5	ECL OUT	Single ended CDR Lock alarm output. When low, the divided VCO freq. deviates more than 500/2000 ppm from REFCK. When system is unlocked, all 16 data outputs and FP will be logic low. When SEL1 = "1" and SEL2 = "0" (LOS), the LOCK will be logic low.
PAR, PARN	M1, L1	57, N/A	ECL OUT	Parity output (XOR of the 16 bit output).
VCTL	A3	2	Anl. IN	VCO control voltage input.
OUCHP	A4	3	Anl. OUT	Phase detector or Phase / frequency charge pump output.
TCK	A2	66	ECL IN	DC - functional and parametric test clock input. Bypasses the VCO when SELTCK is high.
VDD	B1, C2, D2, D4..9, E2, E4..9, F2, F4..9, G1, G2, G4..9, H2, H4..H9, J2, J4..J9, K1, K2, M2	4, 9, 14, 21, 26, 31, 38, 43, 48, 55, 60, 65	PWR	0 V Power for core and ECL I/O.

Mnemonic:	Pin No.: 144 ld.	68 pin	Pin Type:	Description:
VEE	C3..C10, D3, D10, E3, E10, F3, F10, G3, G10, H3, H10, J3, J10, K3..9	34, 35, 68	PWR	-5 V Power for core and ECL I/O.
VDDA	A5, B5	17	PWR	0 V Power for VCO
VEEA	B3, B4	52	PWR	-5 V Power for VCO.
SELTCK	B2	1	PWR	Select test clock, for DC test only, connect to VEE.
VCSREF	L6	N/A	ANALOG	Internal reference voltage, leave open
NC	A8, B7, B8, B10, B11, C11, K10, K11, L4, L5, L2, L10, L11	7, 51		Not used. Reserved for future use.

Package Pinout

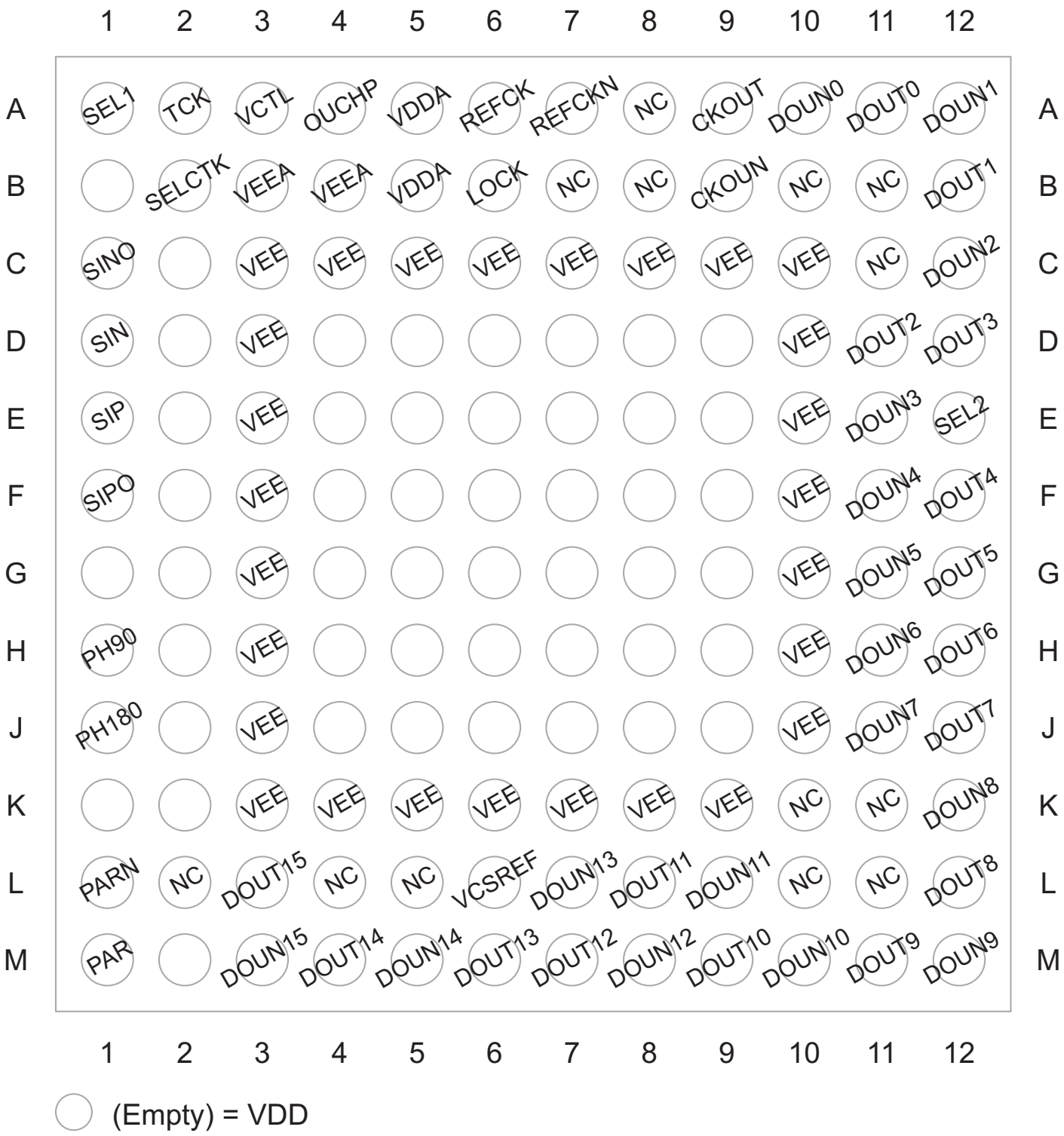


Figure 4. *Package Pinout, 144ld - Top View (seen through the package)*

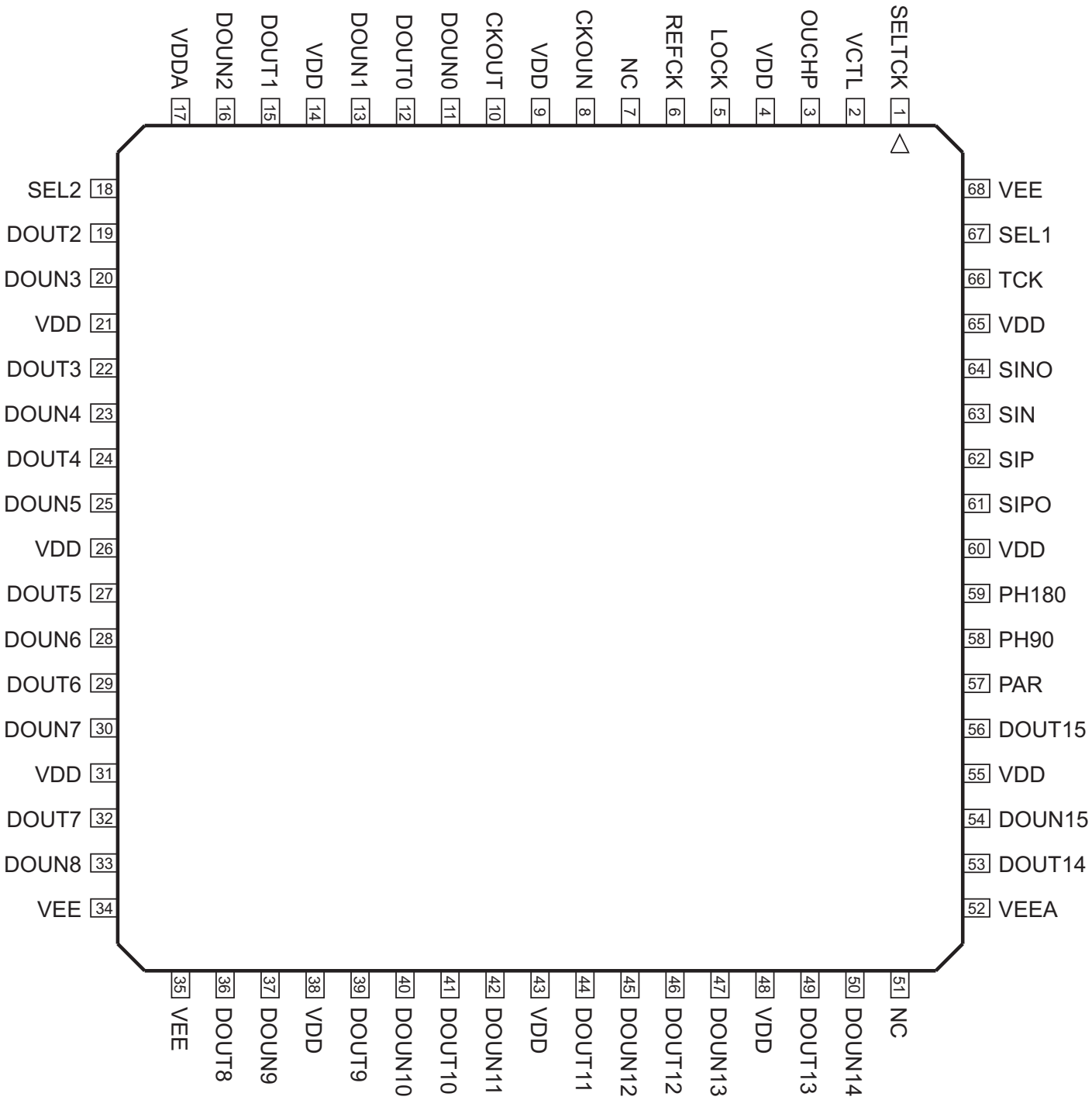


Figure 5. *Package Pinout, 68 pin - Top View*

Maximum Ratings

These are the limits beyond which the component may be damaged.
All voltages in the table are referred to VDD.
All currents in the table are defined positive out of the pin.

Symbol:	**Characteristic:**	**Conditions:**	**MIN.:**	**TYP.:**	**MAX.:**	**UNIT:**
V_{EE}, V_{EEA}	Negative Supply		-7		0	V
$V_{0\ ECL}$	Output Voltage	ECL	V_{EE} -0.5		0.5	V
I_{0} *ECL*	Output Current	ECL			40	mA
$I_{0\ MAX,\ CHPO}$	Output Current				0.251	mA
$V_{1\ ECL}$	Input Voltage	ECL	V_{EE} -0.5		0.5	V
$I_{1\ ECL}$	Input Current	ECL	-1.0		1.0	mA
T_0	Operating Temperature	Channel	-55		+150	°C
T_S	Storage Temperature		-65		+165	°C

DC Characteristics

T_{CASE} = 0 °C to 85 °C, V_{EE} = -5.0 V
θ_{J-C} = 7°C/W, for 68-pin CQFP.

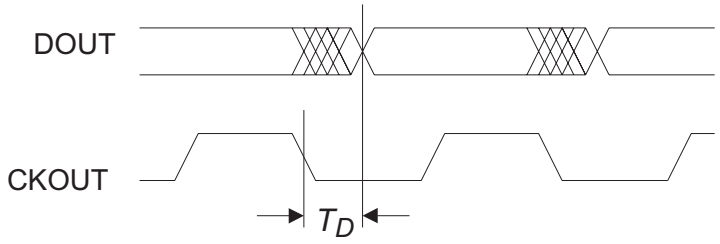
All voltages in the table are referred to VDD.
All input signal and power currents in the table are defined positive into the pin.
All output signal currents are defined positive out of the pin.

Symbol:	Characteristic:	Conditions:	MIN.:	TYP.:	MAX.:	UNIT.:
V_{EE}	Supply Voltage		-5.40		-4.5	V
I_{EE}	Supply Current				500	mA
P_{DISS}	Power Disspipation	Note 1			2.5	W
$V_{I\ SINX/SIPX}$	Data Input Swing, Differential	Note 2		20	30	mV
$V_{I\ SINX/SIPX}$	Data Input Swing, Single-ended	Note 2		20	30	mV
$V_{ICM\ SINX/SIPX}$	Data Common Mode Voltage		-2	-1.3	-1	V
$V_{IL\ REFCK}$	ECL REFCK Input LO Voltage	Note 3	V_{EE}		-1.5	V
$V_{IH\ REFCK}$	ECL REFCK Input HI Voltage	Note 3	-1.1		0	V
$V_{IL\ SEL1/2}$	ECL Set-up Inputs LO Voltage		V_{EE}		-1.5	V
$V_{IH\ SEL1/2}$	ECL Set-up Inputs HI Voltage					
$I_{IH\ ECL}$	ECL Input HI Current	$V_{IH\ MAX}$			100	µA
$I_{IL\ ECL}$	ECL Input LO Current	$V_{IL\ MIN}$			100	µA
$V_{OH\ ECL}$	ECL Output HI Voltage	Note 3, 4	-1.0		-0.5	V
$V_{OL\ ECL}$	ECL Output LO Voltage	Note 3, 4	V_{TT}		-1.6	V
$I_{OH\ ECL}$	ECL Output HI Current	Note 5	20	23	30	mA
$I_{OL\ ECL}$	ECL Output LO Current	Note 5	-2	5	8	mA
V_{VCTL}	VCO Control Voltage	I_{VCTL} < 30 µA	V_{EE}		-1	V
$I_{OH\ CHP}$	OUCHP Source Current (DC Steady)	Note 6		100		µA
$I_{OL\ CHP}$	OUCHP Sink Current (DC Steady)	Note 6		100		µA

Note 1: V_{EE} = -5.0 V
Note 2: AC-coupled, p-p voltage for differential coupling, BER 10^{-12}.
Data eye diagram in accordance with ITU G.957, 2^{23} - 1 PRBS, terminated via loop through 50 Ω.
Note 3: V_{TT} = -2.0 V ±5 %
Note 4: R_{LOAD} = 50 Ω to V_{TT}
Note 5: Not tested, consistent with V_{OH} and V_{OL} tests.
Note 6: Output terminated to -2.5 V during test.

AC Characteristics

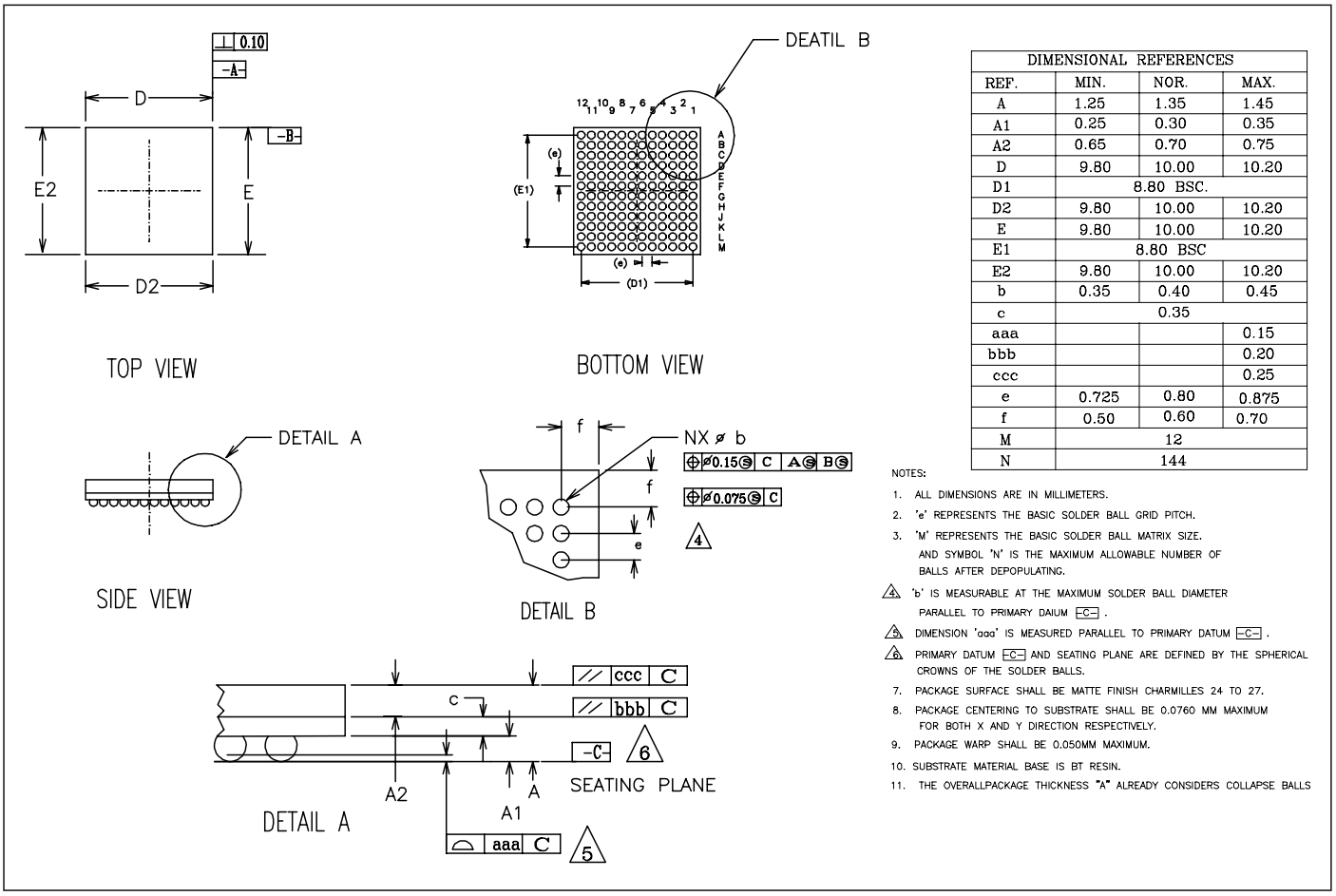
T_{CASE} = 0° to 85°C, V_{EE} = -5.4 V to -4.75 V.



Symbol:	Characteristic:	Conditions:	MIN.:	TYP.:	MAX.:	UNIT:
J_{TOL}	Jitter Tolerance	2 Hz < F <100 kHz (Note 1) 1 MHz < F <5 MHz (Note 1)	1.5 0.15	>2 >0.35		$UI_{16, PP}$ $UI_{16, PP}$
J_{TRF}	Jitter Transfer	12 kHz < F <2 MHz (Note 2)		0.08	0.1	dB
J_{CLK}	Output Clock Intrinsic Jitter	5 kHz < F < 20 MHz (Note 3) 1 MHz < F < 20 MHz (Note 3)			0.125 0.05	UI_1 UI_1
T_A	Aquisition time	2^{23}-1 PRBS		50	500	µs
L_{CID}	Consecutive Identical Digits	No. bits with no transitions	400	1000		bits
D_C	Input Clock / REFXI frequency deviation	Note 4	-200		200	ppm
$C_{DUTY\ REFCK}$	REFCK clock duty cycle	$V_{Thresh.}$ = -1.3 V	40		60	%
$C_{DUTY\ CKOUT}$	Output clock duty cycle	$V_{Thresh.}$ = -1.3 V, 25 Ω to -2 V	45		55	%
$T_{TLH\ CLOCK}$	CKOUT/ CKOUN rise time	20 – 80 %, 25 Ω to -2 V		350	700	ps
$T_{THL\ CLOCK}$	CKOUT/ CKOUN fall time	80 – 20 %, 25 Ω to -2 V		350	700	ps
$T_{TLH\ DATA}$	Output data rise time	20 – 80 %, 50 Ω to -2 V		350	700	ps
$T_{THL\ DATA}$	Output data fall time	80 – 20 %, 50 Ω to -2 V		350	700	ps
T_D	DOUT from CKOUT	*See figure above*		275		ps

Note 1: 1 UI_{16} = 0.40 ns; Data Pattern 2^{23}-1 PRBS.
Note 2: Data Pattern 2^{23}-1 PRBS. Through careful filter design, loop peaking may be controlled which is the major contribute to Jitter Transfer.
Note 3: In the absence of input jitter, the intrinsic jitter at CKOUT as measured over a 60 seconds interval shall not exceed these limits (1 UI_1 = 6.43 ns).
Note 4: Max. deviation between reference clock input and divided VCO clock when in lock.

Package Outline



DIMENSIONAL REFERENCES			
REF.	MIN.	NOR.	MAX.
A	1.25	1.35	1.45
A1	0.25	0.30	0.35
A2	0.65	0.70	0.75
D	9.80	10.00	10.20
D1		8.80 BSC.	
D2	9.80	10.00	10.20
E	9.80	10.00	10.20
E1		8.80 BSC	
E2	9.80	10.00	10.20
b	0.35	0.40	0.45
c		0.35	
aaa			0.15
bbb			0.20
ccc			0.25
e	0.725	0.80	0.875
f	0.50	0.60	0.70
M		12	
N		144	

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. 'e' REPRESENTS THE BASIC SOLDER BALL GRID PITCH.
3. 'M' REPRESENTS THE BASIC SOLDER BALL MATRIX SIZE. AND SYMBOL 'N' IS THE MAXIMUM ALLOWABLE NUMBER OF BALLS AFTER DEPOPULATING.
4. 'b' IS MEASURABLE AT THE MAXIMUM SOLDER BALL DIAMETER PARALLEL TO PRIMARY DAIUM -C- .
5. DIMENSION 'aaa' IS MEASURED PARALLEL TO PRIMARY DATUM -C- .
6. PRIMARY DATUM -C- AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
7. PACKAGE SURFACE SHALL BE MATTE FINISH CHARMILLES 24 TO 27.
8. PACKAGE CENTERING TO SUBSTRATE SHALL BE 0.0760 MM MAXIMUM FOR BOTH X AND Y DIRECTION RESPECTIVELY.
9. PACKAGE WARP SHALL BE 0.050MM MAXIMUM.
10. SUBSTRATE MATERIAL BASE IS BT RESIN.
11. THE OVERALLPACKAGE THICKNESS "A" ALREADY CONSIDERS COLLAPSE BALLS

Figure 6. *Package 144 fpBGA*

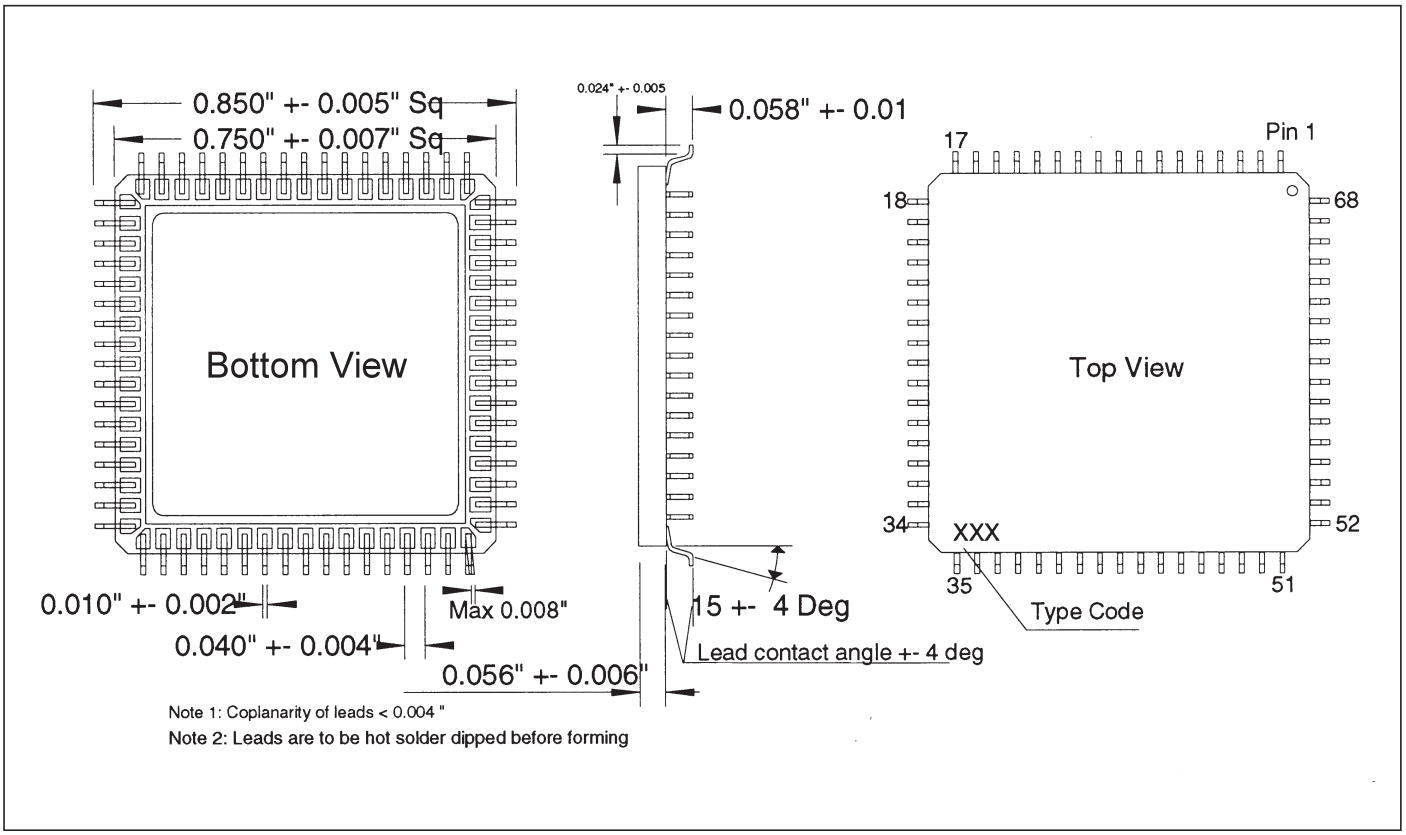


Figure 7. *Package 68 pin*

Ordering Information

Please order as specified below:

Product Name:	Package Type:	Case Temperature Range:	Options:
GD16506-144EA	144 leads fpBGA	0..85 °C	
GD16506-68BA	68 pin MLC	0..85 °C	

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