16-BIT EVEN/ODD PARITY GENERATOR/CHECKER

FEATURES

- **Word-length easily expanded by cascading**
- **Generates either even or odd parity for 16-data bits**
- **Output capability: standard**
- **I_{CC} category: MSI**

GENERAL DESCRIPTION

The 74HC/HCT7080 are high-speed Si-gate CMOS devices. They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT7080 are 16-bit parity generators or checkers commonly used to detect errors in high-speed data transmission or data retrieval systems.

The even and odd parity output is available for generating or checking even/odd parity up to 16-bits.

The even/odd parity output ($E/\overline{O}$) is HIGH when an even number of data inputs (I_0 to I_{15}) are HIGH and the cascade/even-odd-changing input ($\overline{X}$) is HIGH.

Expansion to larger word sizes is accomplished by connecting the even/odd parity output ($E/\overline{O}$) to the cascade/even-odd-changing input ($\overline{X}$) of the final stage.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay I_n to $E/\overline{O}$ $\overline{X}$ to $E/\overline{O}$	C_L = 15 pF V_{CC} = 5 V	29 12	32 15	ns ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	24	25	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

20-lead DIL; plastic (SOT146).
20-lead mini-pack; plastic (SO20; SOT163A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	$\overline{X}$	cascade/even-odd-changing input
2, 3, 4, 5, 6, 7, 8, 9, 11, 12, 13, 14, 15, 16, 17, 18	I_0 to I_{15}	data inputs
10	GND	ground (0 V)
19	$E/\overline{O}$	even/odd parity output
20	V_{CC}	positive supply voltage

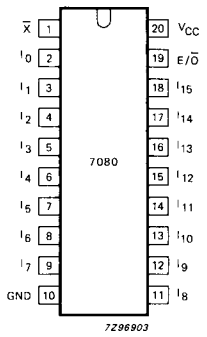

Fig. 1 Pin configuration.

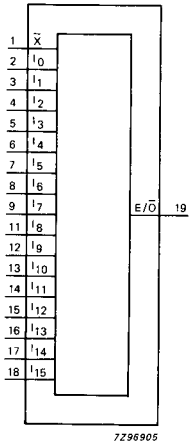

Fig. 2 Logic symbol.

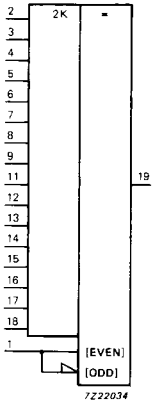

Fig. 3 IEC logic symbol.

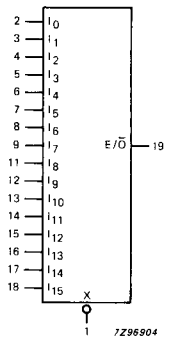

Fig. 4 Functional diagram.

FUNCTION TABLE

INPUTS		OUTPUTS
I_n	$\overline{X}$	E/$\overline{O}$
Σ = E	H	H
	L	L
$\Sigma \neq$ E	H	L
	L	H

H = HIGH voltage level
L = LOW voltage level
E = even

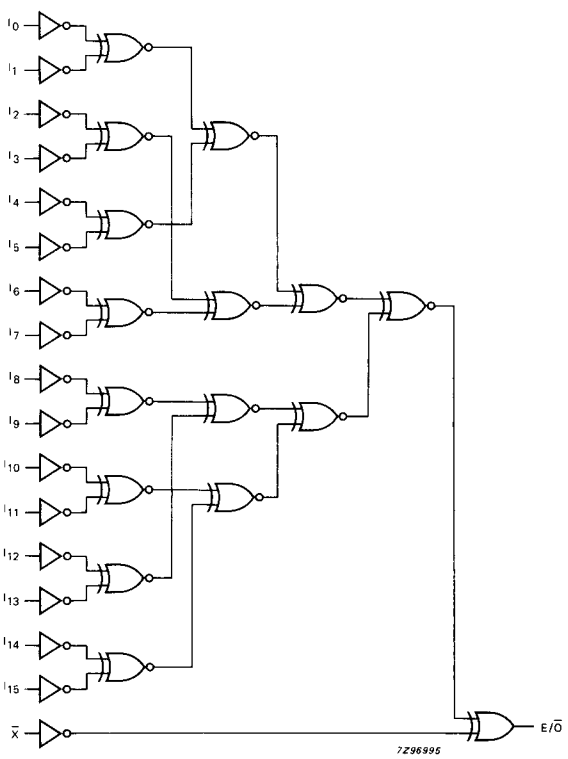

Fig. 5 Logic diagram.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay I_n to E/$\overline{O}$		91 33 26	280 56 48		350 70 60		420 84 71	ns	2.0 4.5 6.0	Fig. 7
t_{PHL}/t_{PLH}	propagation delay $\overline{X}$ to E/$\overline{O}$		41 15 12	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 6
t_{THL}/t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Figs 6 and 7

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications.
To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
I_n	1.0
$\overline{X}$	1.0

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay I_n to E/$\overline{O}$		37	63		79		95	ns	4.5	Fig. 7
t_{PHL}/t_{PLH}	propagation delay $\overline{X}$ to E/$\overline{O}$		18	32		40		48	ns	4.5	Fig. 6
t_{THL}/t_{TLH}	output transition time		7	15		19		22	ns	4.5	Figs 6 and 7

AC WAVEFORMS

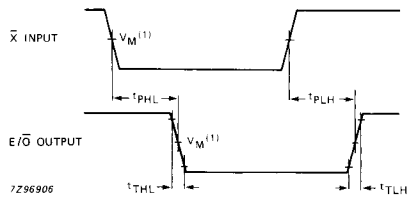

Fig. 6 Waveforms showing the cascade/even-odd-changing input ($\overline{X}$) to the even/odd parity output (E/$\overline{O}$) propagation delays and the output transition times.

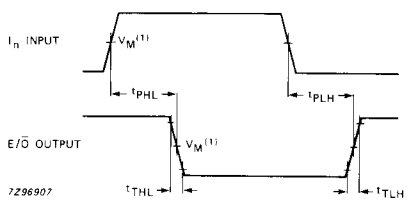

Fig. 7 Waveforms showing the data inputs (I_n) to the even/odd parity output (E/$\overline{O}$) propagation delays and the output transition times.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

TEST CIRCUIT AND WAVEFORMS

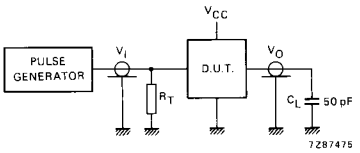

Fig. 8 Test circuit for measuring AC performance.

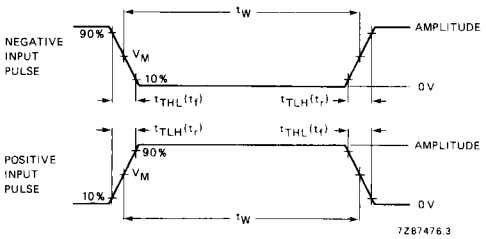

Fig. 9 Input pulse definitions.

Definitions for Figs 8 and 9:

C_L = load capacitance including jig and probe capacitance (see AC CHARACTERISTICS for values).

R_T = termination resistance should be equal to the output impedance Z_O of the pulse generator.

FAMILY	AMPLITUDE	V_M	t_r; t_f	
			f_{max}; PULSE WIDTH	OTHER
74HC	V_{CC}	50%	< 2 ns	6 ns
74HCT	3.0 V	1.3 V	< 2 ns	6 ns