

32/36-bit Data Bus **Dynamic RAM Card**

MF14M1-L1XATXX
 MF14M1-L2XATXX
 MF18M1-L1XATXX
 MF18M1-L2XATXX

Connector Type

Two-piece 88-pin

DESCRIPTION

These DRAM CARDS are developed based on JEIDA DRAM CARD GUIDELINE Ver. 2.0.

These cards are made using industry standard 1 M × 4 and 1 M × 1 Dynamic RAM and interface IC's in TSOP.

FEATURES

- All inputs except RAS inputs are buffered.
- Standard card size : 54mm (W) × 85.6mm (L) × 3.3mm (T)
- 88pin 2 piece connector type.
- RAS only refresh mode, CAS before RAS refresh mode and Page mode functions are available.
- Extended refresh is available. (128ms/1024cycle)

APPLICATIONS

Main/expansion memory unit for Personal Computer, Laser-Printer, FAX etc.

PRODUCT LIST

Product No.	Type name	Item	Memory capacity	Data Bus width (bits)	Access time (trAC) (ns)	Connector type	Number of pins	Outline drawing
No. 1	MF14M1-L17ATXX		4 MB	32	70	Two-piece	88	88P-001
No. 2	MF14M1-L18ATXX			(without parity)	80			
No. 3	MF14M1-L27ATXX			36	70			
No. 4	MF14M1-L28ATXX			(with parity)	80			
No. 5	MF18M1-L17ATXX		8 MB	32	70			
No. 6	MF18M1-L18ATXX			(without parity)	80			
No. 7	MF18M1-L27ATXX			36	70			
No. 8	MF18M1-L28ATXX			(with parity)	80			

DYNAMIC RAM CARDS

PIN ASSIGNMENT

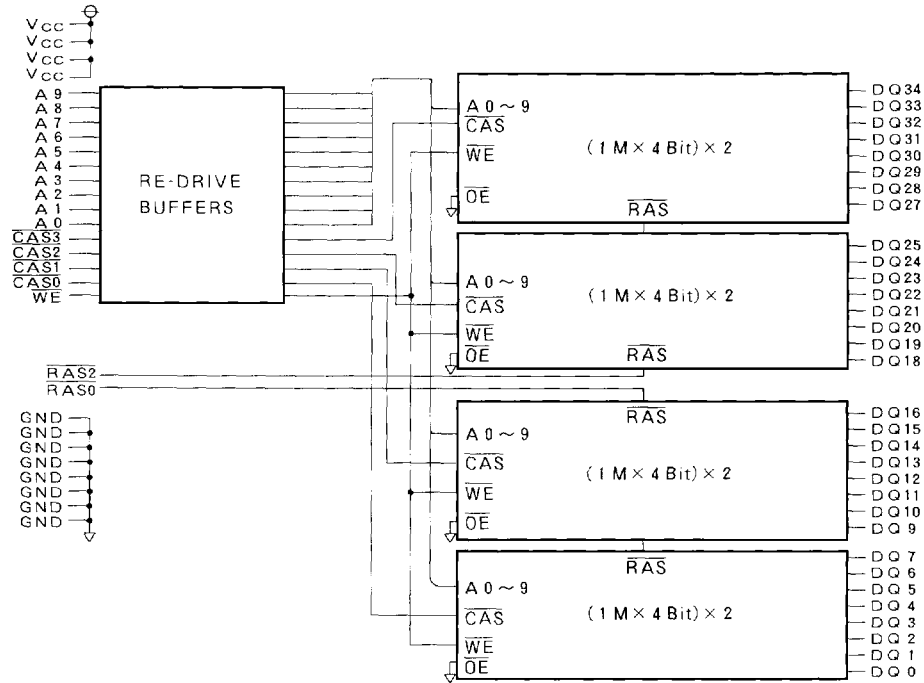
Pin No.	Symbol	Function	Pin No.	Symbol	Function
1	GND	Ground	45	GND	Ground
2	DQ 0	Data I/O	46	DQ 18	Data I/O
3	DQ 1		47	DQ 19	
4	DQ 2		48	DQ 20	
5	DQ 3		49	DQ 21	
6	DQ 4		50	DQ 22	
7	DQ 5		51	DQ 23	
8	DQ 6		52	DQ 24	
9	Vcc	Power supply voltage	53	DQ 25	Data I/O (NC for No. 1, 2, 5, 6)
10	DQ 7	Data I/O	54	DQ 26	
11	NC	No connection	55	NC	No connection
12	DQ 8	Data I/O (NC for No. 1, 2, 5, 6)	56	GND	Ground
13	A 0	Address input	57	A 1	Address input
14	A 2		58	A 3	
15	Vcc	Power supply voltage	59	A 5	
16	A 4	Address input	60	A 7	
17	NC	No connection	61	A 9	No connection
18	A 6	Address input	62	NC	
19	A 8		63	GND	Ground
20	NC	No connection	64	NC	No connection
21	NC		65	RAS 1	Row address strobe 1 (NC for No. 1, 2, 3, 4)
22	RAS 0	Row address strobe 0	66	CAS 2	Column address strobe 2
23	CAS 0	Column address strobe 0	67	GND	Ground
24	CAS 1	Column address strobe 1	68	CAS 3	Column address strobe 3
25	NC	No connection	69	RAS 3	Row address strobe 3 (NC for No. 1, 2, 3, 4)
26	RAS 2	Row address strobe 2	70	WE	Write enable
27	Vcc	Power supply voltage	71	PD 1	Presence detect 1
28	PD 2	Presence detect 2	72	PD 3	Presence detect 3
29	PD 4	Presence detect 4	73	GND	Ground
30	PD 6	Presence detect 6	74	PD 5	Presence detect 5
31	NC	No connection	75	PD 7	Presence detect 7
32	NC		76	PD 8	Presence detect 8
33	DQ 17	Data I/O (NC for No. 1, 2, 5, 6)	77	NC	No connection
34	DQ 9	Data I/O	78	NC	
35	NC	No connection	79	DQ 35	Data I/O (NC for No. 1, 2, 5, 6)
36	DQ 10	Data I/O	80	DQ 27	
37	Vcc	Power supply voltage	81	DQ 28	Data I/O
38	DQ 11	Data I/O	82	DQ 29	
39	DQ 12		83	DQ 30	
40	DQ 13		84	DQ 31	
41	DQ 14		85	DQ 32	
42	DQ 15		86	DQ 33	
43	DQ 16		87	DQ 34	
44	GND	Ground	88	GND	Ground

PD Pin Table

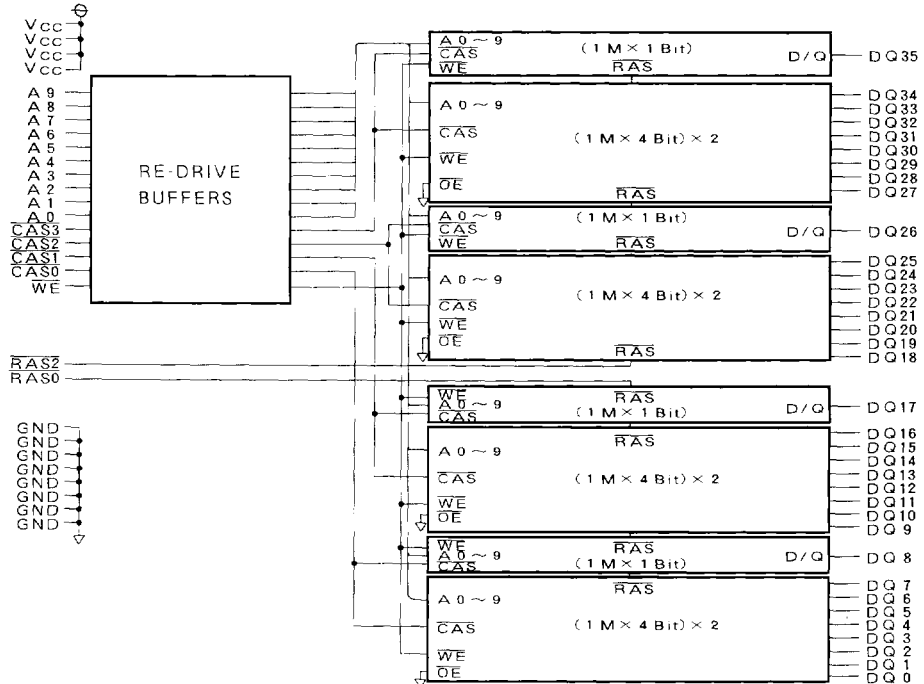
Product No.	PD 1	PD 2	PD 3	PD 4	PD 5	PD 6	PD 7	PD 8
No. 1, No. 3	GND	NC	GND	GND	NC	GND	NC	NC
No. 2, No. 4	GND	NC	GND	GND	NC	NC	GND	NC
No. 5, No. 7	GND	NC	GND	GND	GND	GND	NC	NC
No. 6, No. 8	GND	NC	GND	GND	GND	NC	GND	NC

DYNAMIC RAM CARDS

BLOCK DIAGRAM (No.1, 2)

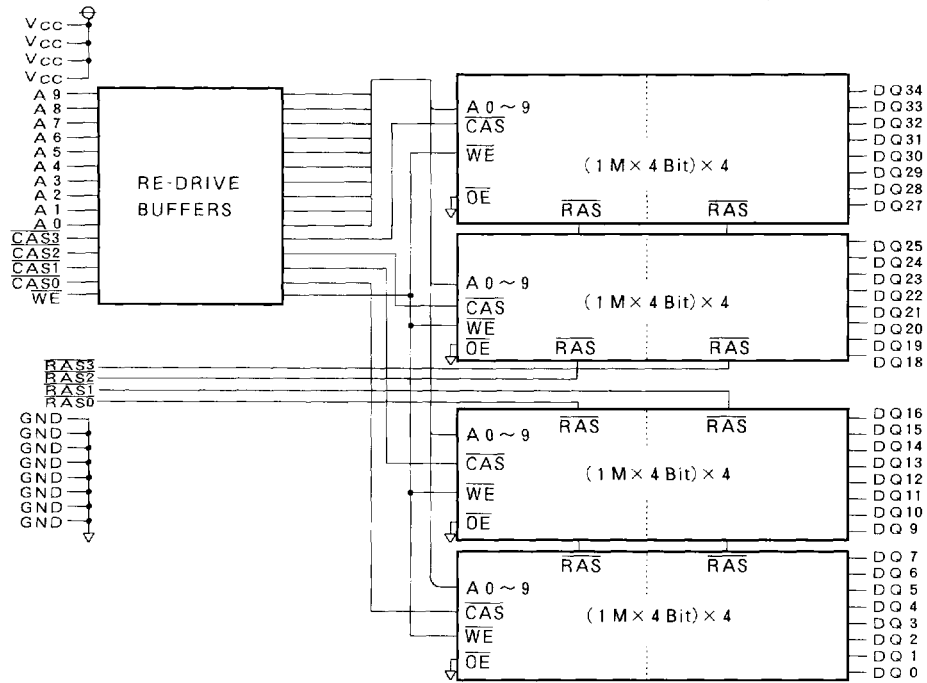


BLOCK DIAGRAM (No.3, 4)

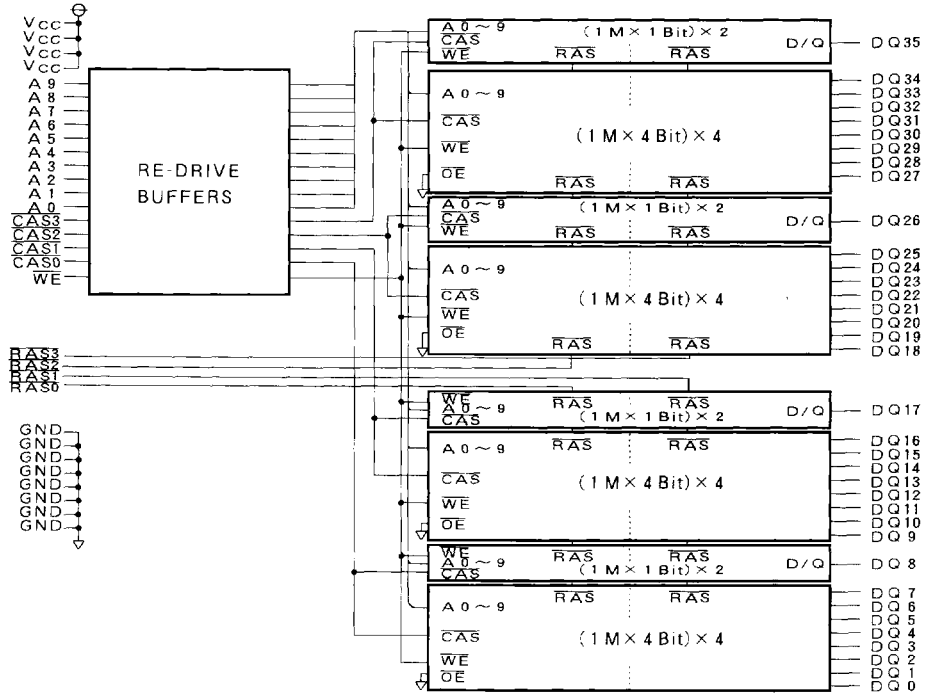


DYNAMIC RAM CARDS

BLOCK DIAGRAM (No.5, 6)



BLOCK DIAGRAM (No.7, 8)



DYNAMIC RAM CARDS

FUNCTION TABLE

Operation	input					input/output		Refresh	Note
	$\overline{\text{RAS}}$	$\overline{\text{CAS}}$	$\overline{\text{WE}}$	Row Address	Column Address	input	output		
Read	ACT	ACT	NAC	APD	APD	OPN	VLD	YES	Page mode identical
Early write	ACT	ACT	ACT	APD	APD	VLD	OPN	YES	
$\overline{\text{RAS}}$ only refresh	ACT	NAC	DNC	APD	DNC	DNC	OPN	YES	
CAS before $\overline{\text{RAS}}$ refresh	ACT	ACT	NAC	DNC	DNC	DNC	OPN	YES	
Standby	NAC	DNC	DNC	DNC	DNC	DNC	OPN	NO	

Note 1 : ACT : active, NAC : nonactive, DNC : don't care, VLD : valid, APD : applied, OPN : open
Don't be active more than two $\overline{\text{RAS}}$ s at the same time.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to GND	-0.5~7	V
V_I	Input voltage		-0.5~ $V_{CC}+0.5$ (7V max.)	V
V_O	Output voltage		-0.5~7	V
I_O	Output current	$T_a=25^\circ\text{C}$	50	mA
P_d	Power dissipation		8	W
T_{opr}	Operating temperature		0~55	$^\circ\text{C}$
T_{stg}	Storage temperature		-40~80	$^\circ\text{C}$

RECOMMENDED OPERATING CONDITIONS ($T_a=0\sim55^\circ\text{C}$, unless otherwise noted): (Note 2)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
V_{CC}	Supply voltage	4.75	5	5.25	V
GND	Supply voltage	0	0	0	V
V_{IL}	Low input voltage	0		0.8	V
V_{IH}	High input voltage	$0.7 \times V_{CC}$		V_{CC}	V

Note 2 : With respect to GND

DYNAMIC RAM CARDS

ELECTRICAL CHARACTERISTICS ($T_a = 0 \sim 55^\circ\text{C}$, $V_{CC} = 5\text{V} \pm 5\%$, $\text{GND} = 0\text{V}$) : (Note 3)

Symbol	Parameter	Test condition	Limits															Unit
			Min.				Typ.	Max.										
			No. 1, No. 2	No. 3, No. 4	No. 5, No. 6	No. 7, No. 8		No. 1	No. 2	No. 3	No. 4	No. 5	No. 6	No. 7	No. 8			
V _{OH}	High output voltage	I _{OH} = - 5 mA	2.4					V _{CC}								V		
V _{OL}	Low output voltage	I _{OL} = 4.2 mA	0					0.4								V		
I _{OZ}	Off-stage output current	0 V ≤ V _{OUT} ≤ V _{CC}	-10	-10	-20	-20		10	10	10	10	20	20	20	20	μA		
I _I	Input current	0 V ≤ V _{IN} ≤ V _{CC} Other input pins = 0 V	-40	-60	-40	-60		40	40	60	60	40	40	60	60	μA		
I _{CC1(AV)}	Average supply current from V _{CC} , operating (Note 4, 5)	RAS, CAS cycling trc = twc = min, output open						800	700	1120	980	820	730	1150	1010	mA		
I _{CC2(AV)}	Supply current from V _{CC} , standby	RAS = CAS = V _{IH} , output open						20	20	28	28	36	36	52	52	mA		
		RAS = CAS ≥ V _{CC} - 0.2V, other input pins ≥ V _{CC} - 0.2V or ≤ 0.2V, output open						5	5	6	6	9	9	10	10			
I _{CC3(AV)}	Average supply current from V _{CC} , refreshing (Note 4)	RAS cycling, CAS = V _{IH} trc = min, output open						800	700	1120	980	820	730	1150	1010	mA		
I _{CC4(AV)}	Average supply current from V _{CC} , Page-Mode (Note 4, 5)	RAS = V _{IL} , CAS cycling trc = min, output open						960	900	1240	1140	980	930	1270	1170	mA		
I _{CC6(AV)}	Average supply current from V _{CC} , CAS before RAS refresh mode (Note 4)	CAS before RAS refresh cycling trc = min, output open						720	620	1040	900	740	650	1070	930	mA		

Note 3 : Current flowing into a CARD is positive, out is negative.

4 : $I_{CC1(AV)}$, $I_{CC3(AV)}$, $I_{CC4(AV)}$ and $I_{CC6(AV)}$ are dependent on cycle rate. Specified values are obtained at the fastest cycle rate.

5 : $I_{CC1(AV)}$ and $I_{CC4(AV)}$ are dependent on output loading. Specified values are obtained with the outputs open.

DYNAMIC RAM CARDS

SWITCHING CHARACTERISTICS ($T_a = 0 \sim 55^\circ\text{C}$, $V_{CC} = 5\text{ V} \pm 5\%$, $\text{GND} = 0\text{ V}$): (Note 6)

Symbol	Parameter	Limits				Unit
		No. 2, No. 4, No. 6, No. 8		No. 1, No. 3, No. 5, No. 7		
		Min.	Max.	Min.	Max.	
tCAC	Access time from CAS (Note7, 8)		30		27	ns
tRAC	Access time from RAS (Note7, 9)		80		70	ns
tCAA	Column Address access time (Note7, 10)		50		45	ns
tOFF	Output disable time after CAS high (Note11)	0	30	0	25	ns

Note 6 : An initial pause of 500 μsec is required after power-up followed by any 8 $\overline{\text{RAS}}$ or $\overline{\text{RAS}}/\overline{\text{CAS}}$ cycles before proper device operation is achieved. Note that $\overline{\text{RAS}}$ may be cycled during the initial pause. And any 8 $\overline{\text{RAS}}$ or $\overline{\text{RAS}}/\overline{\text{CAS}}$ cycles are required after prolonged periods of $\overline{\text{RAS}}$ inactivity before proper device operation is achieved.

7 : Measured with a load circuit equivalent to 2 TTL loads and 100pF.

8 : Assume that $t_{RCD} \geq t_{RCD(max)}$ and $t_{ASC} \geq t_{ASC(max)}$.

9 : Assume that $t_{RCD} \leq t_{RCD(max)}$ and $t_{RAD} \leq t_{RAD(max)}$.

10 : Assume that $t_{RAD} \geq t_{RAD(max)}$ and $t_{ASC} \leq t_{ASC(max)}$.

11 : $t_{OFF(max)}$ define the time at which the output achieves the high impedance state ($|I_{out}| \leq 10\text{ }\mu\text{A}$ or $20\text{ }\mu\text{A}$) and are not reference to $V_{OH(min)}$ or $V_{OL(max)}$.

TIMING REQUIREMENTS ($T_a = 0 \sim 55^\circ\text{C}$, $V_{CC} = 5\text{ V} \pm 5\%$, $\text{GND} = 0\text{ V}$): (Note 12, 13)

Symbol	Parameter	Limits				Unit
		No. 2, No. 4, No. 6, No. 8		No. 1, No. 3, No. 5, No. 7		
		Min.	Max.	Min.	Max.	
tREF	Refresh cycle time (1024 cycles)		128		128	ms
tRP	RAS high pulse width	70		60		ns
tRCD	Delay time, RAS low to CAS low (Note14)	20	50	20	43	ns
tCRP	Delay time, CAS high to RAS low (Note15)	20		20		ns
tRPC	Precharge to CAS active time	0		0		ns
tCPN	CAS high pulse width	10		10		ns
tRAD	Column address delay time from RAS low (Note16)	15	30	15	25	ns
tASR	Row address setup time before RAS low	10		10		ns
tASC	Column address setup time before CAS low (Note17)	5	15	5	13	ns
tRAH	Row address hold time after RAS low	10		10		ns
tCAH	Column address hold time after CAS low	15		15		ns
tT	Transition time (Note18)	3	50	3	50	ns

Note 12 : The timing requirements are assumed $t_T = 5\text{ ns}$.

13 : $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals.

14 : $t_{RCD(max)}$ is specified as a reference point only. If t_{RCD} is greater than $t_{RCD(max)}$, access time is defined as t_{CAC} and t_{CAA} .

15 : t_{CRP} requirement is applicable for all $\overline{\text{RAS}}/\overline{\text{CAS}}$ cycles.

16 : $t_{RAD(max)}$ is specified as reference point only. If $t_{RAD} \geq t_{RAD(max)}$ and $t_{ASC} \leq t_{ASC(max)}$, access time is assumed by t_{CAA} for read cycle.

17 : $t_{ASC(max)}$ is specified as a reference point only of address access time.

18 : t_T is measured between $V_{IH(min)}$ and $V_{IL(max)}$.

DYNAMIC RAM CARDS

Read and Refresh Cycles

Symbol	Parameter	Limits				Unit
		No. 2, No. 4, No. 6, No. 8		No. 1, No. 3, No. 5, No. 7		
		Min.	Max.	Min.	Max.	
tRC	Read cycle time	160		140		ns
tRAS	RAS low pulse width	80	10000	70	10000	ns
tCAS	CAS low pulse width	20	10000	20	10000	ns
tCSH	CAS hold time after RAS low	80		70		ns
tRSH	RAS hold time after CAS low	30		30		ns
tRCS	Read Setup time before CAS low	5		5		ns
tRCH	Read hold time after CAS high	0		0		ns
tRRH	Read hold time after RAS high	10		10		ns

Write Cycle (Early Write)

Symbol	Parameter	Limits				Unit
		No. 2, No. 4, No. 6, No. 8		No. 1, No. 3, No. 5, No. 7		
		Min.	Max.	Min.	Max.	
tWC	Write cycle time	160		140		ns
tRAS	RAS low pulse width	80	10000	70	10000	ns
tCAS	CAS low pulse width	20	10000	20	10000	ns
tCSH	CAS hold time after RAS low	80		70		ns
tRSH	RAS hold time after CAS low	30		30		ns
twCS	Write Setup time before CAS low	5		5		ns
twCH	Write hold time after CAS low	15		15		ns
tDS	Data setup time	10		10		ns
tDH	Data hold time after CAS low	25		25		ns

Page Mode Cycle (Read, Early Write)

Symbol	Parameter	Limits				Unit
		No. 2, No. 4, No. 6, No. 8		No. 1, No. 3, No. 5, No. 7		
		Min.	Max.	Min.	Max.	
tPC	Read,Write cycle time	60		55		ns
tCP	CAS high pulse width(Note19)	10	20	10	18	ns
tRAS	RAS low pulse width	140	100000	125	100000	ns

Note 19 : tCP(max) is specified as a reference point only.

CAS before RAS Refresh Cycle (Note 20)

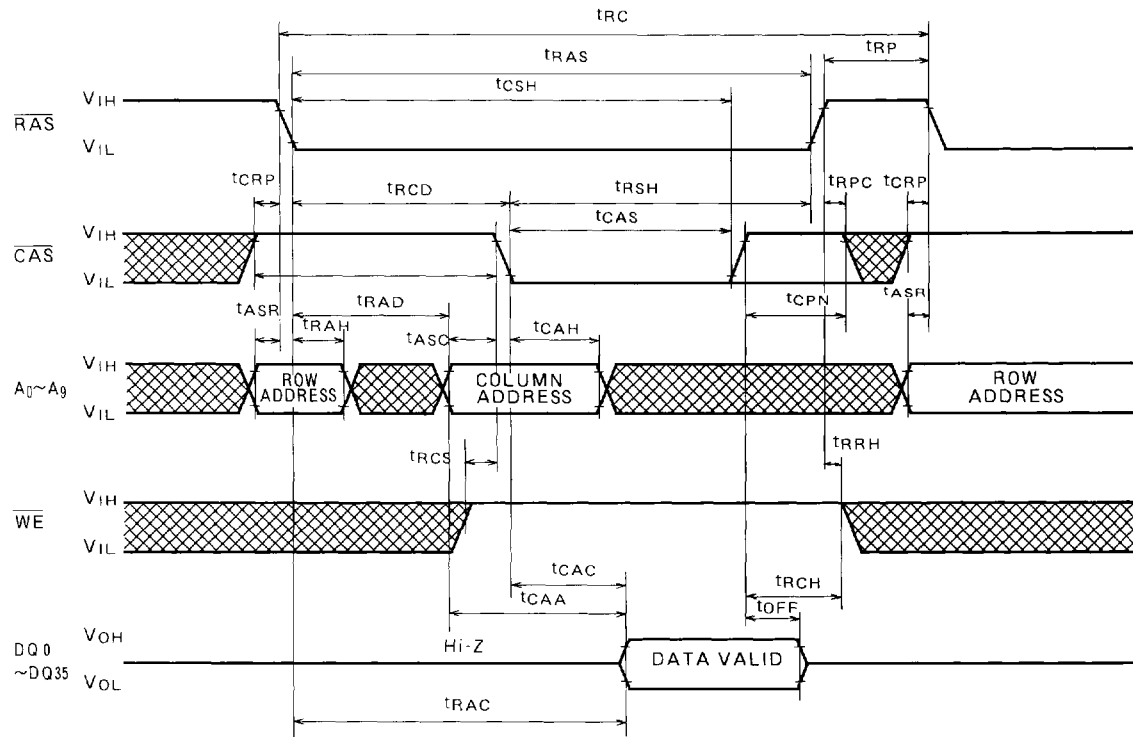
Symbol	Parameter	Limits		Unit
		Min.	Max.	
tCSR	CAS setup time for CAS before RAS refresh	20		ns
tCHR	CAS hold time for CAS before RAS refresh	15		ns

Note 20 : Eight or more CAS before RAS cycles are necessary for proper operation of CAS before RAS refresh mode.

DYNAMIC RAM CARDS

TIMING DIAGRAMS (Note 21)

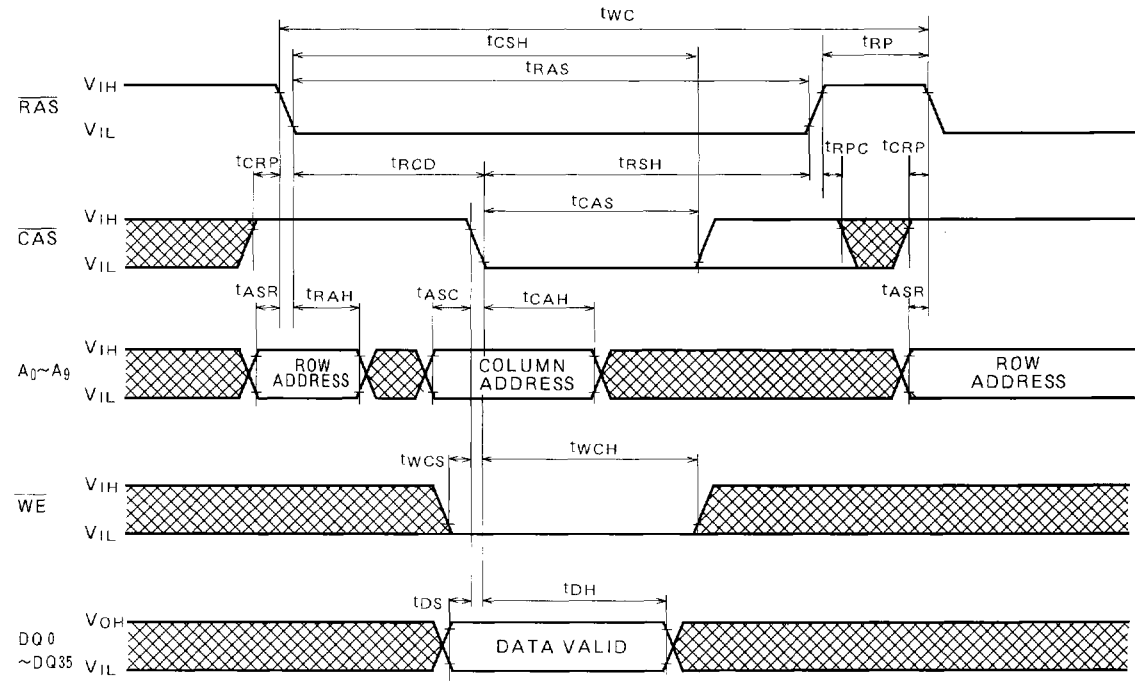
Read Cycle



Note 21 :  Indicates the don't care input.

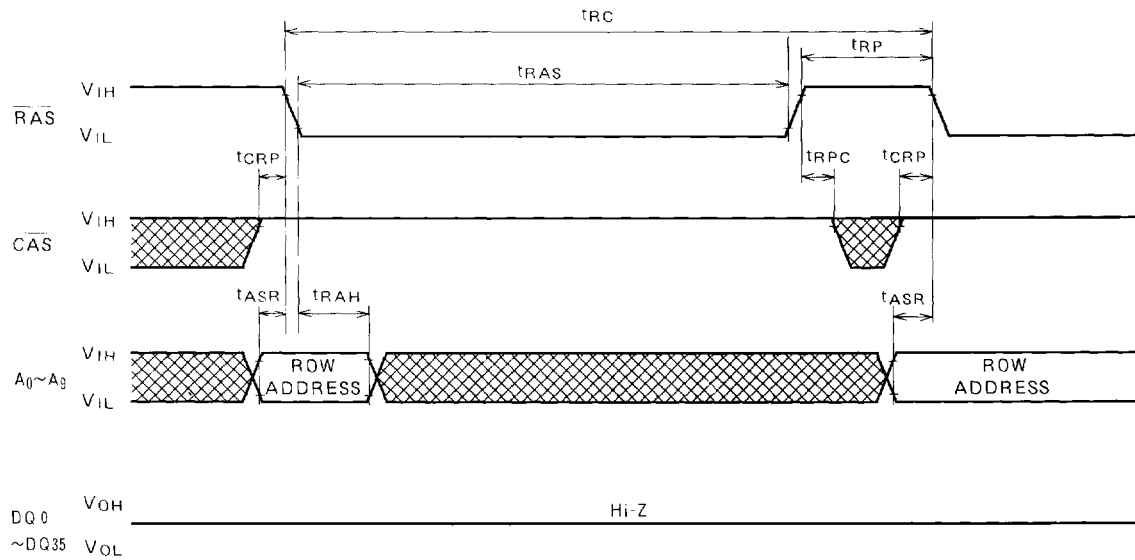
DYNAMIC RAM CARDS

Early Write Cycle

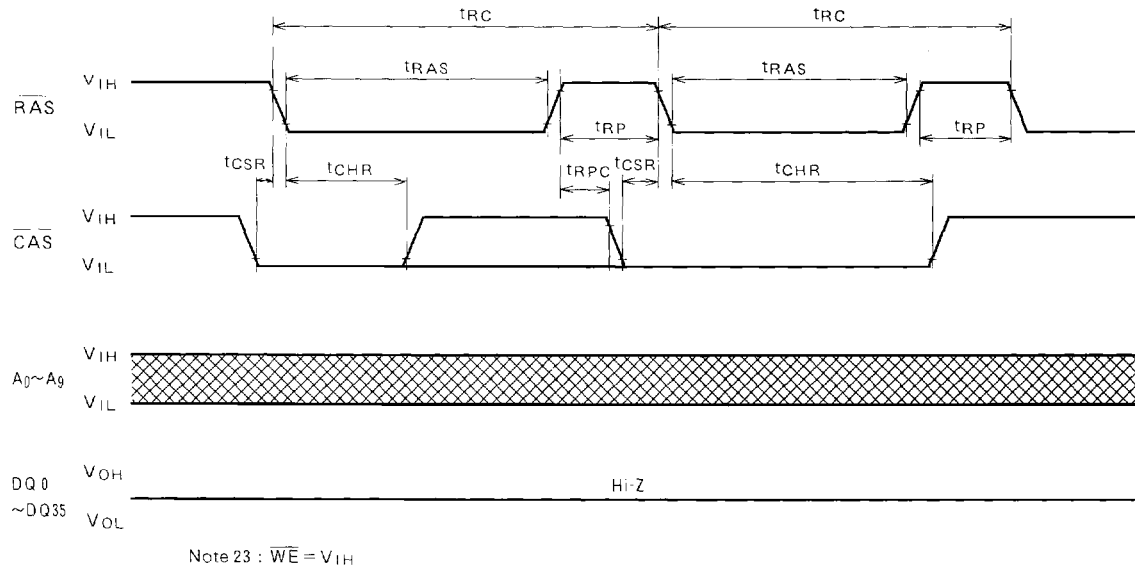


DYNAMIC RAM CARDS

$\overline{\text{RAS}}$ only Refresh Cycle (Note 22)

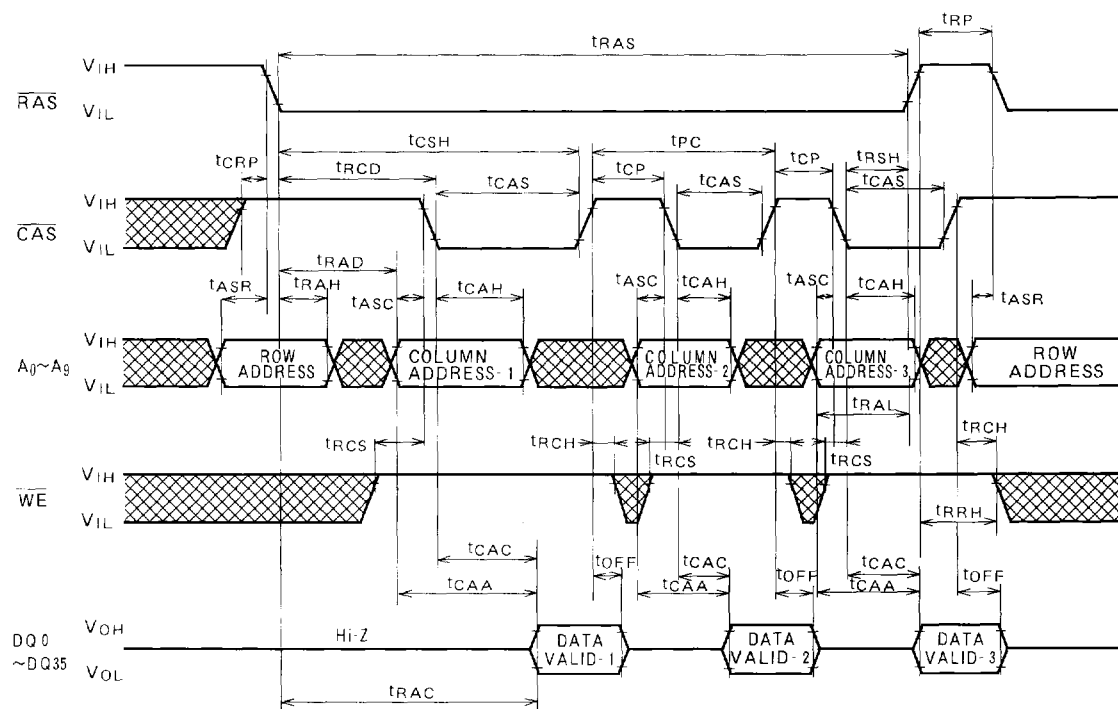


$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh Cycle (Note 23)



DYNAMIC RAM CARDS

Page-Mode Read Cycle



Page-Mode Early Write Cycle

