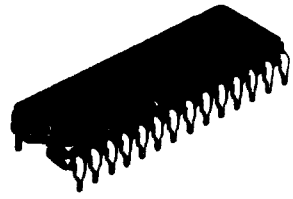
HM65256B Series

32768-word X 8-bit High Speed Pseudo Static RAM

■ FEATURES

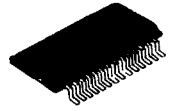
- Single 5V (±10%)
- High Speed
  Access Time
  $\overline{CE}$ Access Time 100/120/150/200ns
  Address Access Time 50/60/75/100ns
  (in Static Column Mode)
  Cycle Time
  Random Read/Write Cycle Time 160/190/235/310ns
  Static Column Mode Cycle Time 55/65/80/105ns
- Low Power
  175mW typ. Active.
- All inputs and outputs TTL compatible
- Static Column Mode Capability
- Non Multiplexed Address
- 256 Refresh Cycles (4ms)
- Refresh Functions
  Address Refresh
  Automatic Refresh
  Self Refresh

HM65256BP Series



(DP-28)

HM65256BFP Series

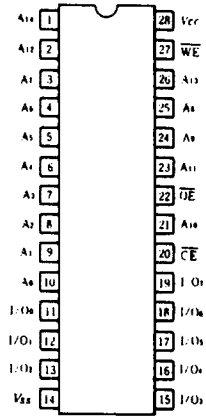


(FP-28DA)

■ ORDERING INFORMATION

Type No.	Access Time	Package
HM65256BP-10	100ns	600 mil 28 pin Plastic DIP
HM65256BP-12	120ns	
HM65256BP-15	150ns	
HM65256BP-20	200ns	
HM65256BLP-10	100ns	
HM65256BLP-12	120ns	
HM65256BLP-15	150ns	
HM65256BLP-20	200ns	
HM65256BFP-10T	100ns	28 pin Plastic SOP
HM65256BFP-12T	120ns	
HM65256BFP-15T	150ns	
HM65256BFP-20T	200ns	
HM65256BLFP-10T	100ns	
HM65256BLFP-12T	120ns	
HM65256BLFP-15T	150ns	
HM65256BLFP-20T	200ns	

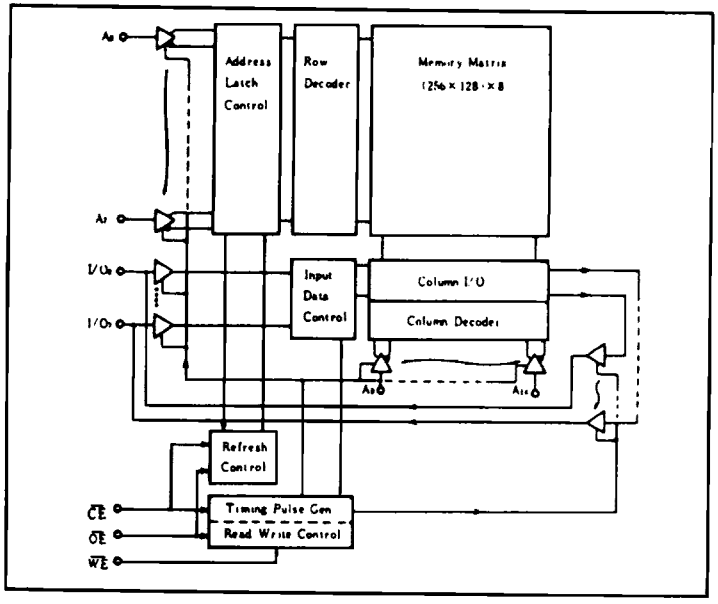
■ PIN ARRANGEMENT



(Top View)

4

■ BLOCK DIAGRAM



■ TRUTH TABLE

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O Pin	mode
L	L	H	Low Z	Read
L	×	L	High Z	Write
L	H	H	High Z	–
H	L	×	High Z	Refresh
H	H	×	High Z	Standby

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Terminal Voltage with Respect to V_{SS}	V_T	−1.0 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Storage Temperature Under Bias	T_{bias}	−10 to +85	°C

■ RECOMMENDED DC OPERATING CONDITIONS (T_a = 0 to +70°C)

Item	Symbol	min.	typ.	max.	unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input Voltage	V_{IH}	2.2	–	6.0	V
	V_{IL}	−0.5*1	–	0.8	V

Note) *1. V_{IL} min = −3.0V for pulse width ≦ 10ns.

■ DC ELECTRICAL CHARACTERISTICS (T_a = 0 to +70°C, V_{CC} = 5V ±10%)

Parameter	Symbol	Test Conditions	HM65256B Series			HM65256BL Series			Unit
			min.	typ.	max.	min.	typ.	max.	
Operating Power Supply Current	I_{CC1}	$I_{I/O}$ = 0mA, t_{cyc} = min.	–	35	65	–	35	65	mA
Standby Power Supply Current	I_{SB1}	$\overline{CE}$ = V_{IH}, $\overline{OE}$ = V_{IH}	–	1	2	–	1	2	mA
	I_{SB2}	$\overline{CE} \geq V_{CC}-0.2V$, $\overline{OE} \geq V_{CC}-0.2V$	–	–	–	–	0.05	0.1	mA
Operating Power Supply Current in Self Refresh Mode	I_{CC2}	$\overline{CE}$ = V_{IH}, $\overline{OE}$ = V_{IL}	–	1	2	–	0.6	1	mA
	I_{CC3}	$\overline{CE} \geq V_{CC}-0.2V$, $\overline{OE} \leq 0.2V$	–	–	–	–	50	100	µA
Input Leakage Current	I_{LI}	V_{CC} = 5.5V, Vin = V_{SS} to V_{CC}	–10	–	10	–10	–	10	µA
Output Leakage Current	I_{LO}	$\overline{OE}$ = V_{IH}, $V_{I/O}$ = V_{SS} to V_{CC}	–10	–	10	–10	–	10	µA
Output Voltage	V_{OL}	I_{OL} = 2.1 mA	–	–	0.4	–	–	0.4	V
	V_{OH}	I_{OH} = –1 mA	2.4	–	–	2.4	–	–	V

■ CAPACITANCE

Item	Symbol	Test Conditions	typ.	max.	Unit
Input Capacitance	Cin	Vin = 0V	–	5	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	–	7	pF

Note) This Parameter is sampled and not 100% tested.

■ AC CHARACTERISTICS (T_a = 0 to +70°C, V_{CC} = 5V ±10%)

- AC Test Conditions

Input Pulse Levels 2.4V, 0.4V
Input Rise and Fall Times 5ns
Timing Measurement Level 2.2V, 0.8V
Reference Level . . . . . V_{OH} = 2.0V, V_{OL} = 0.8V
Output Load . . . . . 1 TTL and 100pF (including scope and jig)

Item	Symbol	HM65256B-10		HM65256B-12		HM65256B-15		HM65256B-20		Unit
		min.	max.	min.	max.	min.	max.	min.	max.	
Random Read or Write Cycle Time	t_{RC}	160	–	190	–	235	–	310	–	ns
Static Column Mode Read or Write Cycle	t_{RSC}	55	–	65	–	80	–	105	–	ns
Chip Enable Access Time	t_{CEA}	–	100	–	120	–	150	–	200	ns
Address Access Time	t_{AA}	–	50	–	60	–	75	–	100	ns
Output Enable Access Time	t_{OEA}	–	40	–	50	–	60	–	75	ns
Chip Disable to Output in High Z	t_{CHZ}	–	25	–	25	–	30	–	35	ns
Chip Enable to Output in Low Z	t_{CLZ}	30	–	30	–	35	–	40	–	ns
Output Enable to Output in Low Z	t_{OLZ}	10	–	10	–	10	–	10	–	ns
Output Disable to Output in High Z	t_{OHZ}	–	25	–	25	–	30	–	35	ns
Chip Enable Pulse Width	t_{CE}	100n	4m	120n	4m	150n	4m	200n	4m	s
Chip Enable Precharge Time	t_P	50	–	60	–	75	–	100	–	ns
Address Set-up Time	t_{AS}	0	–	0	–	0	–	0	–	ns
Row Address Hold Time	t_{RAH}	20	–	20	–	25	–	30	–	ns
Column Address Hold Time	t_{CAH}	100	–	120	–	150	–	200	–	ns
Read Command Set-up Time	t_{RCS}	0	–	0	–	0	–	0	–	ns
Read Command Hold Time	t_{RCH}	0	–	0	–	0	–	0	–	ns
Output Enable Hold Time	t_{OHC}	0	–	0	–	0	–	0	–	ns
Output Enable to Chip Enable Delay Time	t_{OCD}	0	–	0	–	0	–	0	–	ns
Output Hold Time from Column Address	t_{OH}	5	–	5	–	5	–	10	–	ns
Write Command Pulse Width	t_{WP}	25	–	25	–	30	–	35	–	ns
Chip Enable to End of Write	t_{CW}	100	–	120	–	150	–	200	–	ns
Column Address Set-up Time	t_{ASW}	0	–	0	–	0	–	0	–	ns

(to be continued)

Item	Symbol	HM65256B-10		HM65256B-12		HM65256B-15		HM65256B-20		Unit
		min.	max.	min.	max.	min.	max.	min.	max.	
Column Address Hold Time after Write	t_{AHW}	0	–	0	–	0	–	0	–	ns
Data Valid to End of Write	t_{DW}	20	–	20	–	25	–	30	–	ns
Data In Hold Time for Write	t_{DH}	0	–	0	–	0	–	0	–	ns
Output Active from End of Write	t_{OW}	5	–	5	–	5	–	5	–	ns
Write to Output in High Z	t_{WHZ}	–	25	–	25	–	30	–	35	ns
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	3	50	ns
Refresh Command Delay Time	t_{RFD}	50	–	60	–	75	–	100	–	ns
Refresh Precharge Time	t_{FP}	30	–	30	–	30	–	30	–	ns
Refresh Command Pulse Width for Automatic Refresh	t_{FAP}	80	10000	80	10000	80	10000	80	10000	ns
Automatic Refresh Cycle Time	t_{FC}	160	–	190	–	235	–	310	–	ns
Refresh Command Pulse Width for Self Refresh	t_{FAS}	10000	–	10000	–	10000	–	10000	–	ns
Refresh Reset Time for Self Refresh	t_{FRS}	160	–	190	–	235	–	310	–	ns
Refresh Period	t_{REF}	–	4	–	4	–	4	–	4	ms

Notes:

(1) t_{CHZ}, t_{OHZ} and t_{WHZ} are defined as the time at which the output achieves the open circuit conditions.

(2) t_{CLZ}, t_{OLZ} and t_{OW} are sampled under the condition of t_T=5ns, and not 100% tested.

(3) A write occurs during the overlap of a low $\overline{CE}$ and low $\overline{WE}$.

(4) If $\overline{CE}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain in high impedance state.

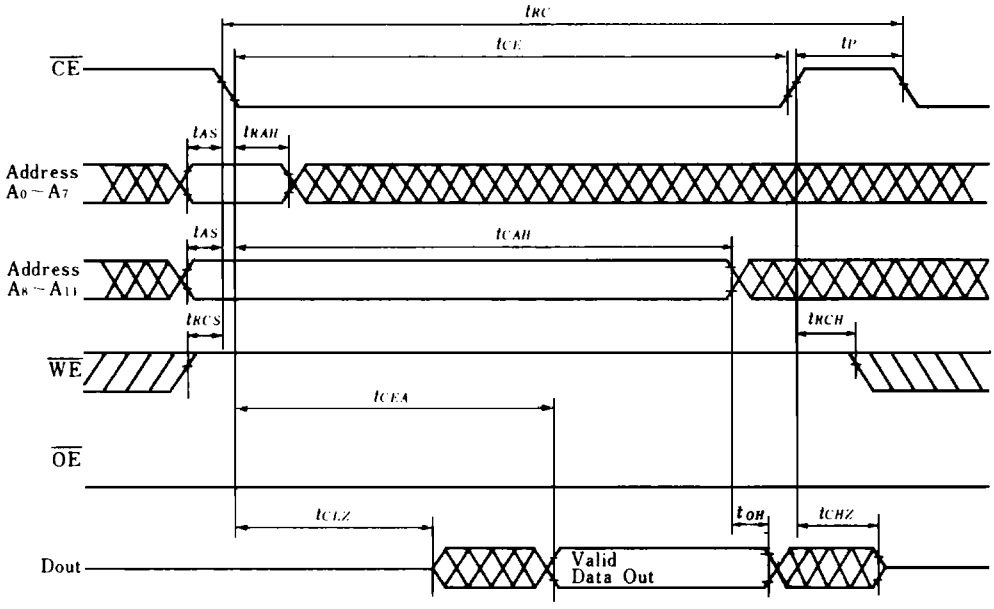
(5) If input signals of opposite phase to the outputs are applied in write cycle, $\overline{OE}$ or $\overline{WE}$ must disable output buffers prior to applying data to the device and data inputs must be floating prior to $\overline{OE}$ or $\overline{WE}$ turning on output buffers.

(6) V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.

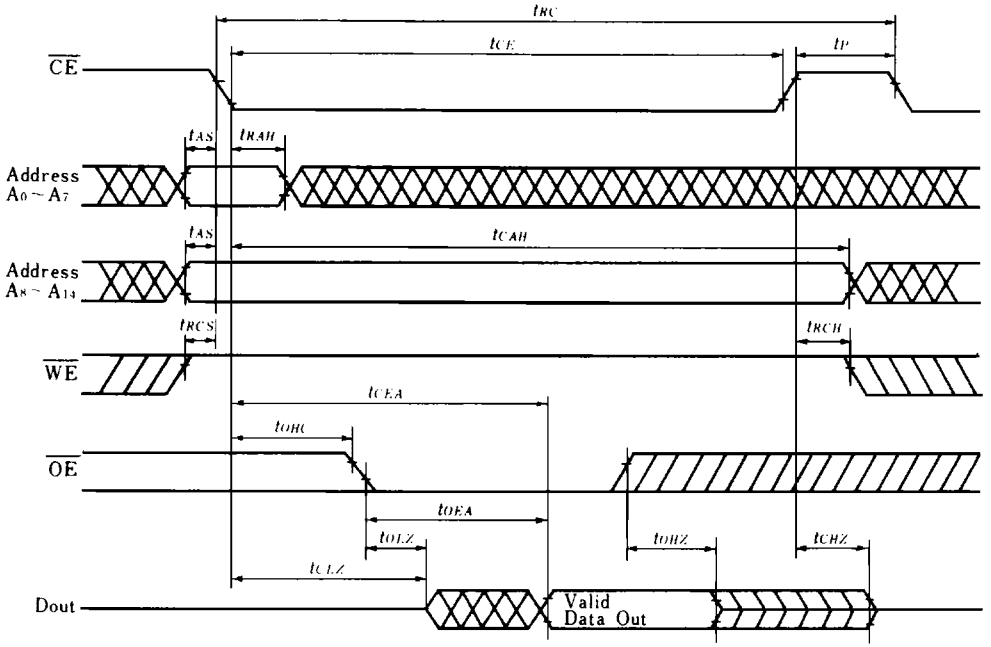
(7) An initial pause of 100μs is required after power-up followed by a minimum of 8 initialization cycles.

■ TIMING WAVEFORMS

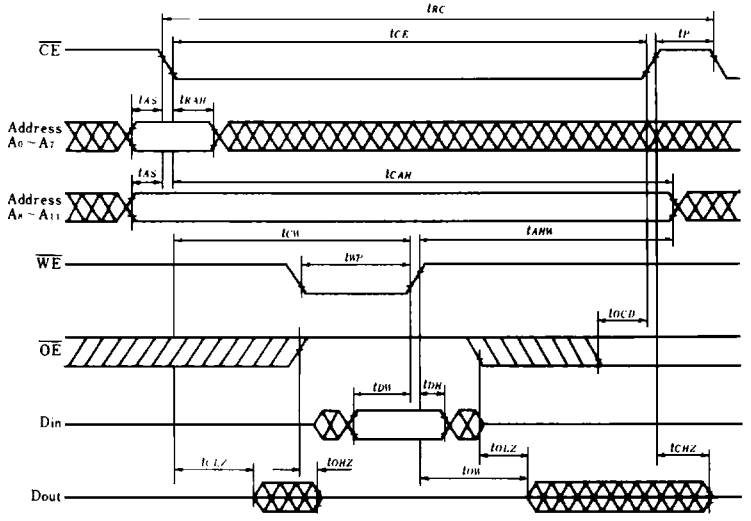
• Read Cycle No. 1 ($\overline{CE}$ controlled)



- **Read Cycle No. 2 ($\overline{OE}$ controlled)**



- **Write Cycle No. 1 ($\overline{OE}$ Clock)**



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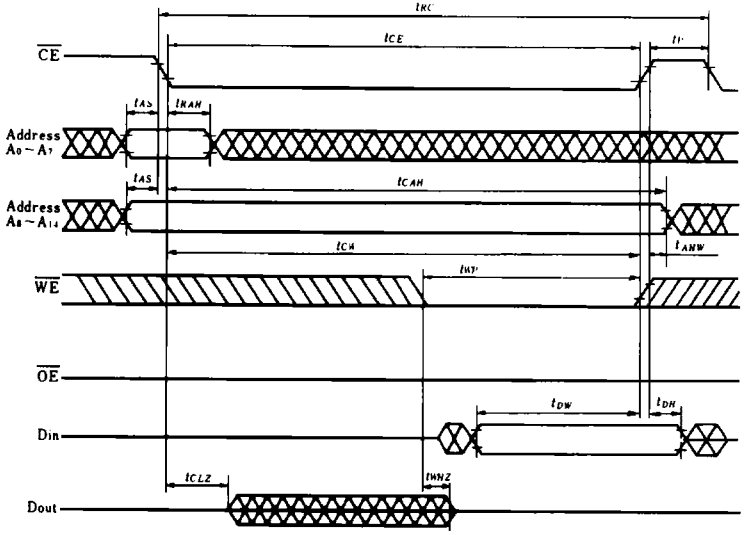
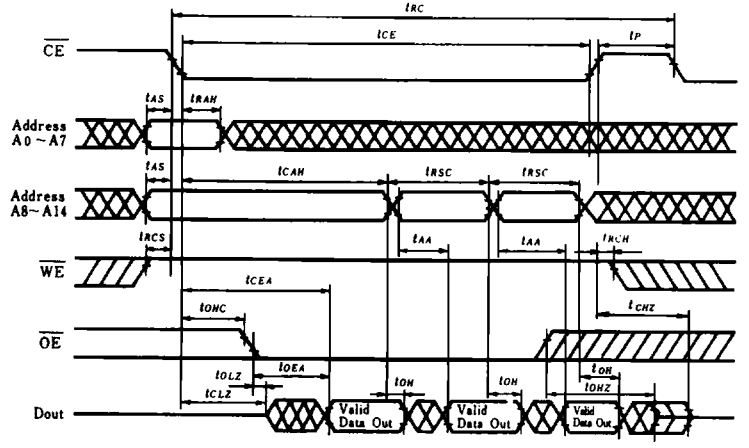
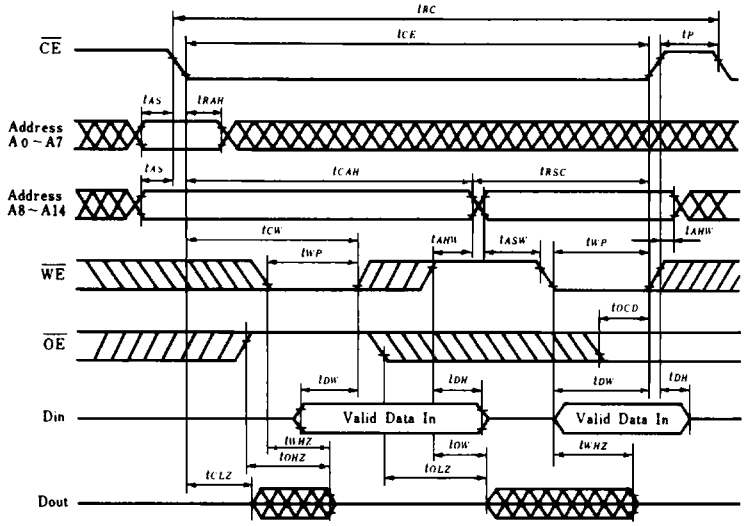
- **Write Cycle No. 2 ($\overline{OE}$ low fix)**



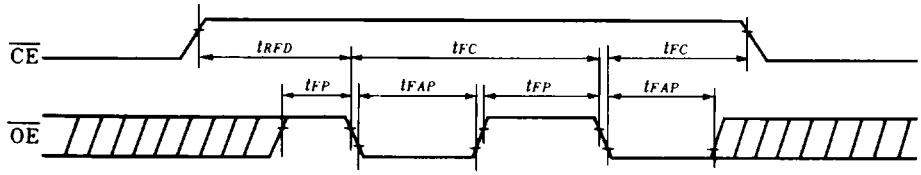
- **Static Column Mode Read Cycle**



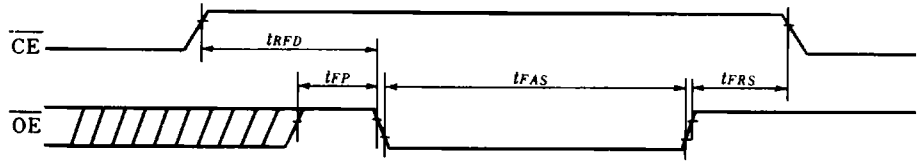
- **Static Column Mode Write Cycle**



- **Automatic Refresh Cycle**



- **Self Refresh Cycle**



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HM658128 Series

131,072-Word × 8-Bit High Speed Psuedo Static Ram

The HM658128 Series has been converted to the HM658128A Series.