CHAPTER 7
ELECTRICAL SPECIFICATIONS

7.1. POWER AND GROUND

For clean on-chip power distribution, the Pentium processor has 50 V_{CC} (power) and 49 V_{SS} (ground) inputs. The 82496 Cache Controller has 56 V_{CC} (power) and 67 V_{SS} (ground) inputs and the 82491 Cache SRAM has 9 V_{CC} (power) and 9 V_{SS} (ground) inputs. Power and ground connections must be made to all external V_{CC} and V_{SS} pins of the Pentium processor, 82496 Cache Controller, and 82491 Cache SRAM. On the circuit board, all V_{CC} pins must be connected to a V_{CC} plane. All Vss pins must be connected to a V_{SS} plane.

7.2. DECOUPLING RECOMMENDATIONS

Liberal decoupling capacitance should be placed near the Pentium processor and 82496 Cache Controller/82491 Cache SRAM second level cache. The CPU Cache Chip Set driving its large address and data buses at high frequencies can cause transient power surges, particularly when driving large capacitive loads.

Low inductance capacitors (i.e., surface mount capacitors) and interconnects are recommended for best high frequency electrical performance. Inductance can be reduced by connecting capacitors directly to the V_{CC} and V_{SS} planes, with minimal trace length between the component pads and vias to the plane. Capacitors specifically for PGA packages are also commercially available.

These capacitors should be evenly distributed among each component. Capacitor values should be chosen to ensure they eliminate both low and high frequency noise components.

7.3. CONNECTION SPECIFICATIONS

All NC pins must remain unconnected.

For reliable operation, always connect unused inputs to an appropriate signal level. Unused active low inputs should be connected to V_{CC}. Unused active high inputs should be connected to ground.

7.4. MAXIMUM RATINGS

Table 7-1 is a stress rating only. Functional operation at the maximums is not guaranteed. Functional operating conditions are given in the AC and DC specification tables.

Extended exposure to the maximum ratings may affect device reliability. Furthermore, although the Pentium processor, 82496 cache controller, and 82491 Cache SRAM contain protective circuitry to resist damage from static electric discharge, always take precautions to avoid high static voltages or electric fields.

Table 7-1. Absolute Maximum Ratings

Case temperature under bias	-65°C to 110°C
Storage temperature	-65°C to 150°C
Voltage on any pin with respect to ground	-0.5 V_{CC} to V_{CC} + 0.5 (V)
Supply voltage with respect to V_{SS}	-0.5V to +6.5V

7.5. DC SPECIFICATIONS

Table 7-2 lists the DC specifications associated with the CPU Cache Chip Set.

Table 7-2. DC Specifications

Legend: PP=Pentium® Processor, CC=82496 Cache Controller, CS=82491 Cache SRAM

V_{CC} = See Notes 16, 17, T_{CASE} = See Notes 18, 19					
Symbol	**Parameter**	**Min**	**Max**	**Unit**	**Notes**
V_{IL}	Input Low Voltage	-0.3	+0.8	V	TTL Level (6) (13)
V_{IH}	Input High Voltage	2.0	Vcc+0.3	V	TTL Level (6) (13)
V_{OL}	Output Low Voltage		0.45	V	TTL Level (1) (6)
V_{OH}	Output High Voltage	2.4		V	TTL Level (2) (6)
I_{CC}	Power Supply Current		900 850 400 365		CC 66MHz (7), (4) CC 60 MHz (7) (4) CS 66 MHz (3), (9) CS 60 MHz (3) (9)
I_{LI}	Input Leakage Current		±15	uA	$0 \le V_{IN} \le V_{CC}$ (8)
I_{LO}	Output Leakage Current		±15	uA	$0 \le V_{OUT} \le V_{CC}$ (8) Tristate
I_{IL}	Input Leakage Current		-400	uA	V_{IN} = 0.45V, (5)
I_{IH}	Input Leakage Current		200	uA	V_{IN} = 2.4V, (10)
C_{IN}	Input Capacitance		15 11 5	pF pF pF	PP, (11) (12) CC, (11) (12) CS, (11) (12)
C_O	Output Capacitance		20 22 --	pF pF pF	PP, (11) (12) CC, (11) (12) CS, (11) (12)
$C_{I/O}$	I/O Capacitance		25 17 10	pF pF pF	PP, (11) (12) CC, (11) (12) CS, (11) (12)
C_{CLK}	CLK Input Capacitance		7 7 7	pF pF pF	PP, (11) (12) CC, (11) (12) CS, (11) (12)
C_{TIN}	Test Input Capacitance		15 9 5	pF pF pF	PP, (11) (12) CC, (11) (12) CS, (11) (12)
C_{TOUT}	Test Output Capacitance		15 14 7	pF pF pF	PP, (11) (12) CC, (11) (12) CS, (11) (12)
C_{TCK}	Test Clock Capacitance		7 9 5	pF pF pF	PP, (11) (12) CC, (11) (12) CS, (11) (12)

NOTES:

(1) Parameter measured at 4 mA load.

For MCFA6-MCFA0, MSET10-MSET0, MTAG11-MTAG0, and MBT3-0, this parameter is measured at 12 mA load.

(2) Parameter measured at 1 mA .

For MCFA6-MCFA0, MSET10-MSET0, MTAG11-MTAG0, and MBT3-0, this parameter is measured at 2 mA load.

(3) 82491 Cache SRAM I_{CC} may be considerably less depending on cycle mix. (For example, idle clocks only require approximately 75 mA)

(4) Typical 82496 Cache Controller Supply current is 800 mA at 66 MHz and 750 mA at 60 MHz.

(5) This parameter is for input with pullup.

(6) TTL levels used for external interface signals.

(7) Worst case average I_{CC} for a mix of test patterns.

(8) This parameter is for input without pullup or pulldown.

(9) Typical 82491 Cache SRAM Supply current is 250 mA at 66 MHz and 230 mA at 60 MHz, assuming a typical cycle mix of: 50% Read Hit - MRU Hit Burst=4, 20% Write Hit Burst=4, 30% Idle.

(10) This parameter is for input with pulldown.

(11) For additional granularity, refer to the I/O models.

(12) Not 100% tested. Guaranteed by design/characterization.

(13) V_{IL} min and V_{IH} max are not 100% tested. Guaranteed by design/characterization.

(14) V_{CC} = 5V ± 5% at 60 MHz

(15) PP V_{CC} = 4.90V to 5.40V at 66 MHz; CC, CS V_{CC} = 5V ± 5% at 66 MHz

(16) PP T_{CASE} = 0°C to +80°C at 60 MHz; CC, CS T_{CASE} = 0°C to +85°C at 60 MHz

(17) PP T_{CASE} = 0°C to +70°C at 66 MHz; CC, CS T_{CASE} = 0°C to +85°C at 66 MHz

7.6. AC SPECIFICATIONS

The AC specifications consist of two sections, Optimized and External interface specifications.

7.6.1. Optimized Interface

The optimized interface is the high-performance interconnect between the Pentium processor, 82496 Cache Controller and 82491 Cache SRAM. This interface is tuned for the known configuration options of the chip set and includes specially designed (non-standard) input and output buffers optimized for the defined electrical environment of each signal path. The specification of this interface is also non-standard; this section describes the signal flight times, signal quality and buffer types parameters used throughout this interface.

The specifications that follow define the requirements of each path in the optimized interface. As outlined in Table 7-3 there are three classes of specifications: flight time to guarantee signal timing; signal quality to guarantee reliable operation; and, buffer models to specify completely flight time and signal quality. Tables 7-3 through 7-17 define the

optimized interface for the **256-Kbyte and 512-Kbyte configurations of the CPU-Cache Chip Set.**

Table 7-3. Three Specification Classes, Their Purpose and the New Parameters

Specification Class	Purpose	Parameters
Flight Time	Guarantee Timing	Maximum Flight Time
Signal Quality	Guarantee Reliable Operation	Absolute Maximum Signal Overshoot (Undershoot)
		Maximum Group Average Overshoot (Undershoot)
		Absolute Maximum Time Beyond the Supply
		Maximum Group Average Time Beyond the Supply
		Maximum Signal Ring-back
		Maximum Settling Time
Buffer Models	Completely Specify Flight Time and Signal Quality	Cin - Input Capacitance
		Lp - Package Inductance
		Cp - Package Capacitance
		dV/dt - Voltage source rate of change
		Ro - Output impedance
		Co - Output Capacitance

7.6.1.1. FLIGHT TIME SPECIFICATION

The first new parameter is flight time. Flight time is the difference in output delay measured between a loaded and an unloaded output buffer.

The most straight forward definition of flight time is the time difference between the loaded and unloaded output signals at the 50% V_{CC} voltage level as illustrated in Figure 7-1 (50% V_{CC} is the normal CMOS switching threshold. The loaded delay must be measured at the last receiver to cross this threshold). This delay is called the 50% delay time.

Unfortunately, it is also necessary to measure delays to the 65% V_{CC} voltage level (or 35% V_{CC} for falling transitions). This is due to differences between waveforms generated in the actual system and for an unloaded buffer, which are caused by the transmission line nature of the system environment. Delays measured to the 65% V_{CC} level must be extrapolated back to the 50% V_{CC} level using a line with a 1V/ns slope (i.e., subtract 0.75 ns when V_{CC}=5V), as shown in Figure 7-2. This delay is called the 65% delay time.

Flight time is defined as the greater of the 50% delay or that obtained by extrapolation from the 65% delay.

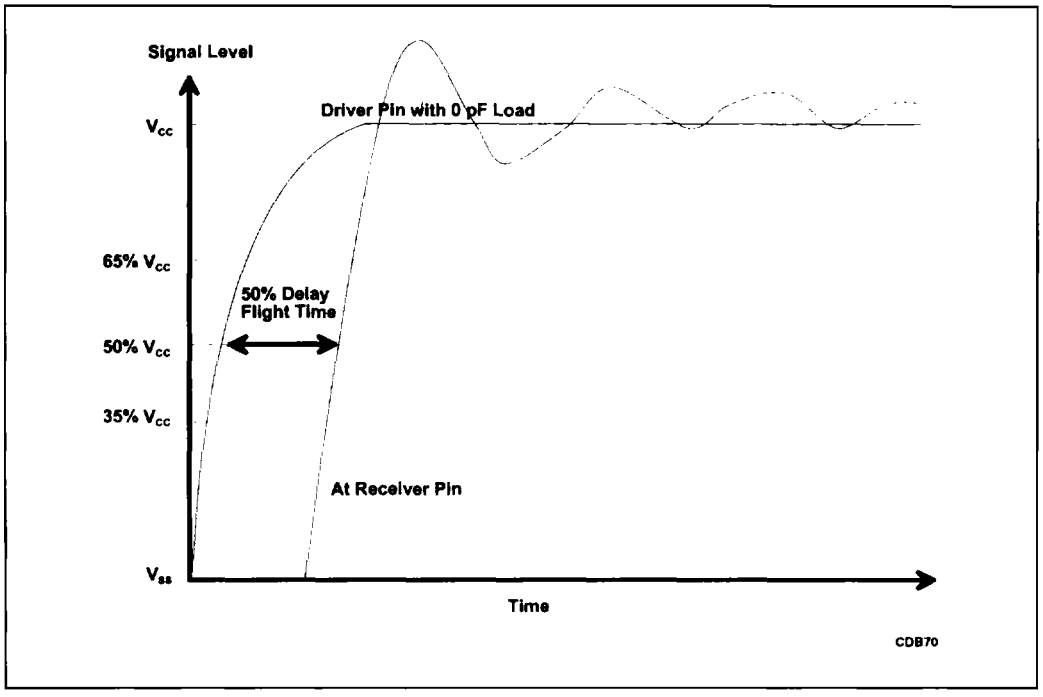


Figure 7-1. Determination of Flight Time

Figure 7-1 shows determination of flight time based on the 50% V_{CC} level measurement of a 0 pF load output with reference to the 50% V_{CC} level of at the receiver pin. The 50% V_{CC} to 65% V_{CC} rise time is faster than 1 volt/nsec in this example.

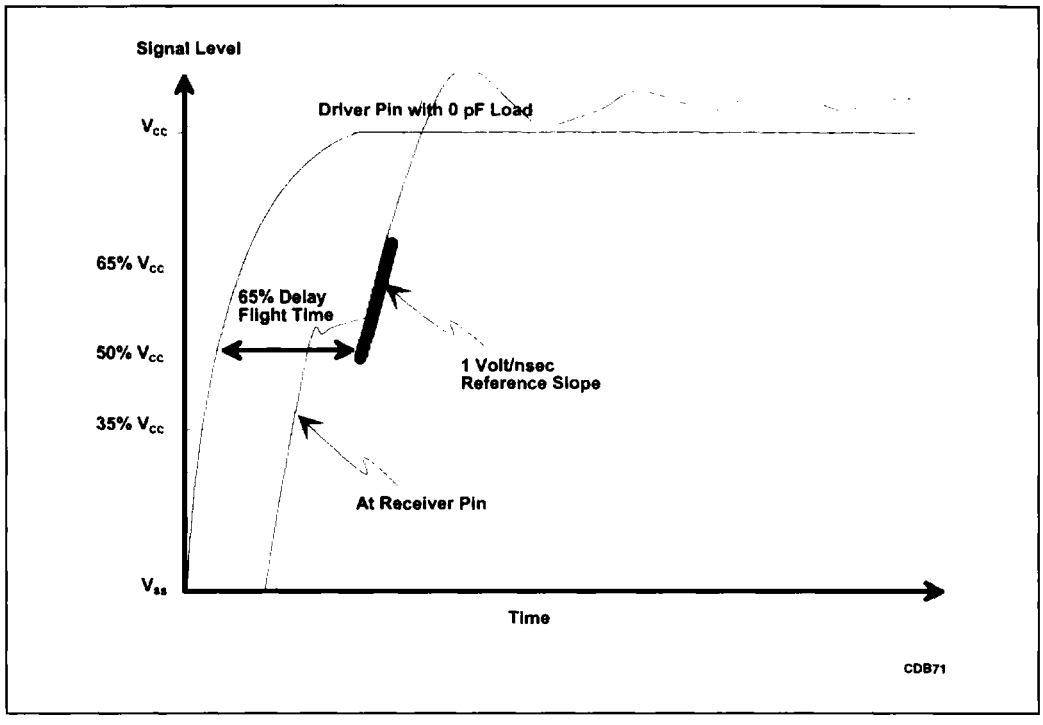


Figure 7-2. Derating the Flight Time

In a system environment it will not usually be possible to measure the delay of an unloaded driver. Figure 7-3 shows the method for measuring flight time in a system environment. As shown, the voltage measured at the pin of the loaded driver will have a ledge near the center of the transition. According to Transmission Line Theory, the time required to reach half the voltage level of the ledge is equivalent to the time required for an unloaded driver to reach the 50% V_{CC} level. The oscillation (if any) seen at the ledge defines the measurement uncertainty for this technique.

To measure flight time via this technique, first measure the maximum and minimum voltages of the ledge and take the average of these two values, $(V_{MAX} + V_{MIN}) / 2$, to arrive at the ledge voltage. Finally, divide the ledge voltage by two, $(V_{MAX} + V_{MIN}) / 4$. The result is the voltage level that approximately corresponds to the point in time at which an unloaded driver's signal would reach the 50% V_{CC} level. The flight time is determined by measuring the difference in time between the $(V_{MAX} + V_{MIN}) / 4$ point and the extrapolated 50% point on the receiver. The uncertainty of this technique is the time difference between the $V_{MIN}/2$ and $V_{MAX}/2$ points.

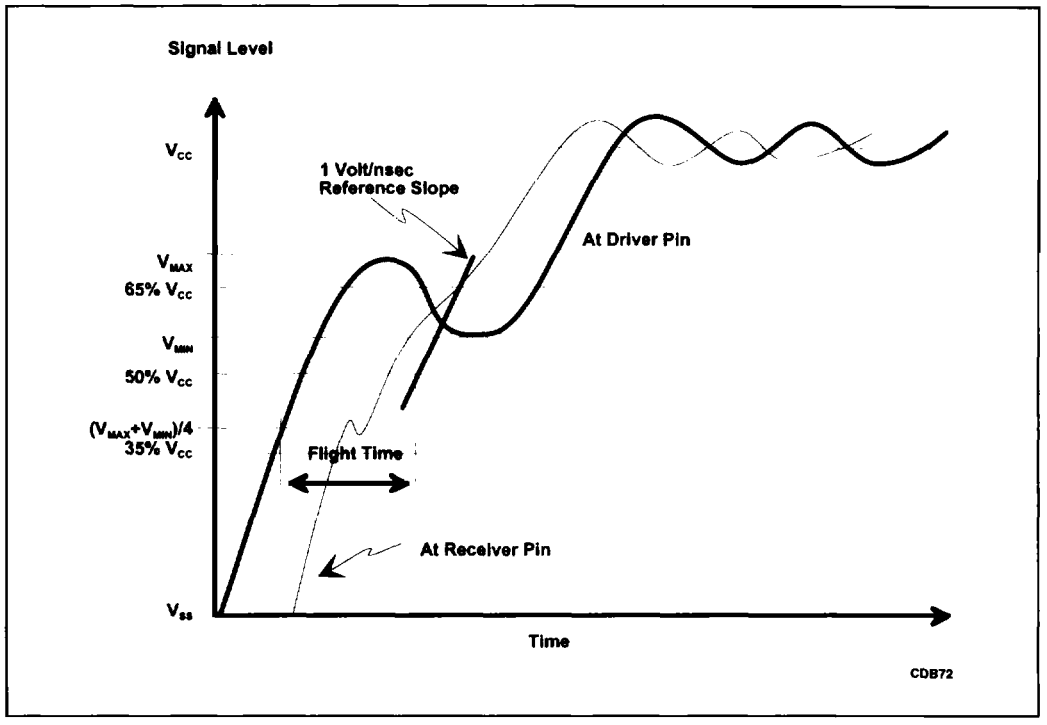


Figure 7-3. In-System Measurement of Flight Time

Table 7-4 describes the maximum flight time and clock skew specifications. Tables 7-5 to Table 7-16 list the flight time and maximum clock skew specifications for each driver-receiver network in the optimized interface. For each net, the driver first order output buffer model type and receiver input buffer model type are also listed. Some signals have **two buffer types** listed in the "Driver Buffer Type" column. These are the signals whose buffer type is **selected** using **BUSCHK#** (Pentium processor) and **CLDRV** (82496 Cache Controller) as described in Table 4-1. The first entry corresponds to driving these configuration signals HIGH during reset and the second to driving them LOW. Tables 7-5 to 7-8 list the flight time and clock skew for the 66-MHz 256-Kbyte CPU Cache Chip Set. Tables 7-9 to 7-12 list the flight time and clock skew for the 60-MHz 256-Kbyte CPU Cache Chip Set. Tables 7-13 to 7-16 list the flight time and clock skew for the 60-MHz 512-Kbyte CPU Cache Chip Set.

Table 7-4. Description of Maximum Flight Time and Clock Skew

Parameter	Description
Maximum Flight Time	Maximum time delay for a signal to reach the receiving component referenced from the driving component's pin, when the driver is unloaded. It includes the time to traverse the PC board trace and any added output delay on the output buffer due to the trace and receiving component loading and is dependent on rise time at the receiving component.
Maximum Clock Skew	Maximum clock skew is the difference in time of the clock signal arriving at different components. It is measured at 0.8V, 1.5V, and 2.0V.

7.6.1.1.1. 66-MHz 256-Kbyte Flight Times

Table 7-5. Signal Group: CPU to Cache RAM (CPU-CRAM) (66-MHz 256-Kbyte Version)

Legend: PP=Pentium® Processor, CC=82496 Cache Controller, CS=82491 Cache SRAM

Driver	Receiver	Max CLK Skew (ns)	Min Flight Time (ns)	Max Flight Time (ns)	Driver Buffer Type	Receiver Buffer Type
PP D0-D63	CS CDATA0-7	0.7	1.0	2.2	ZD2	ZR10
PP DP0-7	CS CDATA0-3	0.7	1.0	2.2	ZD2	ZR10
CS CDATA0-7	PP D0-D63	0.7	1.0	2.2	ZD10	ZR4
CS CDATA0-3	PP DP0-7	0.7	1.0	2.2	ZD10	ZR4

Table 7-6. Signal Group: CPU to Cache (CPU-Cache) (66-MHz 256-Kbyte Version)

Legend: PP=Pentium® Processor, CC=82496 Cache Controller, CS=82491 Cache SRAM

Driver	Receiver	Max CLK Skew (ns)	Max Flight Time (ns)	Driver Buffer Type	Receiver Buffer Type
PP A3-A4	CC CFA0-1	0.2	2.8	ZD6/ZD6a	ZR8
PP A5	CC CFA6	0.2	2.8	ZD6/ZD6a	ZR8
PP A6-A16	CC SET0-10	0.2	2.8	ZD6/ZD6a	ZR8
PP A3-A16	CS A2-A15	0.7	2.8	ZD6/ZD6a	ZR9
CC CFA0-1	PP A3-A4	0.2	9.5	ZD7	ZR6
CC CFA6	PP A5	0.2	9.5	ZD7	ZR6
CC SET0-10	PP A6-A16	0.2	9.5	ZD7	ZR6
CC CFA0-1	CS A2-A3	0.7	9.5	ZD7	ZR9
CC CFA6	CS A4	0.7	9.5	ZD7	ZR9
CC SET0-10	CS A5-A15	0.7	9.5	ZD7	ZR9
PP W/R#	CC W/R#	0.2	3.0	ZD5/ZD5a	ZR7
PP W/R#	CS W/R#	0.7	3.3	ZD5/ZD5a	ZR9
PP HITM#	CC HITM#	0.2	3.0	ZD5/ZD5a	ZR7
PP HITM#	CS HITM#	0.7	3.2	ZD5/ZD5a	ZR9
PP ADS#	CS ADS#	0.7	2.7	ZD5/ZD5a	ZR9
PP BE0-7#	CS BE#	0.7	2.3	ZD1	ZR9
PP BE0-7#	CS CDATA4-7	0.7	2.3	ZD1	ZR10

Table 7-7. Signal Group: CPU to Cache Controller (CPU-CCTL) (66-MHz 256-Kbyte Version)

Legend: PP=Pentium® Processor, CC=82496 Cache Controller, CS=82491 Cache SRAM

Driver	Receiver	Max CLK Skew (ns)	Max Flight Time (ns)	Driver Buffer Type	Receiver Buffer Type
PP A17-A20	CC TAG0-3	0.2	1.7	ZD6/ZD6a	ZR8
PP A21-A28	CC TAG4-11	0.2	1.7	ZD3	ZR8
PP A29-A31	CC CFA2-4	0.2	1.7	ZD3	ZR8
PP BT0-BT3	CC BT0-BT3	0.2	1.7	ZD3	ZR8
CC TAG0-3	PP A17-A20	0.2	3.2	ZD7	ZR6
CC TAG4-11	PP A21-A28	0.2	3.2	ZD7	ZR5
CC AP	PP AP	0.2	2.7	ZD7	ZR3
CC CFA2-4	PP A29-A31	0.2	3.2	ZD7	ZR5
CC BT0-BT3	PP BT0-BT3	0.2	3.2	ZD7	ZR5
PP AP	CC AP	0.2	1.6	ZD4	ZR8
PP SCYC	CC SCYC	0.2	1.6	ZD1	ZR7
PP PWT	CC PWT	0.2	1.6	ZD1	ZR7
PP PCD	CC PCD	0.2	1.6	ZD1	ZR7
PP M/IO#	CC M/IO#	0.2	1.6	ZD1	ZR7
PP D/C#	CC D/C#	0.2	1.4	ZD1	ZR7
PP LOCK#	CC LOCK#	0.2	1.6	ZD1	ZR7
PP CACHE#	CC CACHE#	0.2	1.6	ZD1	ZR7
PP ADSC#	CC ADS#	0.2	1.5	ZD1	ZR7a
CC AHOLD	PP AHOLD	0.2	1.7	ZD8	ZR1
CC EADS#	PP EADS#	0.2	1.7	ZD8	ZR1
CC KEN#	PP KEN#	0.2	1.7	ZD8	ZR1
CC BRDYC1#	PP BRDYC#	0.2	1.6	ZD8	ZR2
CC WBWT#	PP WBWT#	0.2	1.7	ZD8'	ZR1
CC INV	PP INV	0.2	1.7	ZD8	ZR1a
CC NA#	PP NA#	0.2	1.7	ZD8'	ZR1
CC EWBE#	PP EWBE#	0.2	1.7	ZD8	ZR1

Table 7-8. Signal Group: Cache Controller to Cache RAM (CCTL-CRAM) (66-MHz 256-Kbyte Version)

Legend: PP=Pentium® Processor, CC=82496 Cache Controller, CS=82491 Cache SRAM

Driver	Receiver	Max CLK Skew (ns)	Max Flight Time (ns)	Driver Buffer Type	Receiver Buffer Type
CC BOFF#	PP BOFF#	0.2	3.0	ZD9/ZD9a	ZR1
CC BOFF#	CS BOFF#	0.7	3.0	ZD9/ZD9a	ZR9
CC BLAST#	CS BLAST#	0.7	2.5	ZD9/ZD9a	ZR9
CC WRARR#	CS WRARR#	0.7	2.5	ZD9/ZD9a	ZR9
CC WAY	CS WAY	0.7	2.7	ZD9/ZD9a	ZR9
CC MCYC#	CS MCYC#	0.7	2.7	ZD9/ZD9a	ZR9
CC MAWEA#	CS MAWEA#	0.7	2.7	ZD9/ZD9a	ZR9
CC BUS#	CS BUS#	0.7	2.7	ZD9/ZD9a	ZR9
CC WBA	CS WBA	0.7	2.7	ZD9/ZD9a	ZR9
CC WBWE#	CS WBWE#	0.7	2.7	ZD9/ZD9a	ZR9
CC WBTYP	CS WBTYP	0.7	2.7	ZD9/ZD9a	ZR9
CC BRDYC2#	CS BRDYC#	0.7	2.5	ZD9/ZD9a	ZR9
CC BLEC#	CS BLEC#	0.7	2.5	ZD9/ZD9a	ZR9

7.6.1.1.2. 60-MHz 256-Kbyte Flight Times

Table 7-9. Signal Group: CPU to Cache RAM (CPU-CRAM) (60-MHz 256-Kbyte Version)

Legend: PP=Pentium® Processor, CC=82496 Cache Controller, CS=82491 Cache SRAM

Driver	Receiver	Max CLK Skew (ns)	Min Flight Time (ns)	Max Flight Time (ns)	Driver Buffer Type	Receiver Buffer Type
PP D0-D63	CS CDATA0-7	0.8	1.0	2.7	ZD2	ZR10
PP DP0-7	CS CDATA0-3	0.8	1.0	2.7	ZD2	ZR10
CS CDATA0-7	PP D0-D63	0.8	1.0	2.7	ZD10	ZR4
CS CDATA0-3	PP DP0-7	0.8	1.0	2.7	ZD10	ZR4

Table 7-10. Signal Group: CPU to Cache (CPU-Cache) (60-MHz 256-Kbyte Version)

Legend: PP=Pentium® Processor, CC=82496 Cache Controller, CS=82491 Cache SRAM

Driver	Receiver	Max CLK Skew (ns)	Max Flight Time (ns)	Driver Buffer Type	Receiver Buffer Type
PP A3-A4	CC CFA0-1	0.3	3.3	ZD6/ZD6a	ZR8
PP A5	CC CFA6	0.3	3.3	ZD6/ZD6a	ZR8
PP A6-A16	CC SET0-10	0.3	3.3	ZD6/ZD6a	ZR8
PP A3-A16	CS A2-A15	0.8	3.3	ZD6/ZD6a	ZR9
CC CFA0-1	PP A3-A4	0.3	10	ZD7	ZR6
CC CFA6	PP A5	0.3	10	ZD7	ZR6
CC SET0-10	PP A6-A16	0.3	10	ZD7	ZR6
CC CFA0-1	CS A2-A3	0.8	10	ZD7	ZR9
CC CFA6	CS A4	0.8	10	ZD7	ZR9
CC SET0-10	CS A5-A15	0.8	10	ZD7	ZR9
PP W/R#	CC W/R#	0.3	3.5	ZD5/ZD5a	ZR7
PP W/R#	CS W/R#	0.8	3.8	ZD5/ZD5a	ZR9
PP HITM#	CC HITM#	0.3	3.5	ZD5/ZD5a	ZR7
PP HITM#	CS HITM#	0.8	3.7	ZD5/ZD5a	ZR9
PP ADS#	CS ADS#	0.8	3.2	ZD5/ZD5a	ZR9
PP BE0-7#	CS BE#	0.8	2.8	ZD1	ZR9
PP BE0-7#	CS CDATA4-7	0.8	2.8	ZD1	ZR10

Table 7-11. Signal Group: CPU to Cache Controller (CPU-CCTL) (60-MHz 256-Kbyte Version)

Legend: PP=Pentium® Processor, CC=82496 Cache Controller, CS=82491 Cache SRAM

Driver	Receiver	Max CLK Skew (ns)	Max Flight Time (ns)	Driver Buffer Type	Receiver Buffer Type
PP A17-A20	CC TAG0-3	0.3	2.2	ZD6/ZD6a	ZR8
PP A21-A28	CC TAG4-11	0.3	2.2	ZD3	ZR8
PP A29-A31	CC CFA2-4	0.3	2.2	ZD3	ZR8
PP BT0-BT3	CC BT0-BT3	0.3	2.2	ZD3	ZR8
CC TAG0-3	PP A17-A20	0.3	3.7	ZD7	ZR6
CC TAG4-11	PP A21-A28	0.3	3.7	ZD7	ZR5
CC AP	PP AP	0.3	3.2	ZD7	ZR3
CC CFA2-4	PP A29-A31	0.3	3.7	ZD7	ZR5
CC BT0-BT3	PP BT0-BT3	0.3	3.7	ZD7	ZR5
PP AP	CC AP	0.3	2.1	ZD4	ZR8
PP SCYC	CC SCYC	0.3	2.1	ZD1	ZR7
PP PWT	CC PWT	0.3	2.1	ZD1	ZR7
PP PCD	CC PCD	0.3	2.1	ZD1	ZR7
PP M/IO#	CC M/IO#	0.3	2.1	ZD1	ZR7
PP D/C#	CC D/C#	0.3	1.9	ZD1	ZR7
PP LOCK#	CC LOCK#	0.3	2.1	ZD1	ZR7
PP CACHE#	CC CACHE#	0.3	2.1	ZD1	ZR7
PP ADSC#	CC ADS#	0.3	2.0	ZD1	ZR7a
CC AHOLD	PP AHOLD	0.3	2.2	ZD8	ZR1
CC EADS#	PP EADS#	0.3	2.2	ZD8	ZR1
CC KEN#	PP KEN#	0.3	2.2	ZD8	ZR1
CC BRDYC1#	PP BRDYC#	0.3	2.1	ZD8	ZR2
CC WBWT#	PP WBWT#	0.3	2.2	ZD8'	ZR1
CC INV	PP INV	0.3	2.2	ZD8	ZR1a
CC NA#	PP NA#	0.3	2.2	ZD8'	ZR1
CC EWBE#	PP EWBE#	0.3	2.2	ZD8	ZR1

Table 7-12. Signal Group: Cache Controller to Cache RAM (CCTL-CRAM) (60-MHz 256-Kbyte Version)

Legend: PP=Pentium® Processor, CC=82496 Cache Controller, CS=82491 Cache SRAM

Driver	Receiver	Max CLK Skew (ns)	Max Flight Time (ns)	Driver Buffer Type	Receiver Buffer Type
CC BOFF#	PP BOFF#	0.3	3.5	ZD9/ZD9a	ZR1
CC BOFF#	CS BOFF#	0.8	3.5	ZD9/ZD9a	ZR9
CC BLAST#	CS BLAST#	0.8	3.0	ZD9/ZD9a	ZR9
CC WRARR#	CS WRARR#	0.8	3.0	ZD9/ZD9a	ZR9
CC WAY	CS WAY	0.8	3.2	ZD9/ZD9a	ZR9
CC MCYC#	CS MCYC#	0.8	3.2	ZD9/ZD9a	ZR9
CC MAWEA#	CS MAWEA#	0.8	3.2	ZD9/ZD9a	ZR9
CC BUS#	CS BUS#	0.8	3.2	ZD9/ZD9a	ZR9
CC WBA	CS WBA	0.8	3.2	ZD9/ZD9a	ZR9
CC WBWE#	CS WBWE#	0.8	3.2	ZD9/ZD9a	ZR9
CC WBTYP	CS WBTYP	0.8	3.2	ZD9/ZD9a	ZR9
CC BRDYC2#	CS BRDYC#	0.8	3.0	ZD9/ZD9a	ZR9
CC BLEC#	CS BLEC#	0.8	3.0	ZD9/ZD9a	ZR9

7.6.1.1.3. 60-MHz 512-Kbyte Flight Times

Table 7-13 to Table 7-16 list the flight time and clock skew for the 60-MHz 512-Kbyte CPU Cache Chip Set. Note the maximum frequency of the 512K chip set is 60 MHz. All external interface specifications remain unchanged except for the maximum frequency.

Table 7-13. Signal Group: CPU to Cache RAM (CPU-CRAM) (60-MHz 512-Kbyte Version)

Legend: PP=Pentium® Processor, CC=82496 Cache Controller, CS=82491 Cache SRAM

Driver	Receiver	Max CLK Skew (ns)	Min Flight Time (ns)	Max Flight Time (ns)	Driver Buffer Type	Receiver Buffer Type
PP D0-D63	CS CDATA0-3	0.8	1.0	2.7	ZD2	ZR10
PP DP0-7	CS CDATA0-3	0.8	1.0	2.7	ZD2	ZR10
CS CDATA0-3	PP D0-D63	0.8	1.0	2.7	ZD10	ZR4
CS CDATA0-3	PP DP0-7	0.8	1.0	2.7	ZD10	ZR4

Table 7-14. Signal Group: CPU to Cache (CPU-Cache) (60-MHz 512-Kbyte Version)

Legend: PP=Pentium® Processor, CC=82496 Cache Controller, CS=82491 Cache SRAM

Driver	Receiver	Max CLK Skew (ns)	Max Flight Time (ns)	Driver Buffer Type	Receiver Buffer Type
PP A3-A4	CC CFA0-1	0.3	3.3	ZD6/ZD6a	ZR8
PP A5-A6	CC CFA5-6	0.3	3.3	ZD6/ZD6a	ZR8
PP A7-A17	CC SET0-10	0.3	3.3	ZD6/ZD6a	ZR8
PP A3-A17	CS A1-A15	0.8	3.3	ZD6/ZD6a	ZR9
CC CFA0-1	PP A3-A4	0.3	10.6	ZD7	ZR6
CC CFA5-6	PP A5-A6	0.3	10.6	ZD7	ZR6
CC SET0-10	PP A7-A17	0.3	10.6	ZD7	ZR6
CC CFA0-1	CS A1-A2	0.8	10.6	ZD7	ZR9
CC CFA5-6	CS A3-A4	0.8	10.6	ZD7	ZR9
CC SET0-10	CS A5-A15	0.8	10.6	ZD7	ZR9
PP W/R#	CC W/R#	0.3	3.9	ZD5/ZD5a	ZR7
PP W/R#	CS W/R#	0.8	4.0	ZD5/ZD5a	ZR9
PP HITM#	CC HITM#	0.3	3.8	ZD5/ZD5a	ZR7
PP HITM#	CS HITM#	0.8	3.9	ZD5/ZD5a	ZR9
PP ADS#	CS ADS#	0.8	3.2	ZD5/ZD5a	ZR9
PP BE0-7#	CS BE#	0.8	2.8	ZD1	ZR9
PP BE0-7#	CS CDATA4-7	0.8	2.8	ZD1	ZR10

Table 7-15. Signal Group: CPU to Cache Controller (CPU-CCTL) (60-MHz 512-Kbyte Version)

Legend: PP=Pentium® Processor, CC=82496 Cache Controller, CS=82491 Cache SRAM

Driver	Receiver	Max CLK Skew (ns)	Max Flight Time (ns)	Driver Buffer Type	Receiver Buffer Type
PP A18-A21	CC TAG0-3	0.3	2.2	ZD6/ZD6a	ZR8
PP A22-A29	CC TAG4-11	0.3	2.2	ZD3	ZR8
PP A30-A31	CC CFA2-3	0.3	2.2	ZD3	ZR8
PP BT0-BT3	CC BT0-BT3	0.3	2.2	ZD3	ZR8
CC TAG0-3	PP A18-A21	0.3	3.7	ZD7	ZR6
CC TAG4-11	PP A22-A29	0.3	3.7	ZD7	ZR5
CC AP	PP AP	0.3	3.2	ZD7	ZR3
CC CFA2-3	PP A30-A31	0.3	3.7	ZD7	ZR5
CC BT0-BT3	PP BT0-BT3	0.3	3.7	ZD7	ZR5
PP AP	CC AP	0.3	2.1	ZD4	ZR8
PP SCYC	CC SCYC	0.3	2.1	ZD1	ZR7
PP PWT	CC PWT	0.3	2.1	ZD1	ZR7
PP PCD	CC PCD	0.3	2.1	ZD1	ZR7
PP M/IO#	CC M/IO#	0.3	2.1	ZD1	ZR7
PP D/C#	CC D/C#	0.3	1.9	ZD1	ZR7
PP LOCK#	CC LOCK#	0.3	2.1	ZD1	ZR7
PP CACHE#	CC CACHE#	0.3	2.1	ZD1	ZR7
PP ADSC#	CC ADS#	0.3	2.0	ZD1	ZR7a
CC AHOLD	PP AHOLD	0.3	2.2	ZD8	ZR1
CC EADS#	PP EADS#	0.3	2.2	ZD8	ZR1
CC KEN#	PP KEN#	0.3	2.2	ZD8	ZR1
CC BRDYC1#	PP BRDYC#	0.3	2.1	ZD8	ZR2
CC WBWT#	PP WBWT#	0.3	2.2	ZD8'	ZR1
CC INV	PP INV	0.3	2.2	ZD8	ZR1a
CC NA#	PP NA#	0.3	2.2	ZD8'	ZR1
CC EWBE#	PP EWBE#	0.3	2.2	ZD8	ZR1

Table 7-16. Signal Group: Cache Controller to Cache RAM (CCTL-CRAM) (60-MHz 512-Kbyte Version)

Legend: PP=Pentium® Processor, CC=82496 Cache Controller, CS=82491 Cache SRAM

Driver	Receiver	Max CLK Skew (ns)	Max Flight Time (ns)	Driver Buffer Type	Receiver Buffer Type
CC BOFF#	PP BOFF#	0.3	3.7	ZD9/ZD9a	ZR1
CC BOFF#	CS BOFF#	0.8	3.7	ZD9/ZD9a	ZR9
CC BLAST#	CS BLAST#	0.8	3.0	ZD9/ZD9a	ZR9
CC WRARR#	CS WRARR#	0.8	3.0	ZD9/ZD9a	ZR9
CC WAY	CS WAY	0.8	3.2	ZD9/ZD9a	ZR9
CC MCYC#	CS MCYC#	0.8	3.2	ZD9/ZD9a	ZR9
CC MAWEA#	CS MAWEA#	0.8	3.2	ZD9/ZD9a	ZR9
CC BUS#	CS BUS#	0.8	3.2	ZD9/ZD9a	ZR9
CC WBA	CS WBA	0.8	3.2	ZD9/ZD9a	ZR9
CC WBWE#	CS WBWE#	0.8	3.2	ZD9/ZD9a	ZR9
CC WBTYP	CS WBTYP	0.8	3.2	ZD9/ZD9a	ZR9
CC BRDYC2#	CS BRDYC#	0.8	3.0	ZD9/ZD9a	ZR9
CC BLEC#	CS BLEC#	0.8	3.0	ZD9/ZD9a	ZR9

7.6.1.2. SIGNAL QUALITY

Acceptable signal quality must be maintained over all operating conditions. Figure 7-4 illustrates the parameters used to verify acceptable signal quality. Table 7-17 describes each of these parameters.

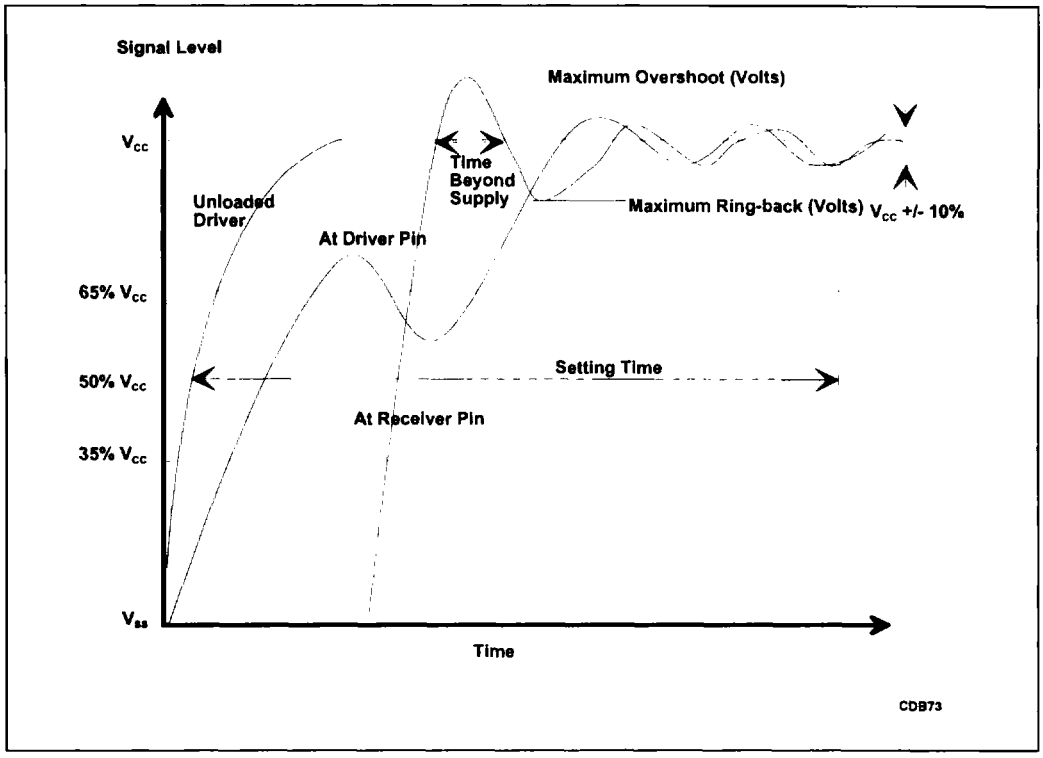


Figure 7-4. Driver and Receiver Signal Waveforms Showing Signal Quality Parameters

Beyond the absolute maximum values shown in Figure 7-4, each of the four signal groups defined by Tables 7-5 to 7-16 in the CPU-Cache Chip Set optimized interface must meet a maximum group average for Overshoot (Undershoot) and Time Beyond the Supply. Maximum group average overshoot (undershoot) is the numeric average of the maximum signal overshoot (undershoot) for each signal within the signal group. Maximum group average Time Beyond the Supply is the numeric average of the Maximum Time Beyond the Supply for each signal within the signal group.

Group average is calculated assuming one component is driving the line. For example the CPU-CRAM group includes the data bus between the Pentium processor and 82491 Cache SRAM. The averages should be calculated assuming the Pentium processor is driving the data bus. A second average is calculated assuming the 82491 Cache SRAM is driving. Both must be less than the specified limit.

Since the maximum value for signal overshoot and undershoot will be limited by the component's ESD diodes, both the absolute and group average specifications for overshoot and undershoot must be met under the simulation conditions described by Tables 7-5 to 7-17.

Table 7-17. Specifications for Signal Quality

Parameter	Description	Group	Specification
Absolute Maximum Signal Overshoot (Undershoot)	Absolute value of the maximum voltage at the receiving pin above V_{CC} (or below V_{SS}) relative to V_{CC} (or V_{SS}) level. (Assumes input diodes are not present.)	NA	3.0 Volts
Absolute Maximum Time Beyond the Supply	Maximum time a signal may exceed V_{CC} (or V_{SS}). Time beyond supply can be ignored if the overshoot is less than 0.5 volts.	NA	6 ns
Maximum Signal Ring-back	Absolute value of the maximum voltage at the receiving pin below V_{CC} (or above V_{SS}) relative to V_{CC} (or V_{SS}) level after the signal has reached its maximum voltage level.	NA	65% V_{CC} Volts (low to high) 35% V_{CC} Volts (high to low)
Maximum Settling Time (Guideline)	Total time required for a signal to settle within 10% of its final value referenced from the unloaded driver's initial crossing of the 50% level.	NA	12.5 nsec
Maximum Group Average Overshoot (Undershoot)	The maximum numeric average of the signal overshoot (undershoot) for all signals within a signal group.	CPU-CRAM	1.5 Volt
		CPU-Cache	2.5 Volt
		CPU-CCTL	1.5 Volt
		CCTL-CRAM	2.5 Volt
Maximum Group Average Time Beyond Supply	The maximum numeric average of the time a signal may exceed V_{CC} (or V_{SS}) for all signals within a signal group. (Signals whose overshoot is less than 0.5V should be ignored in calculating this average.)	CPU-CRAM	3.0 ns
		CPU-Cache	4.5 ns
		CPU-CCTL	3.0 ns
		CCTL-CRAM	4.5 ns

The settling time is defined as the time a signal requires at the receiver to settle within 10% of V_{CC} or V_{SS}. Settling time is the maximum time allowed for a signal to reach within 10% of its final value.

Most available simulation tools are unable to simulate settling time so that it accurately reflects silicon measurements. On a physical board, second order effects and other effects serve to dampen the signal at the receiver. Because of all these concerns, settling time is a recommendation or a tool for layout tuning and not a specification.

Settling time is simulated at the slow corner, to make sure that there is no impact on the flight times of the signals if the waveform has not settled. Settling time may be simulated with the diodes included or excluded from the input buffer model. If diodes are included, Settling Time recommendation will be easier to meet.

Although simulated settling time has not shown good correlation with physical, measured settling time, settling time simulations can still be used as a tool to tune layouts.

Use the following procedure to verify board simulation and tuning with concerns for settling time.

1. Simulate settling time at the slow corner for a particular signal.

2. If settling time violations occur (signal requires more than 12.5 ns. to settle to +/- 10% of its final value), simulate signal trace with DC diodes in place at the receiver pin.
3. If settling time violations still occur, simulate flight times for 5 consecutive cycles for that particular signal.
4. If flight time values are consistent over the 5 consecutive cycles, settling time should not be a concern. If however, flight times are not consistent over the 5 consecutive cycles, tuning of the layout is required.
5. Note that, for signals that are allocated 2 cycles for flight time, the recommended settling time is doubled.

Figure 7-4 depicts settling time. Note that the maximum settling time to within 10% of VIH or VIL is 12.5ns.

7.6.2. External Interface

The external interface is the interface between the chip set components and the memory bus controller, memory address bus, and memory data bus. Intel supplies buffer models for this interface to aid system designers simulation of this section of their design. Unlike the optimized interface, Intel supplies the AC specifications of output valid delay and input setup and hold times.

Tables 7-18 to 7-21 list the 66-MHz AC specifications and Tables 7-22 to 7-25 list the 60-MHz AC specifications associated with the chip set's external interface signals.

All timings are referenced to 1.5 volts for both "0" and "1" logic levels unless otherwise specified. Within the sampling window, a synchronous input must be stable for correct Pentium processor, 82496 Cache Controller, and 82491 Cache SRAM operation.

Care should be taken to read all notes associated with a particular timing parameter. In addition, the following list of notes apply to the timing specification tables in general and are not associated with any one timing. They are 6, 13, 14, 15, 37, 47, 48, and 50.

7.6.2.1. 66-MHz AC SPECIFICATIONS

Table 7-18. 66-MHz CPU Cache Chip Set Common Timings

V_{CC} = See Note 51, Tcase = See Note 52, C_L = 0 pF						
Symbol	**Parameter**	**Min**	**Max**	**Unit**	**Fig.**	**Notes**
t1	CLK Frequency	33.33	66.66	MHz		1X clock, (1), (49)
t2	CLK Period	15	30	ns	7-5	
t3	CLK High Time	4		ns	7-5	(2)
t4	CLK Low Time	4		ns	7-5	(3)
t5	CLK Rise Time	0.15	1.5	ns	7-5	(4)
t6	CLK Fall Time	0.15	1.5	ns	7-5	(4)
t7	CLK Stability		+/- 250	pS		(18), (19), (20), (21)
t8	RESET, INIT Setup Time	5		ns	7-9	To guarantee recognition on a given CLK edge. (16), (17)
t9	RESET, INIT Hold Time	1.5		ns	7-9	To guarantee recognition on a given CLK edge.
t10	RESET Pulse Width, CLK and V_{CC} Stable	15		CLKs	7-9	(11), (17)
t11	INIT Pulse Width, Async.	2		CLKs		To guarantee asynchronous recognition
t13	RESET Active After CLK and V_{CC} Stable	1		ms	7-9	Power Up (11), (12)
t20	TCK Frequency	—	16	MHz		
t21	TCK Period	62.5		ns	7-5	
t22	TCK High Time	25		ns	7-5	(2)
t23	TCK Low Time	25		ns	7-5	(3)
t24	TCK Rise Time		5	ns	7-5	(9), (4)
t25	TCK Fall Time		5	ns	7-5	(9), (4)

Table 7-18. 66-MHz CPU Cache Chip Set Common Timings (Contd.)

V_{CC} = See Note 51, Tcase = See Note 52, C_L = 0 pF						
Symbol	**Parameter**	**Min**	**Max**	**Unit**	**Fig.**	**Notes**
t28	TRST# Pulse Width	40		ns	7-15	(46), Asynchronous
t29	TDI, TMS Setup Time	5		ns	7-14	(7)
t30	TDI, TMS Hold Time	13		ns	7-14	(7)
t31	TDO Valid Delay	3	20	ns	7-14	(8)
t32	TDO Float Delay		25	ns	7-14	(8), (46)
t33	All Non-Test Outputs Valid Delay	3	20	ns	7-14	(8), (10)
t34	All Non-Test Outputs Float Delay		25	ns	7-14	(8), (10), (46)
t35	All Non-Test Inputs Setup Time	5		ns	7-14	(7), (8)
t36	All Non-Test Inputs Hold Time	13		ns	7-14	(7), (8)

Table 7-19. 66-MHz Pentium® Processor Memory Bus Interface Timings

Legend: PP=Pentium® Processor, CC=82496 Cache Controller, CS=82491 Cache SRAM

V_{CC} = See Note 51, Tcase = See Note 52, C_L = 0 pF						
Symbol	**Parameter**	**Min**	**Max**	**Unit**	**Fig.**	**Notes**
t40	PP reset configurations Setup Time	5		ns	7-9	
t41	PP reset configurations Hold Time	1.5		ns	7-9	
t42	PP reset configurations Setup Time Referenced to Falling Edge of RESET	2		CLKs	7-9	
t43	PP reset configurations Hold Time Reference to Falling Edge of RESET	2		CLKs	7-9	
t50	HLDA Valid Delay	1.5	8	ns	7-6	(5)
t51	BREQ Valid Delay	1.5	8	ns	7-6	
t52	PCHK#, APCHK#, FERR#, IERR# Valid Delay	1.5	8.3	ns	7-6	(5)
t53	IU, IV, IBT Valid Delay	1.5	10	ns	7-6	
t54	BP0-3, PM0-1 Valid Delay	1.5	10	ns	7-6	
t55	A20M#, FLUSH#, IGNNE#, NMI, INTR, Setup Time	5		ns	7-7	(16), (17)
t56	A20M#, FLUSH#, IGNNE#, NMI, INTR, Hold Time	1.5		ns	7-7	
t57	FLUSH#, IGNNE#, NMI, Pulse Width, Async	2		CLKs		(17)
t58	PEN#, BUSCHK# Setup Time	5		ns	7-7	
t59	PEN#, BUSCHK# Hold Time	1.5		ns	7-7	
t60	HOLD Setup Time	5		ns	7-7	
t61	HOLD Hold Time	1.5		ns	7-7	
t62	BRDY# Setup Time	5		ns	7-7	
t63	BRDY# Hold Time	1.5		ns	7-7	
t64	R/S#, SMI# Setup Time	5		ns	7-7	(16), (17)
t65	R/S#, SMI# Hold Time	1.5		ns	7-7	
t66	R/S#, SMI# Pulse Width, Async	2		CLKs		(17)
t67	PRDY, SMIACT# Valid Delay	1.5	8	ns	7-6	

Table 7-20. 66-MHz 82496 Cache Controller Memory Bus Interface Timings

V_{CC} = See Note 51, Tcase = See Note 52, C_L = 0 pF						
Symbol	**Parameter**	**Min**	**Max**	**Unit**	**Fig.**	**Notes**
t70	CFG0-2, CLDRV, HIGHZ#, MALDRV, SLFTST#, SNPMD, WWOR#, FLUSH#[V_{CC}] Setup Time	6		ns	7-9	(12), (22), (36)
t71	CFG0-2, CLDRV, HIGHZ#, MALDRV, SLFTST#, SNPMD, WWOR#, FLUSH#[V_{CC}] Hold Time	1		ns	7-9	(12), (23), (36)
t72	CFG0-2, CLDRV, HIGHZ#, MALDRV, SLFTST#, SNPMD, WWOR#, FLUSH#[V_{CC}] Setup Time Referenced to Falling Edge of RESET	10		CLKs	7-9	(12), (36)
t73	CFG0-2, CLDRV, HIGHZ#, MALDRV, SLFTST#, SNPMD, WWOR#, FLUSH#[V_{CC}] Hold Time Referenced to Falling Edge of RESET	0		CLKs	7-9	(12), (36)
t75	FLUSH#, SYNC# Setup Time	6		ns	7-7	(34)
t76	FLUSH#, SYNC#, Hold Time	1		ns	7-7	(34)
t77	FLUSH#, SYNC#, Pulse Width, Async	2		CLKs		
t80	CADS#, CDTS# Valid Delay	1.5	8.2	ns	7-6	Glitch Free
t81	KLOCK#, MCACHE#, RDYSRC Valid Delay	1.5	8.2	ns	7-6	KLOCK# is Glitch Free
t82	CW/R#, CD/C#, CMI/O# Valid Delay	1.5	8.2	ns	7-6	
t83	CPWT, CPCD, CCACHE#, CSCYC Valid Delay	1.5	8.2	ns	7-6	
t84	CAHOLD, CWAY, PALLC# Valid Delay	1.5	8.2	ns	7-6	
t85	FSIOUT# Valid Delay	1.5	8.2	ns	7-6	
t86	NENE#, SMLN# Valid Delay	1.5	12	ns	7-6	
t87	APERR#, IPERR#, MAPERR# Valid Delay	1.5	8.2	ns	7-6	Glitch Free
t88	APIC# Valid Delay	1.5	12	ns	7-6	
t89	BLE# Valid Delay	1.5	8.2	ns	7-6	(35)

Table 7-20. 66-MHz 82496 Cache Controller Memory Bus Interface Timings (Contd.)

V_{CC} = See Note 51, Tcase = See Note 52, C_L = 0 pF						
Symbol	**Parameter**	**Min**	**Max**	**Unit**	**Fig.**	**Notes**
t90	MCFA0-6, MSET0-10, MTAG0-11, MAP, MBT0-3 Valid Delay	1.5	11	ns	7-6	(25), (43)
t91	MCFA0-6, MSET0-10, MTAG0-11, MAP, MBT0-3 Valid Delay	1.5	11	ns	7-10	(26), (43)
t92	MCFA0-6, MSET0-10, MTAG0-11, MAP, MBT0-3 Valid Delay	1.5	10	ns	7-10	(27), (43)
t93	MCFA0-6, MSET0-10, MTAG0-11, MAP, MBT0-3 Float Delay		11	ns	7-10	(28), (46)
t95	BRDY#, CRDY# Setup Time	6.5		ns	7-7	
t96	BRDY#, CRDY# Hold Time	1		ns	7-7	
t97	BGT#, CNA#, KWEND#, SWEND# Setup Time	6		ns	7-7	
t98	BGT#, CNA#, KWEND#, SWEND# Hold Time	1		ns	7-7	
t100	DRCTM#, MRO#, MWB/WT# Setup Time	6		ns	7-7	(24)
t100a	MKEN# Setup Time	6.5		ns	7-7	(24)
t101	DRCTM#, MKEN#, MRO#, MWB/WT# Hold Time	1		ns	7-7	(24)
t110	SNPCLK Frequency	8.3	66.66	MHz		1X clock
t111	SNPCLK Period	15	120	ns	7-5	
t112	SNPCLK High Time	4		ns	7-5	
t113	SNPCLK Low Time	4		ns	7-5	
t114	SNPCLK Rise Time		1.5	ns	7-5	(38)
t115	SNPCLK Fall Time		1.5	ns	7-5	(38)
t118	SNPADS#, SNPCYC# Valid Delay	1.5	8.2	ns	7-6	Glitch Free.
t120	MCFA0-6, MSET0-10, MTAG0-11, MAP, MBT0-3 Setup Time	6		ns	7-7	(29)
t121	MCFA0-6, MSET0-10, MTAG0-11, MAP, MBT0-3 Hold Time	1		ns	7-7	(29)
t122	MCFA0-6, MSET0-10, MTAG0-11, MAP, MBT0-3 Setup Time	6		ns	7-7	(30)

Table 7-20. 66-MHz 82496 Cache Controller Memory Bus Interface Timings (Contd.)

V_{CC} = See Note 51, Tcase = See Note 52, C_L = 0 pF						
Symbol	**Parameter**	**Min**	**Max**	**Unit**	**Fig.**	**Notes**
t123	MCFA0-6, MSET0-10, MTAG0-11, MAP, MBT0-3 Hold Time	1		ns	7-7	(30)
t124	MCFA0-6, MSET0-10, MTAG0-11, MAP, MBT0-3 Setup Time	1		ns	7-8	(31)
t125	MCFA0-6, MSET0-10, MTAG0-11, MAP, MBT0-3 Hold Time	6		ns	7-8	(31)
t130	MAOE#, MBAOE#, SNPINV, SNPNCA Setup Time	6		ns	7-7	(29)
t131	MAOE#, MBAOE#, SNPINV, SNPNCA Hold Time	1		ns	7-7	(29)
t132	MAOE#, MBAOE#, SNPINV, SNPNCA Setup Time	6		ns	7-7	(30)
t133	MAOE#, MBAOE#, SNPINV, SNPNCA Hold Time	1		ns	7-7	(30)
t134	MAOE#, MBAOE#, SNPINV, SNPNCA Setup Time	1		ns	7-8	(31)
t135	MAOE#, MBAOE#, SNPINV, SNPNCA Hold Time	6		ns	7-8	(31)
t140	SNPSTB# Setup Time	6		ns	7-7	(29)
t141	SNPSTB# Hold Time	1		ns	7-7	(29)
t142	SNPSTB# Setup Time	6		ns	7-7	(30)
t143	SNPSTB# Hold Time	1		ns	7-7	(30)
t144	SNPSTB# Active Time	6		ns	7-16	(32)
t145	SNPSTB# Inactive Time	6		ns	7-16	(32)
t148	MHITM#, MTHIT#, SNPBSY# Valid Delay	1.5	10	ns	7-6	

Table 7-21. 66-MHz 82491 Cache SRAM Memory Bus Interface Timings

V_{CC} = See Note 51, Tcase = See Note 52, C_L = 0 pF						
Symbol	**Parameter**	**Min**	**Max**	**Unit**	**Fig.**	**Notes**
t150	MDLDRV, MSTBM, MTR4/8#, MX4/8#, PAR# Setup Time	5		ns	7-9	(22), (42)
t151	MDLDRV, MSTBM, MTR4/8#, MX4/8#, PAR# Hold Time	1		ns	7-9	(23), (42)
t152	MDLDRV, MSTBM, MTR4/8#, MX4/8#, PAR# Setup Time Referenced to Falling Edge of RESET	4		CLKs	7-9	(41), (42)
t153	MDLDRV, MSTBM, MTR4/8#, MX4/8#, PAR# Hold Time Referenced to Falling Edge of RESET	0		CLKs	7-9	(41), (42)
t155	BRDY#, CRDY# Setup Time	5		ns	7-7	
t156	BRDY#, CRDY# Hold Time	1		ns	7-7	
t160	MDATA Setup to CLK (CLK before BRDY# Active)	5		ns	7-7	(44)
t161	MDATA Valid Delay From CLK (CLK from CDTS# Valid, MDOE# Active)		13	ns	7-6	(49)
t162	MDATA Valid Delay From MDOE# Active		8	ns	7-10	
t163	MDATA Float Delay From MDOE# Inactive		10	ns	7-10	
t165	MBE# Valid Delay	1.5	8	ns	7-6	(39)
Clocked Mode						
t170	MCLK, MOCLK Frequency		66.66	MHz		1X clock, (49)
t171	MCLK, MOCLK Period	15		ns	7-5	
t172	MOCLK High Time	4		ns	7-5	
t173	MOCLK Low Time	4		ns	7-5	
t174	MCLK High Time	5		ns	7-5	(40)
t175	MCLK Low Time	5		ns	7-5	(40)
t176	MCLK, MOCLK Rise Time		1.5	ns	7-5	
t177	MCLK, MOCLK Fall Time		1.5	ns	7-5	

Table 7-21. 66-MHz 82491 Cache SRAM Memory Bus Interface Timings (Contd.)

V_{CC} = See Note 51, Tcase = See Note 52, C_L = 0 pF						
Symbol	**Parameter**	**Min**	**Max**	**Unit**	**Fig.**	**Notes**
Clocked Mode						
t180	MOCLK Falling Edge To MCLK Rising Edge	2		ns		
t181	MFRZ#, MZBT# Setup Time	5		ns	7-7	Referenced to MCLK
t182	MFRZ#, MZBT# Hold Time	1		ns	7-7	Referenced to MCLK
t183	MBRDY#, MSEL#, MEOC# Setup Time	5		ns	7-7	Referenced to MCLK
t184	MBRDY#, MSEL#, MEOC# Hold Time	1		ns	7-7	Referenced to MCLK
t185	MDATA Setup Time	5		ns	7-7	Referenced to MCLK
t186	MDATA Hold Time	1		ns	7-7	Referenced to MCLK
t187	MDATA Valid Delay From MCLK•MBRDY#	2	12	ns	7-6	
t188	MDATA Valid Delay From MCLK•MEOC#	2	20	ns	7-6	
t189	MDATA Valid Delay From MCLK•MSEL#	2	18	ns	7-6	(45)
t190	MDATA Valid Delay From MOCLK	1.5	10	ns	7-6	
Strobed Mode						
t195	MEOC# High Time	8		ns	7-16	(49)
t196	MEOC# Low Time	8		ns	7-16	
t197	MISTB, MOSTB High Time	12		ns	7-16	(49)
t198	MISTB, MOSTB Low Time	12		ns	7-16	
t199	MEOC#, MISTB, MOSTB Rise Time		2	ns		

Table 7-21. 66-MHz 82491 Cache SRAM Memory Bus Interface Timings (Contd.)

V_{CC} = See Note 51, Tcase = See Note 52, C_L = 0 pF						
Symbol	**Parameter**	**Min**	**Max**	**Unit**	**Fig.**	**Notes**
Strobed Mode						
t200	MEOC#, MISTB, MOSTB Fall Time		2	ns		
t201	MSEL# High Time for Restart	8		ns	7-16	
t202	MSEL# Setup Before Transition on MISTB or MOSTB	5		ns	7-12	(49)
t203	MSEL# Hold After Transition on MISTB or MOSTB	10		ns	7-12	
t204	MSEL# Setup Before Transition on MEOC#	5		ns	7-12	
t205	MSEL# Hold After Transition on MEOC#	1		ns	7-12	
t206	MISTB, MOSTB Transition to/from MEOC# Falling Transition	10		ns		
t207	MZBT# Setup To MSEL# or MEOC# Falling Edge	5		ns	7-11	
t208	MZBT# Hold From MSEL# or MEOC# Falling Edge	1		ns	7-11	
t209	MFRZ# Setup To MEOC# Falling Edge	5		ns	7-11	
t210	MFRZ# Hold From MEOC# Falling Edge	1		ns	7-11	
t211	MDATA Setup To MISTB transition or MEOC# Falling Edge	5		ns	7-11	
t212	MDATA Hold From MISTB transition or MEOC# Falling Edge	1		ns	7-11	
t213	MDATA Valid Delay From Transition on MOSTB	2	12	ns	7-13	
t214	MDATA Valid Delay From MEOC# Falling Transition or MSEL# Deactivation	2	20	ns	7-13	

NOTES:

1. Below 66 MHz only functionality is guaranteed, the following equations provide the change in AC specifications required to operate at lower frequencies:

   Pentium® processor: no effect

   82496 Cache Controller: (signals: SET0-10, ADS#, CFA2-6, and TAG0-11)
   Δ setup = 0.57 (Δ cycle time) +/- 0.5ns

   82491 Cache SRAM: no effect

2. High times are measured between 2.0V crossing points.
3. Low times are measured between 0.8V crossing points.

4. Rise and Fall times are measured between 0.8V and 2.0V.
5. APCHK#, FERR#, HLDA, IERR#, and PCHK# are glitch free outputs. Glitch free signals monotonically transition without false transitions (i.e., glitches).
6. TTL input test waveforms are assumed to be 0 to 3 Volt transitions with 1 Volt/ns rise and fall times.
7. Referenced to TCK rising edge.
8. Referenced to TCK falling edge.
9. 1 ns can be added to the maximum TCK rise and fall times for every 10 MHz of frequency below 16 MHz. 1ns must be added to t30 and t36 for every 10 MHz of frequency below 16 MHz.
10. Non-Test Outputs and Inputs are the normal output or input signals (besides TCK, TRST#, TDI, TDO, and TMS). These timings correspond to the response of these signals due to boundary scan operations.
11. FRCMC# should be tied to V_{CC} (high) to ensure proper operation of the Pentium processor as a master Pentium processor.
12. If configuration signals with internal pullup resistors are left floating in the system, RESET pulse width must be at least 10 microseconds.
13. CLK skew between Pentium processor and 82496 Cache Controller assumed to be less than 0.2 ns. CLK skew is measured at 0.8V, 1.5V, and 2.0V of the rising edge of CLK.
14. 0.8 V/ns <= CLK input rise/fall time <= 8 V/ns.
15. 0.3 V/ns <= Input rise/fall time <= 5 V/ns.
16. This input may be driven asynchronously.
17. When driven asynchronously, NMI, FLUSH#, R/S#, INIT, and SMI must be deasserted (inactive) for a minimum of 2 clocks before being returned active.
18. Functionality is guaranteed by design/characterization.
19. Measured on rising edge of adjacent CLKs at 1.5V.
20. To ensure a 1:1 relationship between the magnitude of the input jitter and the internal and external clocks, the jitter frequency spectrum should not have any power spectrum peaking between 500 KHz and 1/3 of the CLK operating frequency. If this occurs, I/O timings are degraded by twice the jitter component within this frequency range. For example, if 15% of the jitter energy is within this range degrade I/O timings by 2 x 0.15 x magnitude of jitter.
21. The amount of jitter present must be accounted for as a component of CLK skew between devices.
22. Setup time is required to guarantee recognition on a specific clock.
23. Hold time is required to guarantee recognition on a specific clock.
24. Only need to meet setup and hold times during the KWEND and SWEND sample times.
25. Valid delay from CLK only if MALE or MBALE, MAOE#, MBAOE# are active.
26. Valid delay from MALE or MBALE going active, if both MAOE# and MBAOE# are active.
27. Valid delay from MAOE#, MBAOE# going active.
28. Float delay from MAOE#, MBAOE# going inactive.
29. In Synchronous mode, referenced to CLK.
30. In Clocked mode, referenced to SNPCLK.
31. In Strobed mode, referenced to SNPSTB# falling edge.
32. In Strobed mode, must meet active/inactive times
34. To guarantee recognition on a given CLK edge.
35. This signal is not used when using the 82496 Cache Controller with the 82491 Cache SRAM.
36. For proper configuration, t70, t71, t72, and t 73 must all be met.
37. Glitch free signals monotonically transition without false transitions (i.e., glitches).
38. 1 ns can be added to maximum SNPCLK rise/fall time for every 10 MHz of frequency below 66 MHz. 1 ns must be added to t123 and t133 for every 10 MHz of frequency below 66 MHz.

39. From CLK in which BLEC# sampled active.
40. Tighter symmetry required since MCLK input does not use a PLL.
41. Timing is referenced to falling edge of RESET.
42. For proper configuration, t150, t151, t152, and t153 must all be met.
43. AC timings assume MALDRV=low on reset. If MALDRV=high on reset, add 0.7 ns to t90, t91, and t92.
44. Must meet MDATA setup to CLK one full CLK before BRDY# active for first transfer on line fills and all non-cacheable transfers.
45. MSEL# sampled inactive resets burst counter. Data is re-driven beginning with data corresponding to first address requested.
46. Not 100% Tested. Guaranteed by design/characterization.
47. Float and Enable times measured at Vcc/2 level at gate of output device are guaranteed by design. (Not 100% tested)
48. CLK Skew between 82491 Cache SRAM and other devices (Pentium processor, 82496 Cache Controller, and other C8Cs) assumed to be less than 0.7 ns.
49. Signal Restrictions
    a. For proper operation the following signals must have monotonic transitions:
       — CLK,
       — MCLK in clocked mode,
       — MISTB, MOSTB, and MEOC# in strobed mode.
    b. For proper operation the following signals must remain stable (must not glitch) throughout a cycle.
       — MDOE#,
       — MSEL#, when active during strobed mode.
50. All TTL timings are referenced from 1.5V.
51. PP V_{CC} = 4.90V to 5.40V; CC, CS V_{CC} = 5V ± 5%
52. PP T_{CASE} = 0°C to +70°C; CC, CS T_{CASE} = 0°C to +85°C

7.6.2.2. 60-MHz AC SPECIFICATIONS

Table 7-22. 60-MHz CPU Cache Chip Set Common Timings

V_{CC} = 5 V ± 5%, Tcase = See Note 51, C_L = 0 pF						
Symbol	**Parameter**	**Min**	**Max**	**Unit**	**Fig.**	**Notes**
t1	CLK Frequency	33.33	60	MHz		1X clock, (1), (49)
t2	CLK Period	16.67	30	ns	7-5	
t3	CLK High Time	4		ns	7-5	(2)
t4	CLK Low Time	4		ns	7-5	(3)
t5	CLK Rise Time	0.15	1.5	ns	7-5	(4)
t6	CLK Fall Time	0.15	1.5	ns	7-5	(4)
t7	CLK Stability		+/- 250	pS		(18), (19), (20), (21)
t8	RESET, INIT Setup Time	5.5		ns	7-9	To guarantee recognition on a given CLK edge. (16), (17)
t9	RESET, INIT Hold Time	1.5		ns	7-9	To guarantee recognition on a given CLK edge.
t10	RESET Pulse Width, CLK and V_{CC} Stable	15		CLKs	7-9	(11), (17)
t11	INIT Pulse Width, Async.	2		CLKs		To guarantee asynchronous recognition.
t13	RESET Active After CLK and V_{CC} Stable	1		ms	7-9	Power Up (11), (12)
t20	TCK Frequency	—	16	MHz		
t21	TCK Period	62.5		ns	7-5	
t22	TCK High Time	25		ns	7-5	(2)
t23	TCK Low Time	25		ns	7-5	(3)
t24	TCK Rise Time		5	ns	7-5	(9), (4)
t25	TCK Fall Time		5	ns	7-5	(9), (4)
t28	TRST# Pulse Width	40		ns	7-15	(46), Asynchronous
t29	TDI, TMS Setup Time	5		ns	7-14	(7)

Table 7-22 60-MHz CPU Cache Chip Set Common Timings (Contd.)

V_{CC} = 5 V ± 5%, Tcase = See Note 51, C_L = 0 pF						
Symbol	**Parameter**	**Min**	**Max**	**Unit**	**Fig.**	**Notes**
t30	TDI, TMS Hold Time	13		ns	7-14	(7)
t31	TDO Valid Delay	3	20	ns	7-14	(8)
t32	TDO Float Delay		25	ns	7-14	(8), (46)
t33	All Non-Test Outputs Valid Delay	3	20	ns	7-14	(8), (10)
t34	All Non-Test Outputs Float Delay		25	ns	7-14	(8), (10), (46)
t35	All Non-Test Inputs Setup Time	5		ns	7-14	(7), (8)
t36	All Non-Test Inputs Hold Time	13		ns	7-14	(7), (8)

Table 7-23. 60-MHz Pentium® Processor Memory Bus Interface Timings

Legend: PP=Pentium® Processor, CC=82496 Cache Controller, CS=82491 Cache SRAM

V_{CC} = 5 V ± 5%, Tcase = See Note 51, C_L = 0 pF						
Symbol	**Parameter**	**Min**	**Max**	**Unit**	**Fig.**	**Notes**
t40	PP reset configurations Setup Time	5.5		ns	7-9	
t41	PP reset configurations Hold Time	1.5		ns	7-9	
t42	PP reset configurations Setup Time Referenced to Falling Edge of RESET	2		CLKs	7-9	
t43	PP reset configurations Hold Time Reference to Falling Edge of RESET	2		CLKs	7-9	
t50	HLDA Valid Delay	1.5	9	ns	7-6	(5)
t51	BREQ Valid Delay	1.5	9	ns	7-6	
t52	PCHK#, APCHK#, FERR#, IERR# Valid Delay	1.5	9.3	ns	7-6	(5)
t53	IU, IV, IBT Valid Delay	1.5	11	ns	7-6	
t54	BP0-3, PM0-1 Valid Delay	1.5	11	ns	7-6	
t55	A20M#, FLUSH#, IGNNE#, NMI, INTR, Setup Time	5.5		ns	7-7	(16), (17)
t56	A20M#, FLUSH#, IGNNE#, NMI, INTR, Hold Time	1.5		ns	7-7	
t57	FLUSH#, IGNNE#, NMI, Pulse Width, Async	2		CLKs		(17)
t58	PEN#, BUSCHK# Setup Time	5.5		ns	7-7	
t59	PEN#, BUSCHK# Hold Time	1.5		ns	7-7	
t60	HOLD Setup Time	5.5		ns	7-7	
t61	HOLD Hold Time	1.5		ns	7-7	
t62	BRDY# Setup Time	5.5		ns	7-7	
t63	BRDY# Hold Time	1.5		ns	7-7	
t64	R/S#, SMI# Setup Time	5.5		ns	7-7	(16), (17)
t65	R/S#, SMI# Hold Time	1.5		ns	7-7	
t66	R/S#, SMI# Pulse Width, Async	2		CLKs		(17)
t67	PRDY, SMIACT# Valid Delay	1.5	9	ns	7-6	

Table 7-24. 60-MHz 82496 Cache Controller Memory Bus Interface Timings

V_{CC} = 5 V ± 5%, Tcase = See Note 51, C_L = 0 pF						
Symbol	**Parameter**	**Min**	**Max**	**Unit**	**Fig.**	**Notes**
t70	CFG0-2, CLDRV, HIGHZ#, MALDRV, SLFTST#, SNPMD, WWOR#, FLUSH#[V_{CC}] Setup Time	6.5		ns	7-9	(12), (22), (36)
t71	CFG0-2, CLDRV, HIGHZ#, MALDRV, SLFTST#, SNPMD, WWOR#, FLUSH#[V_{CC}] Hold Time	1		ns	7-9	(12), (23), (36)
t72	CFG0-2, CLDRV, HIGHZ#, MALDRV, SLFTST#, SNPMD, WWOR#, FLUSH#[V_{CC}] Setup Time Referenced to Falling Edge of RESET	10		CLKs	7-9	(12), (36)
t73	CFG0-2, CLDRV, HIGHZ#, MALDRV, SLFTST#, SNPMD, WWOR#, FLUSH#[V_{CC}] Hold Time Referenced to Falling Edge of RESET	0		CLKs	7-9	(12), (36)
t75	FLUSH#, SYNC# Setup Time	6.5		ns	7-7	(34)
t76	FLUSH#, SYNC#, Hold Time	1		ns	7-7	(34)
t77	FLUSH#, SYNC#, Pulse Width, Async	2		CLKs		
t80	CADS#, CDTS# Valid Delay	1.5	9.2	ns	7-6	Glitch Free
t81	KLOCK#, MCACHE#, RDYSRC Valid Delay	1.5	9.2	ns	7-6	KLOCK# is Glitch Free
t82	CW/R#, CD/C#, CMI/O# Valid Delay	1.5	9.2	ns	7-6	
t83	CPWT, CPCD, CCACHE#, CSCYC Valid Delay	1.5	9.2	ns	7-6	
t84	CAHOLD, CWAY, PALLC# Valid Delay	1.5	9.2	ns	7-6	
t85	FSIOUT# Valid Delay	1.5	9.2	ns	7-6	
t86	NENE#, SMLN# Valid Delay	1.5	13	ns	7-6	
t87	APERR#, IPERR#, MAPERR# Valid Delay	1.5	9.2	ns	7-6	Glitch Free
t88	APIC# Valid Delay	1.5	13	ns	7-6	
t89	BLE# Valid Delay	1.5	9.2	ns	7-6	(35)

Table 7-24. 60-MHz 82496 Cache Controller Memory Bus Interface Timings (Contd.)

V_{CC} = 5 V ± 5%, Tcase = See Note 51, C_L = 0 pF						
Symbol	**Parameter**	**Min**	**Max**	**Unit**	**Fig.**	**Notes**
t90	MCFA0-6, MSET0-10, MTAG0-11, MAP, MBT0-3 Valid Delay	1.5	12	ns	7-6	(25), (43)
t91	MCFA0-6, MSET0-10, MTAG0-11, MAP, MBT0-3 Valid Delay	1.5	12	ns	7-10	(26), (43)
t92	MCFA0-6, MSET0-10, MTAG0-11, MAP, MBT0-3 Valid Delay	1.5	11	ns	7-10	(27), (43)
t93	MCFA0-6, MSET0-10, MTAG0-11, MAP, MBT0-3 Float Delay		12	ns	7-10	(28), (46)
t95	BRDY# Setup Time	6.75		ns	7-7	
t95a	CRDY# Setup Time	7.5		ns	7-7	
t96	BRDY#, CRDY# Hold Time	1		ns	7-7	
t97	BGT#, CNA#, KWEND#, SWEND# Setup Time	6.5		ns	7-7	
t98	BGT#, CNA#, KWEND#, SWEND# Hold Time	1		ns	7-7	
t100	DRCTM#, MRO#, MWB/WT# Setup Time	6.5		ns	7-7	(24)
t100a	MKEN# Setup Time	6.75		ns	7-7	(24)
t101	DRCTM#, MKEN#, MRO#, MWB/WT# Hold Time	1		ns	7-7	(24)
t110	SNPCLK Frequency	8.3	60	MHz		1X clock
t111	SNPCLK Period	16.67	120	ns	7-5	
t112	SNPCLK High Time	4		ns	7-5	
t113	SNPCLK Low Time	4		ns	7-5	
t114	SNPCLK Rise Time		1.5	ns	7-5	(38)
t115	SNPCLK Fall Time		1.5	ns	7-5	(38)
t118	SNPADS#, SNPCYC# Valid Delay	1.5	9.2	ns	7-6	Glitch Free.

Table 7-24. 60-MHz 82496 Cache Controller Memory Bus Interface Timings (Contd.)

V_{CC} = 5 V ± 5%, Tcase = See Note 51, C_L = 0 pF						
Symbol	**Parameter**	**Min**	**Max**	**Unit**	**Fig.**	**Notes**
t120	MCFA0-6, MSET0-10, MTAG0-11, MAP, MBT0-3 Setup Time	6.5		ns	7-7	(29)
t121	MCFA0-6, MSET0-10, MTAG0-11, MAP, MBT0-3 Hold Time	1		ns	7-7	(29)
t122	MCFA0-6, MSET0-10, MTAG0-11, MAP, MBT0-3 Setup Time	6.5		ns	7-7	(30)
t123	MCFA0-6, MSET0-10, MTAG0-11, MAP, MBT0-3 Hold Time	1		ns	7-7	(30)
t124	MCFA0-6, MSET0-10, MTAG0-11, MAP, MBT0-3 Setup Time	1		ns	7-8	(31)
t125	MCFA0-6, MSET0-10, MTAG0-11, MAP, MBT0-3 Hold Time	6.5		ns	7-8	(31)
t130	MAOE#, MBAOE#, SNPINV, SNPNCA Setup Time	6.5		ns	7-7	(29)
t131	MAOE#, MBAOE#, SNPINV, SNPNCA Hold Time	1		ns	7-7	(29)
t132	MAOE#, MBAOE#, SNPINV, SNPNCA Setup Time	6.5		ns	7-7	(30)
t133	MAOE#, MBAOE#, SNPINV, SNPNCA Hold Time	1		ns	7-7	(30)
t134	MAOE#, MBAOE#, SNPINV, SNPNCA Setup Time	1		ns	7-8	(31)
t135	MAOE#, MBAOE#, SNPINV, SNPNCA Hold Time	6.5		ns	7-8	(31)
t140	SNPSTB# Setup Time	6.5		ns	7-7	(29)
t141	SNPSTB# Hold Time	1		ns	7-7	(29)
t142	SNPSTB# Setup Time	6.5		ns	7-7	(30)
t143	SNPSTB# Hold Time	1		ns	7-7	(30)
t144	SNPSTB# Active Time	6.5		ns	7-16	(32)
t145	SNPSTB# Inactive Time	6.5		ns	7-16	(32)
t148	MHITM#, MTHIT#, SNPBSY# Valid Delay	1.5	11	ns	7-6	

Table 7-25. 60-MHz 82491 Cache SRAM Memory Bus Interface Timings

V_{CC} = 5 V ± 5%, Tcase = See Note 51, C_L = 0 pF						
Symbol	**Parameter**	**Min**	**Max**	**Unit**	**Fig.**	**Notes**
t150	MDLDRV, MSTBM, MTR4/8#, MX4/8#, PAR# Setup Time	5.5		ns	7-9	(22), (42)
t151	MDLDRV, MSTBM, MTR4/8#, MX4/8#, PAR# Hold Time	1		ns	7-9	(23), (42)
t152	MDLDRV, MSTBM, MTR4/8#, MX4/8#, PAR# Setup Time Referenced to Falling Edge of RESET	4		CLKs	7-9	(41), (42)
t153	MDLDRV, MSTBM, MTR4/8#, MX4/8#, PAR# Hold Time Referenced to Falling Edge of RESET	0		CLKs	7-9	(41), (42)
t155	BRDY#, CRDY# Setup Time	5.5		ns	7-7	
t156	BRDY#, CRDY# Hold Time	1		ns	7-7	
t160	MDATA Setup to CLK (CLK before BRDY# Active)	5.5		ns	7-7	(44)
t161	MDATA Valid Delay From CLK (CLK from CDTS# Valid, MDOE# Active)		13	ns	7-6	(49)
t162	MDATA Valid Delay From MDOE# Active		8	ns	7-10	
t163	MDATA Float Delay From MDOE# Inactive		11	ns	7-10	
t165	MBE# Valid Delay	1.5	9	ns	7-6	(39)
Clocked Mode						
t170	MCLK, MOCLK Frequency		60	MHz		1X clock, (49)
t171	MCLK, MOCLK Period	16.67		ns	7-5	
t172	MOCLK High Time	4		ns	7-5	
t173	MOCLK Low Time	4		ns	7-5	
t174	MCLK High Time	5		ns	7-5	(40)
t175	MCLK Low Time	5		ns	7-5	(40)
t176	MCLK, MOCLK Rise Time		1.5	ns	7-5	
t177	MCLK, MOCLK Fall Time		1.5	ns	7-5	

Table 7-25. 60-MHz 82491 Cache SRAM Memory Bus Interface Timings (Contd.)

V_{CC} = 5 V ± 5%, Tcase = See Note 51, C_L = 0 pF						
Symbol	**Parameter**	**Min**	**Max**	**Unit**	**Fig.**	**Notes**
Clocked Mode						
t180	MOCLK Falling Edge To MCLK Rising Edge	2		ns		
t181	MFRZ#, MZBT# Setup Time	5		ns	7-7	Referenced to MCLK
t182	MFRZ#, MZBT# Hold Time	1		ns	7-7	Referenced to MCLK
t183	MBRDY#, MSEL#, MEOC# Setup Time	5		ns	7-7	Referenced to MCLK
t184	MBRDY#, MSEL#, MEOC# Hold Time	1		ns	7-7	Referenced to MCLK
t185	MDATA Setup Time	5		ns	7-7	Referenced to MCLK
t186	MDATA Hold Time	1		ns	7-7	Referenced to MCLK
t187	MDATA Valid Delay From MCLK•MBRDY#	2	13	ns	7-6	
t188	MDATA Valid Delay From MCLK•MEOC#	2	20	ns	7-6	
t189	MDATA Valid Delay From MCLK•MSEL#	2	18	ns	7-6	(45)
t190	MDATA Valid Delay From MOCLK	1.5	10	ns	7-6	

Table 7-25. 60-MHz 82491 Cache SRAM Memory Bus Interface Timings (Contd.)

V_{CC} = 5 V ± 5%, Tcase = See Note 51, C_L = 0 pF						
Symbol	**Parameter**	**Min**	**Max**	**Unit**	**Fig.**	**Notes**
Strobed Mode						
t195	MEOC# High Time	8		ns	7-16	(49)
t196	MEOC# Low Time	8		ns	7-16	
t197	MISTB, MOSTB High Time	12		ns	7-16	(49)
t198	MISTB, MOSTB Low Time	12		ns	7-16	
t199	MEOC#, MISTB, MOSTB Rise Time		2	ns		
t200	MEOC#, MISTB, MOSTB Fall Time		2	ns		
t201	MSEL# High Time for Restart	8		ns	7-16	
t202	MSEL# Setup Before Transition on MISTB or MOSTB	5		ns	7-12	(49)
t203	MSEL# Hold After Transition on MISTB or MOSTB	10		ns	7-12	
t204	MSEL# Setup Before Transition on MEOC#	5		ns	7-12	
t205	MSEL# Hold After Transition on MEOC#	1		ns	7-12	
t206	MISTB, MOSTB Transition to/from MEOC# Falling Transition	10		ns		
t207	MZBT# Setup To MSEL# or MEOC# Falling Edge	5		ns	7-11	
t208	MZBT# Hold From MSEL# or MEOC# Falling Edge	1		ns	7-11	
t209	MFRZ# Setup To MEOC# Falling Edge	5		ns	7-11	
t210	MFRZ# Hold From MEOC# Falling Edge	1		ns	7-11	
t211	MDATA Setup To MISTB transition or MEOC# Falling Edge	5		ns	7-11	
t212	MDATA Hold From MISTB transition or MEOC# Falling Edge	1		ns	7-11	
t213	MDATA Valid Delay From Transition on MOSTB	2	12	ns	7-13	
t214	MDATA Valid Delay From MEOC# Falling Transition or MSEL# Deactivation	2	20	ns	7-13	

NOTES:

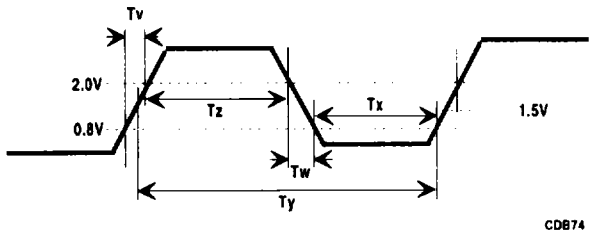
1. Below 60 MHz only functionality is guaranteed, the following equations provide the change in AC specifications required to operate at lower frequencies:

   Pentium® processor: no effect

   82496 Cache Controller: (signals: SET0-10, ADS#, CFA2-6, and TAG0-11)
   Δ setup = 0.57 (Δ cycle time) +/- 0.5ns

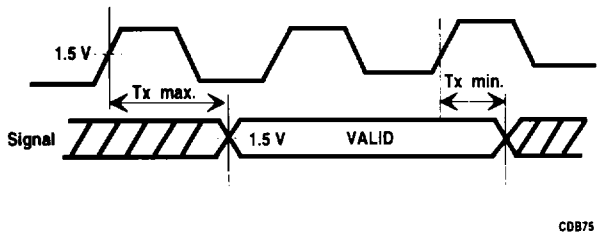
   82491 Cache SRAM: no effect
2. High times are measured between 2.0V crossing points.
3. Low times are measured between 0.8V crossing points.
4. Rise and Fall times are measured between 0.8V and 2.0V.
5. APCHK#, FERR#, HLDA, IERR#, and PCHK# are glitch free outputs. Glitch free signals monotonically transition without false transitions (i.e., glitches).
6. TTL input test waveforms are assumed to be 0 to 3 Volt transitions with 1 Volt/ns rise and fall times.
7. Referenced to TCK rising edge.
8. Referenced to TCK falling edge.
9. 1ns can be added to the maximum TCK rise and fall times for every 10 MHz of frequency below 16 MHz. 1 ns must be added to t30 and t36 for every 10 MHz of frequency below 16 MHz.
10. Non-Test Outputs and Inputs are the normal output or input signals (besides TCK, TRST#, TDI, TDO, and TMS). These timings correspond to the response of these signals due to boundary scan operations.
11. FRCMC# should be tied to V_{CC} (high) to ensure proper operation of the Pentium processor as a master Pentium processor.
12. If configuration signals with internal pullup resistors are left floating in the system, RESET pulse width must be at least 10 microseconds.
13. CLK skew between Pentium processor and 82496 Cache Controller assumed to be less than 0.2 ns. CLK skew is measured at 0.8V, 1.5V, and 2.0V of the rising edge of CLK.
14. 0.8 V/ns <= CLK input rise/fall time <= 8 V/ns.
15. 0.3 V/ns <= Input rise/fall time <= 5 V/ns.
16. This input may be driven asynchronously.
17. When driven asynchronously, NMI, FLUSH#, R/S#, INIT, and SMI must be deasserted (inactive) for a minimum of 2 clocks before being returned active.
18. Functionality is guaranteed by design/characterization.
19. Measured on rising edge of adjacent CLKs at 1.5V.
20. To ensure a 1:1 relationship between the magnitude of the input jitter and the internal and external clocks, the jitter frequency spectrum should not have any power spectrum peaking between 500 KHz and 1/3 of the CLK operating frequency. If this occurs, I/O timings are degraded by twice the jitter component within this frequency range. For example, if 15% of the jitter energy is within this range degrade I/O timings by 2 x 0.15 x magnitude of jitter.
21. The amount of jitter present must be accounted for as a component of CLK skew between devices.
22. Setup time is required to guarantee recognition on a specific clock.
23. Hold time is required to guarantee recognition on a specific clock.
24. Only need to meet setup and hold times during the KWEND and SWEND sample times.
25. Valid delay from CLK only if MALE or MBALE, MAOE#, MBAOE# are active.
26. Valid delay from MALE or MBALE going active, if both MAOE# and MBAOE# are active.
27. Valid delay from MAOE#, MBAOE# going active.
28. Float delay from MAOE#, MBAOE# going inactive.
29. In Synchronous mode, referenced to CLK.

30. In Clocked mode, referenced to SNPCLK.
31. In Strobed mode, referenced to SNPSTB# falling edge.
32. In Strobed mode, must meet active/inactive times.
34. To guarantee recognition on a given CLK edge.
35. This signal is not used when using the 82496 Cache Controller with the 82491 Cache SRAM.
36. For proper configuration, t70, t71, t72, and t 73 must all be met.
37. Glitch free signals monotonically transition without false transitions (i.e., glitches).
38. 1 ns can be added to maximum SNPCLK rise/fall time for every 10 MHz of frequency below 60 MHz. 1 ns must be added to t123 and t133 for every 10 MHz of frequency below 60 MHz.
39. From CLK in which BLEC# sampled active.
40. Tighter symmetry required since MCLK input does not use a PLL.
41. Timing is referenced to falling edge of RESET.
42. For proper configuration, t150, t151, t152, and t153 must all be met.
43. AC timings assume MALDRV=low on reset. If MALDRV=high on reset, add 0.7 ns to t90, t91, and t92.
44. Must meet MDATA setup to CLK one full CLK before BRDY# active for first transfer on line fills and all non-cacheable transfers.
45. MSEL# sampled inactive resets burst counter. Data is re-driven beginning with data corresponding to first address requested.
46. Not 100% Tested. Guaranteed by design/characterization.
47. Float and Enable times measured at Vcc/2 level at gate of output device are guaranteed by design. (Not 100% tested)
48. CLK Skew between 82491 Cache SRAM and other devices (Pentium processor, 82496 Cache Controller, and other C8Cs) assumed to be less than 0.7 ns.
49. Signal Restrictions
    a. For proper operation the following signals must have monotonic transitions:
       — CLK,
       — MCLK in clocked mode,
       — MISTB, MOSTB, and MEOC# in strobed mode.
    b. For proper operation the following signals must remain stable (must not glitch) throughout a cycle.
       — MDOE#,
       — MSEL#, when active during strobed mode.
50. All TTL timings are referenced from 1.5V.
51. PP T_{CASE} = 0°C to +80°C; CC, CS T_{CASE} = 0°C to +85°C



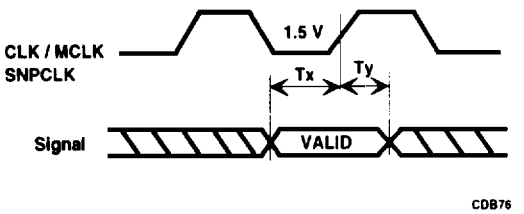
Tv = t5, t24, t114, t176
Tw = t6, t25, t115, t177
Tx = t4, t23, t113, t173, t175
Ty = t2, t20, t111, t171
Tz = t3, t22, t112, t172, t174

Figure 7-5. Clock Waveform



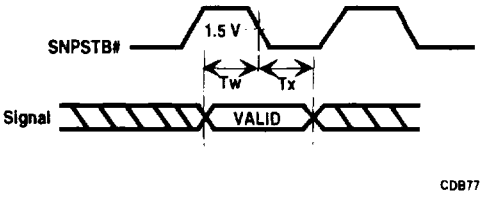
Tx = t50-t54, t67, t80-90, t118, t148, t161, t165, t187-190

Figure 7-6. Valid Delay Timings



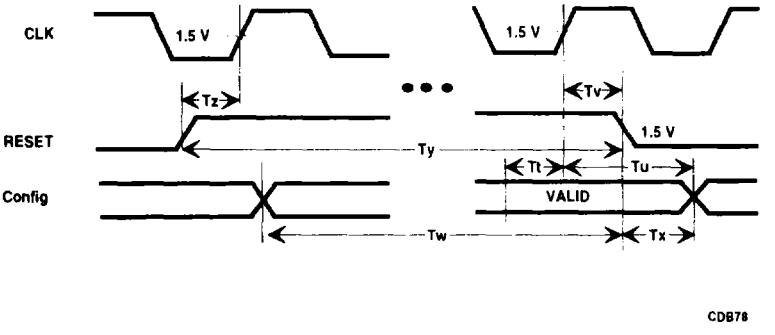
Tx = t55, t58, t60, t62, t64, t75, t95, t97, t100, t120, t122, t130, t132, t140, t155, t160, t181, t183, t185
Ty = t56, t59, t61, t63, t65, t76, t96, t98, t101, t121, t123, t131, t133, t141, t143, t156, t182, t184, t186

Figure 7-7. Setup and Hold Timings



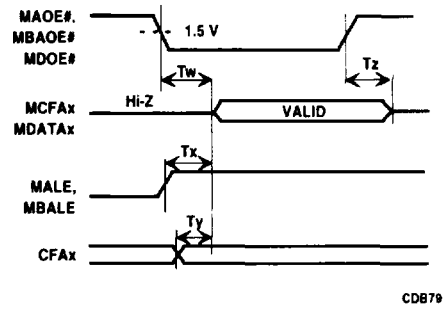
Tw = t124, t134
Tx = t125, t135

Figure 7-8. Setup and Hold Timings in Strobed Snooping Mode



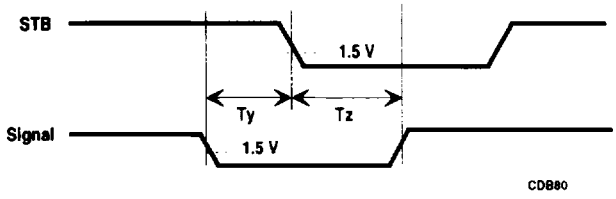
Tt = t40, t70, t150
Tu = t41, t71, t151
Tv = t9
Tw = t42, t72, t1152
Tx = t43, t73, t1153
Ty = t10, t13
Tz = t8

Figure 7-9. Reset and Configuration Timings



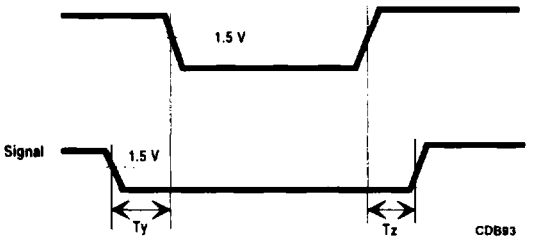
Tw = t92, t162
Tx = t91
Ty =
Tz = t93, t163

Figure 7-10. Memory Interface Timings



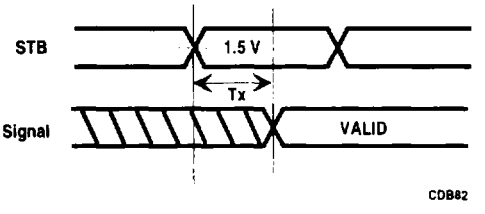
Ty = t207, t209, t211
Tz = t208, t210, t212

Figure 7-11. Setup and Hold Timings to Strobes



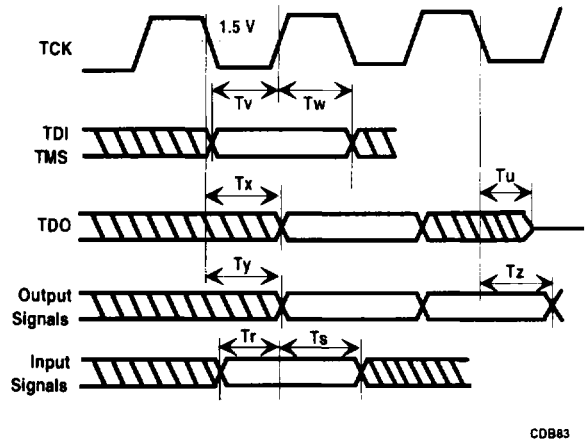
Ty = t202, t204
Tz = t203, t205

Figure 7-12. Setup and Hold Timings M_XST



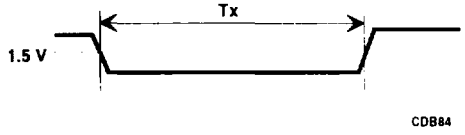
Tx = t213, t214

Figure 7-13. Valid Delay Timings from Strobes



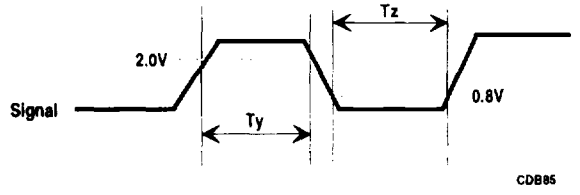
Tr = t35
Ts = t36
Tu = t32
Tv = t29
Tw = t30
Tx = t31
Ty = t33
Tz = t34

Figure 7-14. Test Timings



Tx = t28

Figure 7-15. Test Reset Timings



Ty = t145, t195, t197, t201
Tz = t144, t196, t198

Figure 7-16. Active/Inactive Timings

Each valid delay is specified for a 0 pF load. The system designer should use I/O buffer modeling to account for signal flight time delays. Table 7-26 lists the buffer type to be used for each signal in the external interface.

Table 7-26. External Interface Signal Buffer Assignment

Legend: PP=Pentium® Processor, CC=82496 Cache Controller, CS=82491 Cache SRAM

Device	Signals	Type	Driver Buffer Type	Receiver Buffer Type
PP	A20M#, FLUSH#, FRCMC#, HOLD, IGNNE#, INIT, INTR, NMI, PEN#, R/S#, RESET, SMI#, TDI, TMS,	I	N/A	ER1
	BRDY#, BUSCHK#, TRST#	I	N/A	ER2
	CLK	I	N/A	ER3
	TCK	I	N/A	ER4
	APCHK#, BP3-0#, PM1, PM0, FERR#, HLDA, IBT, IERR#, IU, IV, PCHK#, PRDY, SMIACT#, TDO	O	ED1	N/A
CC	BRDY#, CNA#, FLUSH#, MALE, MAOE#, MBALE, MBAOE#, MKEN#, RESET, SNPCLK, SNPINV, SNPNCA, SNPSTB#, SWEND#, SYNC#, TCK, TDI, TMS, TRST#	I	N/A	ER5
	BGT#, CRDY#, KWEND#	I	N/A	ER6
	DRCTM#, MRO#, MWB/WT#	I	N/A	ER7
	CLK	I	N/A	ER8
	MAP (IN: MAOE#=1, OUT: MAOE#=0) MCFA6:0, MSET10:0, MTAG11:0 , MBT3:0 (IN:MAOE#/MBAOE#=1, OUT: MAOE#/MBAOE#=0) For MALDRV = 1 For MALDRV = 0	I/O	 ED2 ED3	 ER9 ER9
	APERR#, APIC#, BLE#, CADS#, CAHOLD, CCACHE#, CD/C#, CM/IO#, CPCD, CPWT, CSCYC, CW/R#, FSIOUT#, IPERR#, KLOCK#, MAPERR#, MCACHE#, PALLC#, RDYSRC, SNPADS#,SNPCYC#,TDO	O	ED4	N/A
	CWAY	O	ED4'	N/A
	CDTS#, MHITM#, MTHIT#, NENE#, SMLN#, SNPBSY#	O	ED5	N/A
CS	BRDY#, CRDY#, MBRDY#(MISTB), MCLK, MDOE#, MEOC#, MFRZ#, MOCLK(MOSTB), MSEL#, MZBT#, RESET, TCK, TDI, TMS	I	N/A	ER10
	MBE#	I/O	ED6	ER10'
	MDATA7-0(IN: READ CYCLE, OUT: WRITE CYCLE) For MDLDRV = 1 For MDLDRV = 0	I/O	 ED7 ED8	 ER12 ER12
	TDO	O	ED6	N/A
	CLK	I	N/A	ER11

7.7. OVERSHOOT/UNDERSHOOT GUIDELINES

The overshoot/undershoot guideline is provided to limit signals transitioning beyond V_{CC} or V_{SS} due to the fast signal switching at these frequencies. Excessive ringback is the dominant harmful effect resulting from overshoot/undershoot.

Overshoot (Undershoot) is the absolute value of the maximum voltage above V_{CC} (below V_{SS}). The guideline assumes the absence of diodes on the input. This guideline should be used in simulations, without the diodes present, to ensure overshoot (undershoot) is within the acceptable range.

Maximum Overshoot/Undershoot on Inputs = 1.6 Volts
(without diodes)

Ringback is the absolute value of the maximum voltage at the receiving pin below V_{CC} (or above V_{SS}) relative to V_{CC} (or V_{SS}) level after the signal has reached its maximum voltage level. The input diodes are assumed present. This guideline is provided to allow system designers to verify, in an actual system, the decisions made based on simulation using the overshoot (undershoot) guideline. Ringback only applies if the signal crossed above V_{CC} (below V_{SS}).

Maximum Ringback on Inputs = 0.8 Volts
(with diodes)

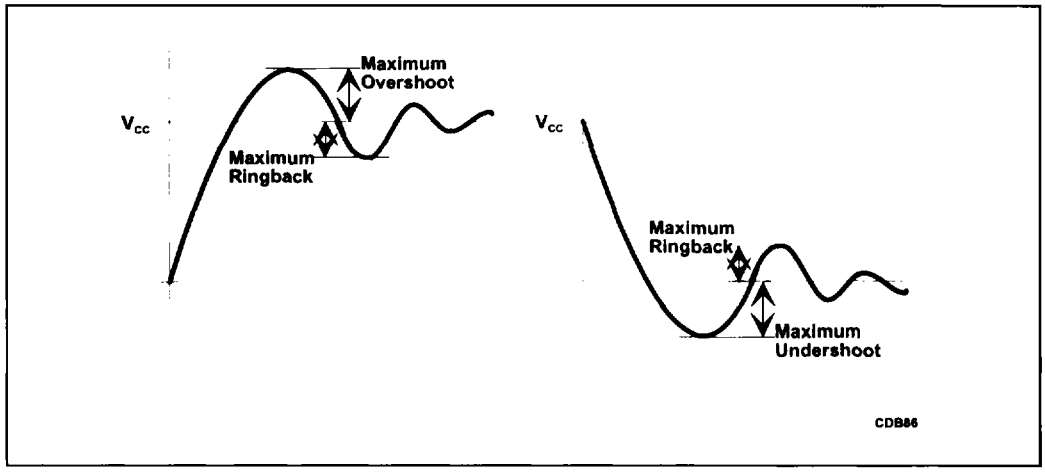


Figure 7-17. Overshoot/Undershoot and Ringback Guidelines