

**PDSP1610**

**MULTIPRECISION MULTIPLIER-ACCUMULATOR**

(SUPERSEDES DECEMBER 1986 EDITION)

The PDSP1610 is a high speed CMOS Multiply Accumulator with on-chip Register File, Shifter and Feedback Paths that allow DSP algorithms to be executed internally. The PDSP1610 performs 16 x 24 Multiply Accumulate operations, accumulating across 48 bits in 100ns. In common with the rest of the PDSP1600 Family, the PDSP1610 supports Multicycle Multiprecision operation allowing 24 x 32 or larger Multiply-Accumulates.

**FEATURES**

- 16 x 24 Multiply Array
- Independent 32-Function ALU
- Dual 48-bit Accumulator Registers
- 8 x 32-bit or 16 x 16-bit Register File
- Funnel Shifter
- Three Port Structure - No I/O Bottle Neck
- Multiprecision Operation; e.g. 200ns 24 x 32
- Block Floating Point Support
- 2 micron CMOS
- 500mW Maximum Power Dissipation

**APPLICATIONS**

- Digital Signal Processing
- Medical Processing
- Array Processing
- High Speed Arithmetic Processors

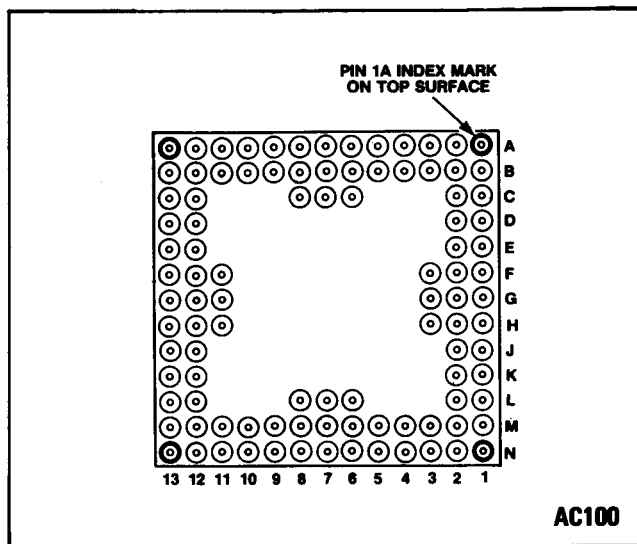


Fig.1 Pin connections - bottom view

**ASSOCIATED PRODUCTS**

- PDSP1601** Arithmetic Logic Unit
- PDSP1640** 40MHz Address Generator

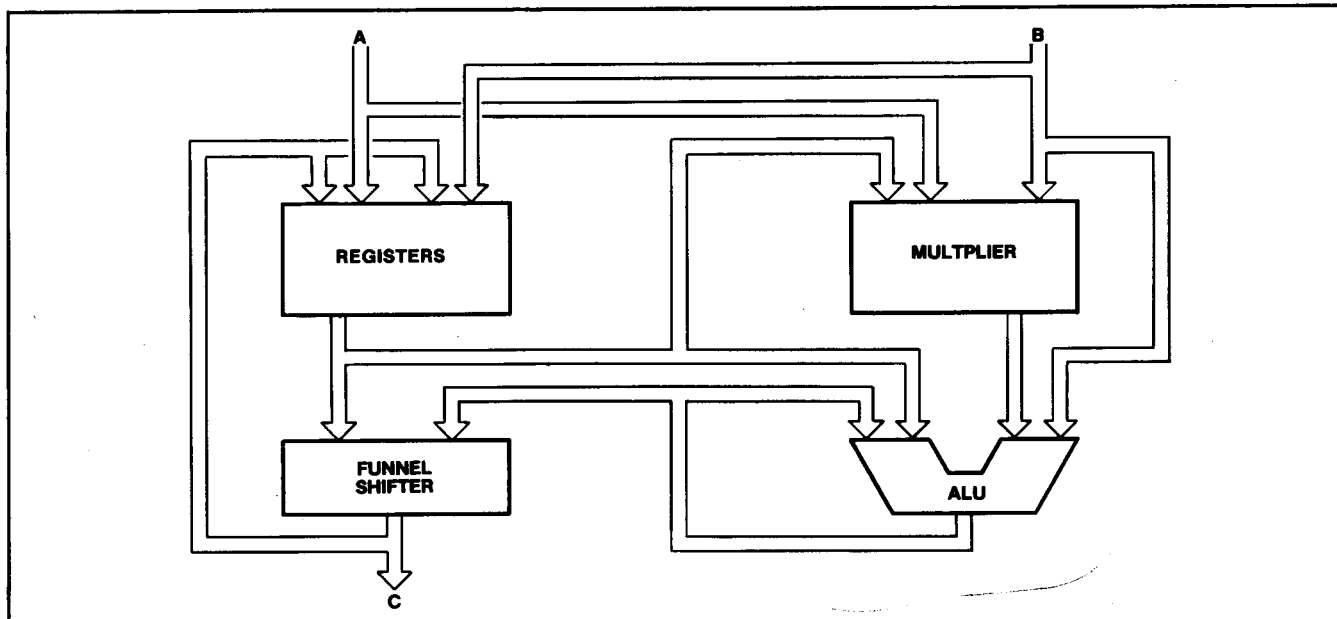


Fig.2 Simplified block diagram

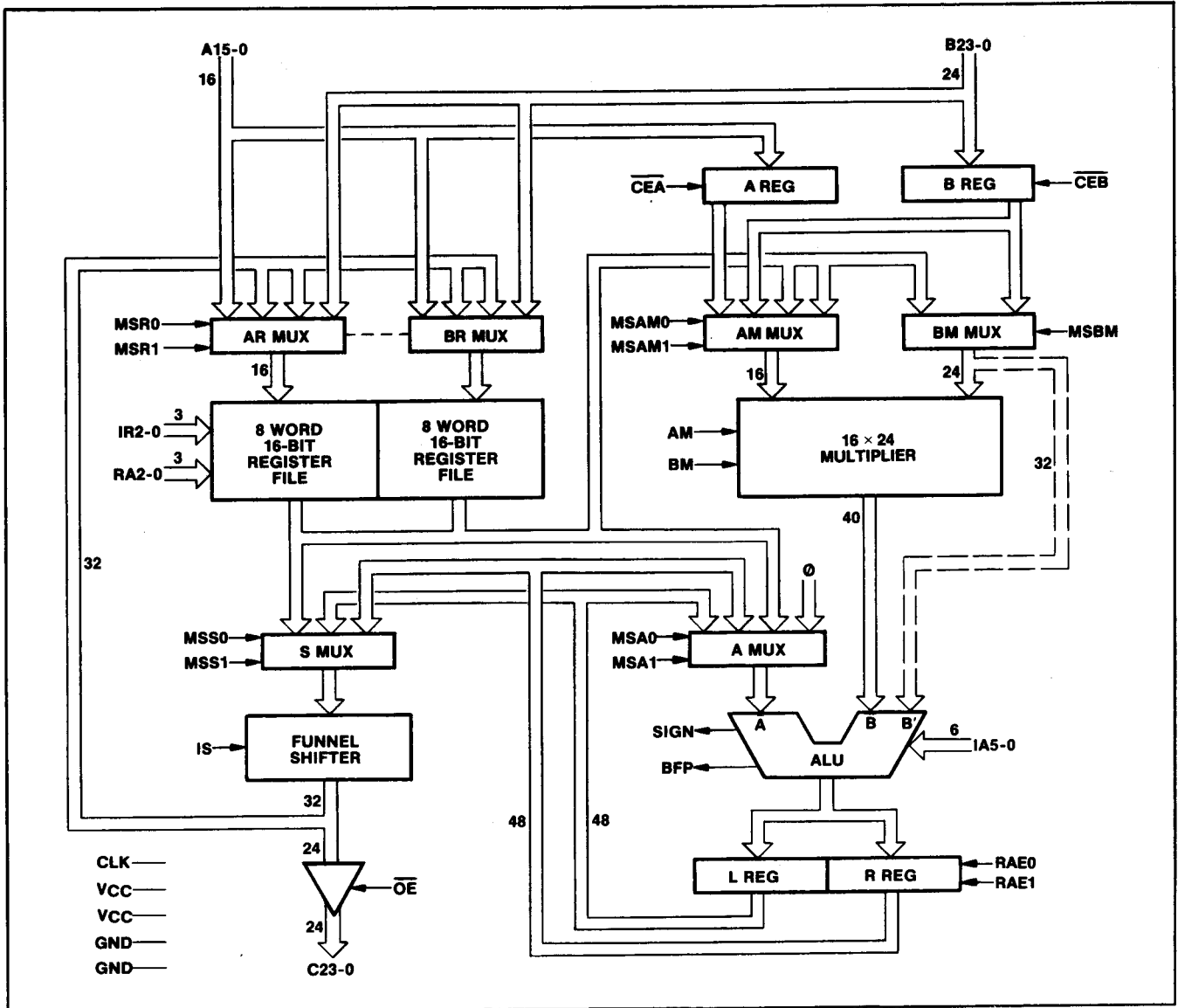


Fig.3 PDSP1610 block diagram

## PIN FUNCTIONS

Signal	Type	Description
CLK	Input	Clock, all operations are initiated by a rising edge of CLK
$\overline{CEA}$	Input	Clock enable A register
$\overline{CEB}$	Input	Clock enable B register
A15-0	Input	16-bit input to device
B23-0	Input	24-bit input to device
C23-0	Output	24-bit output from device
$\overline{OE}$	Input	Output enable (active low)
MSR1-0	Input	Register file input mux control
RA2-0	Input	Register file read control
IR2-0	Input	Register file write instructions
MSS1-0	Input	Funnel shifter input mux control
IS	Input	Funnel shifter control
MSAM1-0	Input	Multiplier A input mux control
MSBM	Input	Multiplier B input mux control
AM	Input	Multiplier A input signed/unsigned control
BM	Input	Multiplier B input signed/unsigned control
MSA1-0	Input	ALU A mux control
IA5-0	Input	ALU instruction
RAE1-0	Input	ALU accumulator register load enables
SIGN	Output	Sign bit output from ALU
BFP	Output	Flag output from ALU
V <sub>cc</sub>	Power	+5V supply. Both V <sub>cc</sub> pins must be connected.
GND	Ground	0V supply. Both GND pins must be connected.

## ALU INSTRUCTIONS

Other IA codes are reserved for preprogrammed instructions.

IA5-0	Description	IA5-0	Description
00 0000	A plus B	01 0000	A plus B'
00 0001	A/2 plus B	01 0001	A minus B'
00 0010	A/2 <sup>16</sup> plus B	01 0010	B' minus A
00 0011	A plus 2B	01 0011	A
00 0100	A minus B	01 0100	minus A
00 0101	A/2 minus B	01 0101	A ÷ 2
00 0110	A/2 <sup>16</sup> minus B	01 0110	2A
00 0111	A minus 2B	01 0111	B'
00 1000	B minus A	01 1000	A and B'
00 1001	B minus A/2	01 1001	A or B'
00 1010	B minus A/2 <sup>16</sup>	01 1010	A exor B'
00 1011	2B minus A	01 1011	A/2 plus B'
00 1100	A/2 <sup>16</sup> plus 2B	01 1100	Set BFP OVR
00 1101	A/2 <sup>16</sup> plus B/2	01 1101	Set BFP UND1
00 1110	Reserved	01 1110	Set BFP UND2
00 1111	Clr Acc Reg's	01 1111	Set BFP ZERO

## FUNCTIONAL DESCRIPTION

The PDSP1610 is a high speed variable precision Multiply Accumulator containing independent Multiplier and ALU, together with a Funnel Shifter and Register File and sufficient internal data paths to permit algorithms to be executed without sending data off chip. The multiplier utilizes a non-square architecture with 16-bit and 24-bit ports. Data will fall from on-chip registers through the multiplier and the 48-bit ALU to the Accumulator registers in 100ns, allowing full 10MHz operation.

### Multiplier

The 16 x 24 Multiplier uses 2-bit Booth encoding for high speed and supports signed, unsigned and mixed mode arithmetic. The preferred format is twos complement fractional.

The multiplier produces a full 40-bit result from the 16- and 24-bit inputs without the need for format adjusting as the  $-1 \times -1$  condition is trapped to produce  $+1$  as the result.

### ALU

The 48-bit ALU supports 32 instructions split into two 16-instruction fields. The first field supports ALU instructions that use data routed to the B' input rather than the B input from the multiplier. This latter field includes the four instructions that program the active condition of the BFP Flag and an instruction for clearing the accumulator register.

The ALU has two accumulator registers each of which is 48-bits wide and may be loaded independently. The two flags indicate the sign of the current result, or whether one of the four BFP conditions has been satisfied. These four conditions are: OVR, indicating that an overflow of the 48-bit field has occurred; UND1 indicates that the current ALU result is within a factor of 2 of overflowing; UND2 indicates that the current ALU result is within a factor of 4 of overflowing; and ZERO indicates that the current ALU result is zero. Input fields to the ALU that are less than 48-bits wide are automatically sign extended to 48-bit fields.

### Funnel Shifter

The Funnel Shifter selects 32-bit fields from the 48-bit input on 16- and 24-bit boundaries. This function allows the 48-bit input to be considered as either two 24-bit fields for output on the C port, or as three 16-bit fields that may be written into the register file.

### Register File

The register file consists of 16 x 16-bit words configured as 8 x 32-bit words. The two instruction fields allow random access to any of the eight 32-bit words for reading and a selection of eight load instructions for assembling 32-bit words from 16-bit fields. The Register file is configured as a push down stack, whereby each new word written into the stack pushes down by one address the current contents of the stack. Data that 'falls off' the bottom of the stack may be routed back and rewritten into the stack via the funnel shifter.

### Multiprecision Operation

Multiprecision operation is supported via the Accumulator feedback path to the ALU A input port. Data fed back via this route may be shifted by special ALU instructions to ensure that consecutive Multiplier outputs align in weighting even when they have been generated from multiplier inputs of different weighting. A 24 x 32 multiply (for example) is executed in two cycles, the first using the least significant 16-bits of the 32-bit word, the second using the most significant 16-bits. Before the two multiplier outputs can be added to generate the final result, the first output must be shifted 16 places, an operation that is supported by the ALU.

### ABSOLUTE MAXIMUM RATINGS

Supply voltage $V_{CC}$	-0.5V to 7.0V
Input voltage $V_{IN}$	-0.9V to $V_{CC} + 0.9V$
Output voltage $V_{OUT}$	-0.9V to $V_{CC} + 0.9V$
Clamp diode current per pin $I_K$ (See Note 2)	$\pm 18mA$
Static discharge voltage $V_{STAT}$ (HMB)	500V
Storage temperature $T_S$	-65°C to +150°C
Ambient temperature with power applied $T_{amb}$	-40°C to +85°C
Package power dissipation $P_{TOT}$ AC package	1000mW

### NOTES

1. Exceeding these ratings may cause permanent damage. Functional operation under these conditions is not implied.
2. Maximum dissipation or 1 second should not be exceeded, only one output to be tested at any one time.

## ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

$T_{amb} = -40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ ,  $V_{cc} = 5.0\text{V} \pm 10\%$ , Ground = 0V

### Static Characteristics

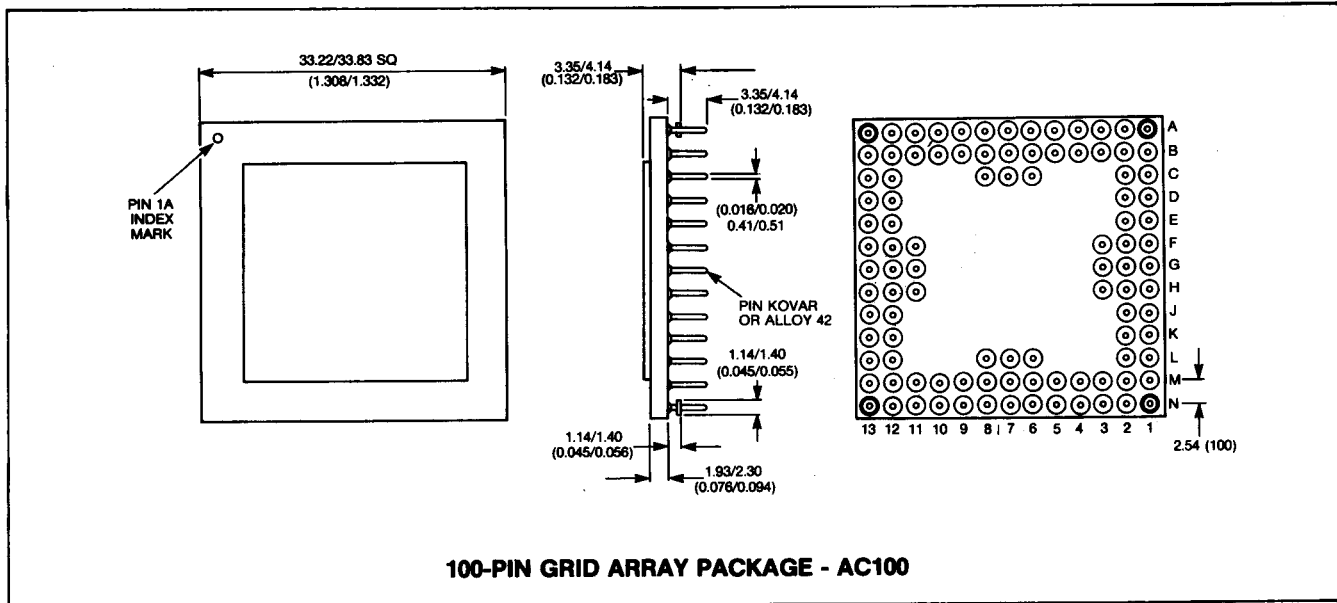
Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Output high voltage	$V_{OH}$	2.4		-	V	$I_{OH} = 3.2\text{mA}$ $I_{OL} = -1.6\text{mA}$
Output low voltage	$V_{OL}$	-		0.4	V	
Input high voltage	$V_{IH}$	2.0		-	V	$GND < V_{IN} < V_{CC}$
Input low voltage	$V_{IL}$	-		0.8	V	
Input leakage current	$I_{IL}$	-10		+10	$\mu\text{A}$	
Input capacitance	$C_{IN}$	-	-	5	pF	
Output leakage current	$I_{OZ}$	-50		+50	$\mu\text{A}$	$GND < V_{OUT} < V_{CC}$
Output short circuit current	$I_{OS}$				mA	
$V_{CC}$ current	$I_{CC}$	-		90	mA	$V_{CC} = \text{Max.}$

### Switching Characteristics

Characteristic	Value			Units
	Min.	Typ.	Max.	
Clock period	100			ns
Clock high time	30			ns
Clock low time	30			ns
Input data setup to clock rising edge	30			ns
Input data hold after clock rising edge	0			ns
Instruction setup to clock rising edge	30			ns
Instruction hold after clock rising edge	0			ns
Clock rising edge to data valid			60	ns
Clock rising edge to status flags valid			95	ns
$\overline{OE}$ low to output data high valid			25	ns
$\overline{OE}$ low to output data low valid			25	ns
$\overline{OE}$ low to output data high impedance			25	ns

## PACKAGE DETAILS

Dimensions are shown thus: mm (in).



## ORDERING INFORMATION

**Industrial**  
**PDSP1610 B0 AC**

**Military**  
**PDSP1610 A0 AC**

Call for availability on High Reliability parts and MIL 883C screening.



**PLESSEY SEMICONDUCTORS LTD.**,  
 Cheney Manor, Swindon,  
 Wiltshire SN2 2QW, United Kingdom.  
 Tel: (0793) 36251 Tx: 449637.  
 Fax: (0793) 36251 Ext. 2198

**PLESSEY SEMICONDUCTORS**,  
 9 Parker, Irvine, California 92718,  
 United States of America.  
 Tel: (714) 472 0303 Twx: (910) 595-1930.  
 Telex: 701464 Fax: (714) 770-0627

We also have sales and marketing centres in:

- **BENELUX** Brussels Tel: 02 733 9730 Tx: 22100
- **FRANCE** Les Ulis Cedex Tel: (1) 64-46-23-45 Tx: 692858F
- **GERMANY (FDR)** Munich Tel: 089 23 62-0 Tx: 0522197
- **ITALY** Milan Tel: (2) 390044/5 Tx: 331347
- **UNITED KINGDOM** Swindon Tel: (0793) 726666 Tx: 444410

These are supported by Agents and Distributors in major countries world-wide.

©The Plessey Company plc 1987 Publication No. P.S. 2126 March 1987

This publication is issued to provide outline information only which (unless agreed by the Company in writing) may not be used, applied or reproduced for any purpose or form part of any order or contract or be regarded as a representation relating to the products or services concerned. The Company reserves the right to alter without notice the specification, design, price or conditions of supply of any product or service. PLESSEY and the Plessey symbol are trademarks of The Plessey Company plc.

008971 / - -