MOTOROLA

MC54/74HC92

Product Preview

HIGH-PERFORMANCE
CMOS
LOW-POWER COMPLEMENTARY MOS
SILICON-GATE

4-STAGE BINARY RIPPLE COUNTER WITH ÷2 AND ÷6 SECTIONS

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The MC54/74HC92 is identical in pinout to the LS92. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

The HC92 is a 4-bit ripple counter consisting of a four master/sale flip-flops that are internally connected to provide separate divide-by-two and divide-by-six sections. Each section has a separate Clock input which initiates state changes of the counter on the high-to-low clock transition. State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and should not be used as clocks or as strobes except when gated with the Clock of the HC92. Q_A is the output of the divide-by-two section; Q_B, Q_C and Q_D are the binary outputs of the divide-by-six section.

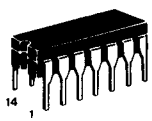
A gated AND asynchronous Reset is provided which resets all the flip-flops.

Because the output from the divide-by-two section is not internally connected to the succeeding stages, the devices may be operated in various counting modes:

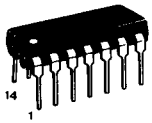
1. A Modulo-12, Divide-By-Twelve Counter — The Clock B input must be externally connected to the Q_A output. The Clock A input receives the incoming count and Q_D produces a symmetrical divide-by-twelve square wave output.
2. Divide-By-Two and Divide-By-Six Counters — No external interconnections are required. The first flip-flop is used as a binary element for the divide-by-two function. The Clock B input is used to obtain divide-by-three operation at the Q_B and Q_C outputs and divide-by-six operation at the Q_D output.

- Choice of Counting Modes: ÷2, ÷6, and ÷12
- Low Power Consumption Characteristic of CMOS Devices
- Output Drive Capability: 10 LSTTL Loads Minimum
- Operating Speeds Similar to LSTTL
- Wide Operating Voltage Range: 2 to 6 Volts
- Low Input Current: 1 μA Maximum
- Low Quiescent Current: 80 μA Maximum (74HC Series)
- High Noise Immunity Characteristic of CMOS Devices
- Diode Protection on All Inputs

PRODUCT CANCELLED



J SUFFIX
CERAMIC PACKAGE
CASE 632



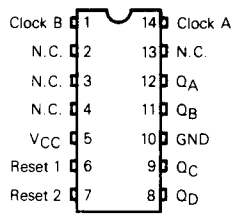
N SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

54 Series: −55°C to +125°C
MC54HCXXJ (Ceramic Package Only)

74 Series: −40°C to +85°C
MC74HCXXN (Plastic Package)
MC74HCXXJ (Ceramic Package)

PIN ASSIGNMENT



N.C. = No Connection

MODE SELECTION TABLE

Inputs			Outputs			
Reset 1	Reset 2	Clock	Q_D	Q_C	Q_B	Q_A
H	H	X	L	L	L	L
L	H	⌥	Count			Toggle
H	L	⌥	Count			Toggle
L	L	⌥	Count			Toggle

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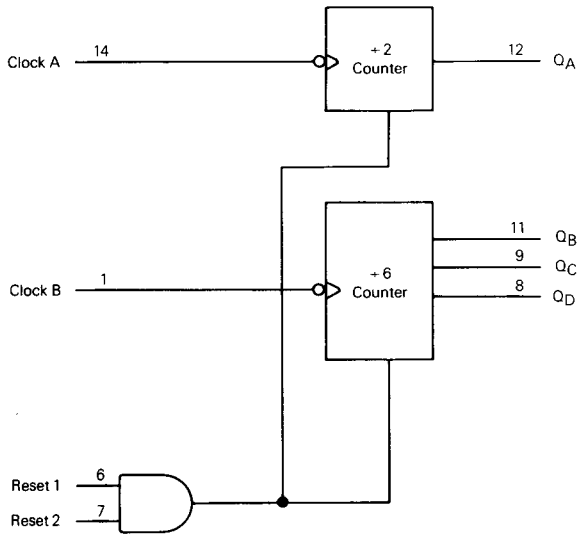
This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice

BLOCK DIAGRAM



V_{CC} = Pin 5
GND = Pin 10
No Connection = Pins 2, 3, 4, 13

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