REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Delete case X dimensions and use D-10, appendix C of MIL-M38510. Change terminal connections for case 3. Changes to recommended operating conditions, table I, and table II. Convert to military drawing format. Editorial changes throughout.	87-04-17	N. A. Hauck
B	Changes in accordance with NOR 5962-R028-96.	96-01-03	Monica L. Poelking
C	Incorporated revision B and updated boilerplate and editorial changes throughout. Added vendor CAGE CODE 34371. - LTG	00-07-31	Monica L. Poelking
D	Update boilerplate to MIL-PRF-38535 requirements. – LTG	01-05-24	Thomas M. Hess
E	Correct marking requirements in 3.5. Update boilerplate in accordance with MIL-PRF-38535 requirements. Editorial changes throughout. - PHN.	05-02-23	Thomas M. Hess

REV																				
SHEET																				
REV																				
SHEET																				
REV STATUS				REV			E	C	E	E	C	C	E	E	E	E	E	E		
OF SHEETS				SHEET			1	2	3	4	5	6	7	8	9	10	11	12		

PMIC N/A

PREPARED BY
Greg A. Pitz

CHECKED BY
D. A. DiCenzo

APPROVED BY
N. A. Hauck

DRAWING APPROVAL DATE
85-11-08

REVISION LEVEL
E

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43218-3990
http://www.dscc.dla.mil

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

MICROCIRCUIT, DIGITAL, CMOS, SERIAL CONTROLLER INTERFACE, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**85015**

SHEET 1 OF 12

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:

85015	01	X	X
Drawing number	Device type (see 1.2.1)	Case outline (see 1.2.2)	Lead finish (see 1.2.3)

1.2.1 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Frequency	Circuit function
01	82C52	16 MHz	CMOS monolithic serial controller interface

1.2.2 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	GDIP1-T28 or CDIP2-T28	28	Dual-in-line package
3	CQCC1-N28	28	Square chip carrier package

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings.

Supply voltage (referenced to ground) ..... +8.0 V dc
Input, output, or I/O voltage applied ..... GND -0.5 V dc to V_{CC} +0.5 V dc
Storage temperature range (T_{STG}) ..... -65°C to +150°C
Maximum power dissipation (P_D): ..... 1 W
Lead temperature (soldering, 10 seconds) ..... +260°C
Maximum junction temperature (T_J) ..... +150°C
Thermal resistance, junction-to-case (θ_{JC}):
Case X ..... 18°C/W
Case 3 ..... 60°C/W 1/

1.4 Recommended operating conditions.

Supply voltage range (V_{CC}) ..... +4.5 V dc min to +5.5 V dc max
Case operating temperature range (T_C) ..... -55°C to +125°C
IX input rise or fall time (t_r, t_f) ..... tx 2/
Frequency of operation ..... 16 MHz maximum
Operating supply current (I_{CCOP}) (outputs open) ..... 3.0 mA maximum 3/
Read disable (t_{RHDZ}) ..... 0 to 60 ns maximum 4/

1/ When a thermal resistance value is included in MIL-STD-1835, it shall supersede the value stated herein.
2/ tx < 1/6 F_C or 50 ns, whichever is less. See figure 3.
3/ External clock, f = 2.4576 MHz, V_{CC} = 5.5 V, V_{IN} = V_{CC} or GND.
4/ See figure 4, test condition 2 and figure 3 waveform.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or http://assist.daps.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used. This drawing has been modified to allow the manufacturer to use the alternate die/fabrication requirements of paragraph A.3.2.2 of MIL-PRF-38535 or other alternative approved by the qualifying activity.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Functional diagram. The functional diagram shall be as specified on figure 2.

3.2.4 Switching waveforms and test circuit. The switching waveforms and test circuit shall be as specified on figures 3.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked.

3.5.1 Certification/compliance mark. A compliance indicator “C” shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator “C” shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used. For product built in accordance with A.3.2.2 of MIL-PRF-38535, or as modified in the manufacturer’s QM plan, the “QD” certification mark shall be used in place of the "Q" or "QML" certification mark.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DSCC-VA shall be required for any change that affects this drawing.

3.9 Verification and review. DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

TABLE I. Electrical performance characteristics.

Test	Symbol	Test conditions $-55°C \le T_C \le +125°C$ unless otherwise specified		Group A subgroups	Limits		Unit
					Min	Max	
High level output voltage 1/	V_{OH}	I_{OH} = -2.5 mA, V_{CC} = 4.5 V Except OX		1, 2, 3	3.0		V
		I_{OH} = -100 µA, V_{CC} = 4.5 V For OX, I_{OH} = -1.0 mA		1, 2, 3	V_{CC}-0.4		
Low level output voltage 1/	V_{OL}	I_{OL} = +2.5 mA, V_{CC} = 4.5 V For OX, I_{OL} = +1.0 mA		1, 2, 3		0.4	V
High level input voltage	V_{IH}	V_{CC} = 5.5 V		1, 2, 3	0.7V_{CC}		V
Low level input voltage	V_{IL}	V_{CC} = 4.5 V		1, 2, 3		0.4	V
Input leakage current (Except for IX)	I_{IN}	V_{CC} = 5.5 V	V_{IN} = 0.0 V	1, 2, 3	-1.0		µA
			V_{IN} = V_{CC}	1, 2, 3		1.0	
Output leakage current	I_{OUT}	V_{CC} = 5.5 V	V_{IN} = 0.0 V	1, 2, 3	-10		µA
			V_{IN} = V_{CC}			10	
Schmitt trigger logical one input voltage	V_{TH}	Reset input, V_{CC} = 5.5 V		1, 2, 3	V_{CC}-0.5		V
Schmitt trigger logical zero input voltage	V_{TL}	Reset input, V_{CC} = 4.5 V		1, 2, 3		GND+0.5	V
Logical one clock input voltage	V_{IH} ($_{CLK}$)	External clock, V_{CC} = 5.5 V		1, 2, 3	V_{CC}-0.5		V
Logical zero clock input voltage	V_{IL} ($_{CLK}$)	External clock, V_{CC} = 4.5 V		1, 2, 3		GND+0.5	V

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions 2/ $-55°C \le T_C \le +125°C$ V_{CC} = 4.5 V and 5.5 V unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
Input capacitance	C_{IN}	Frequency = 1MHz	4		12	pF
Output capacitance	C_{OUT}	T_C = +25°C	4		15	pF
I/O capacitance	$C_{I/O}$	See 4.3.1c All measurements are referenced to device ground	4		15	pF
Functional tests		See 4.3.1d 2/ V_{CC} = 4.5 V and 5.5 V	7, 8			
Select setup to control leading edge	t_{SVCTL}		9, 10, 11	30		ns
Select hold from control trailing edge	t_{CTHSX}		9, 10, 11	50		ns
Control pulse width	t_{CTLCTH}	Control consists of $\overline{RD}$ or $\overline{WR}$	9, 10, 11	150		ns
Control disable to control enable	t_{CTHCTL}		9, 10, 11	190		ns
Read low to data valid	t_{RLDV}	Test condition 1	9, 10, 11		120	ns
Data setup time	t_{DVWH}		9, 10, 11	50		ns
Data hold time	t_{WHDX}		9, 10, 11	20		ns
Clock frequency 3/	F_C		9, 10, 11	0	16	MHz
Clock high time	t_{CHCL}		9, 10, 11	25		ns
Clock low time	t_{CLCH}		9, 10, 11	25		ns
Clock output fall time	t_{FCO}	Measured from 0.7 V_{CC} to 0.8 V	9, 10, 11		15	ns
Clock output rise time	t_{RCO}	Measured from 0.8 V to 0.7 V_{CC}	9, 10, 11		15	ns

1/ Interchanging of force and sense conditions is permitted.
2/ Tested as follows: f = 1 MHz, V_{IH} = 0.7 V_{CC}, V_{IL} = 0.4 V, C_L = 50 pF unless a test condition is specified, $V_{IH}(CLK) = V_{CC}$-0.5 V, $V_{IL}(CLK)$ = GND + 0.5 V, $V_{TH} = V_{CC}$ –0.5 V, V_{TL} = GND + 0.5 V, $V_{OH} \ge 1.5$ V, and $V_{OL} \le 1.5$ V. See figures 3.
3/ F_C is calculated on measured t_{CHCL} and t_{CLCH} times. t_{CHCL} and t_{CLCH} must be ≥ 62.5 ns.

Device type 01			
Case outlines	**X and 3**		
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	$\overline{RD}$	15	SDO
2	$\overline{WR}$	16	GND
3	D0	17	$\overline{CTS}$
4	D1	18	$\overline{DSR}$
5	D2	19	$\overline{DTR}$
6	D3	20	$\overline{RTS}$
7	D4	21	CO
8	D5	22	TBRE
9	D6	23	RST
10	D7	24	INTR
11	A0	25	SDI
12	A1	26	DR
13	IX	27	VCC
14	OX	28	$\overline{CSO}$

FIGURE 1. Terminal connections.

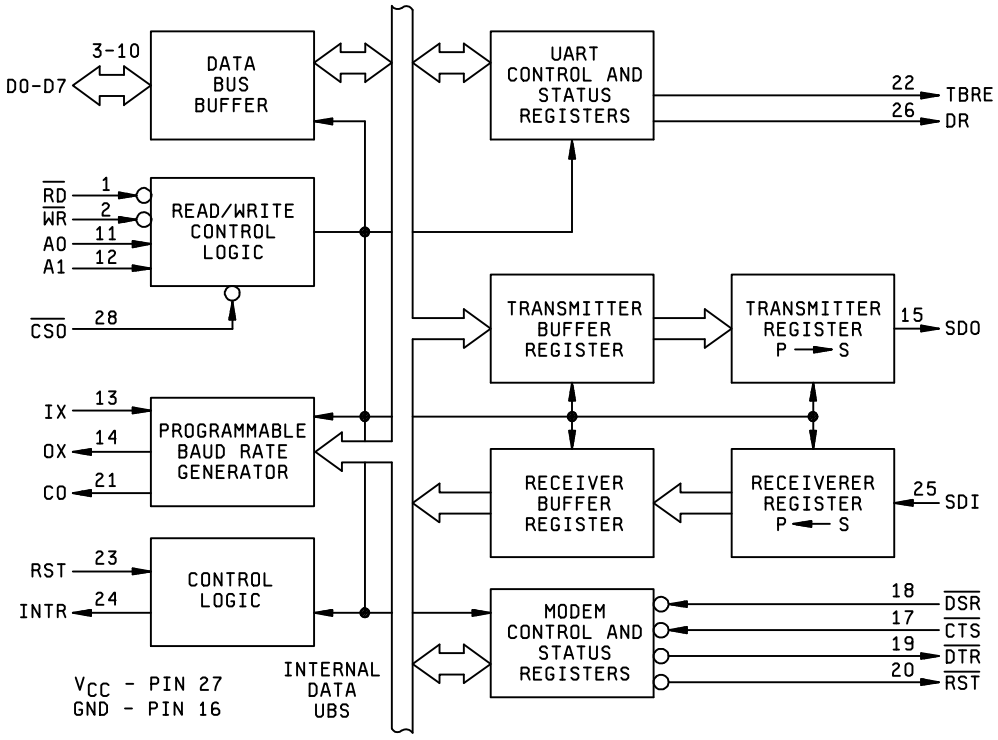
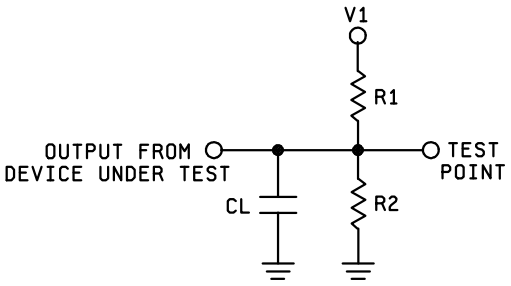
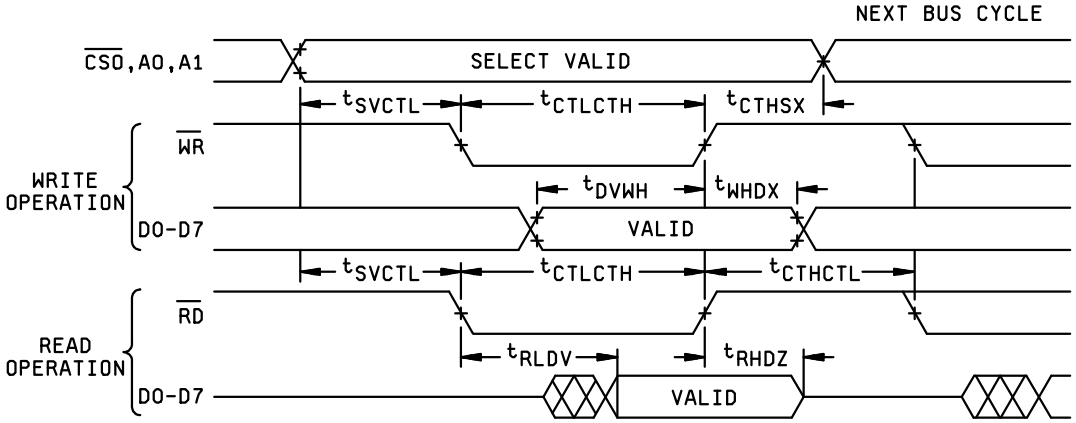
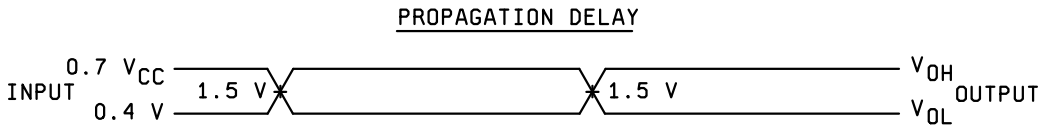


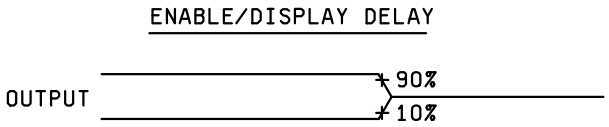
FIGURE 2. Functional diagram.



TEST CONDITION		V1	R1	R2	CL
1	Propagation delay	1.7 V	520Ω	∞	100 pF
2	Disable delay	V_{CC}	5KΩ	5KΩ	50 pF







NOTE:
AC testing: All input signals (other than CLK or RESET) must switch between 0.4 V and 0.7 V_{CC}. Input rise and fall times are driven at 1.0 ns/V.

FIGURE 3. Switching waveforms and test circuit.

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D . The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	------
Final electrical test parameters (method 5004)	1/ 1, 2, 3, 7, 8, 9, 10, 11
Group A test requirements (method 5005)	1, 2, 3, 4, 7, 8 ,9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	2, 8(+125°C only), 10

* PDA applies to subgroup 1.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 4, 5, and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} measurement) shall be measured only for the initial test and after process or design changes which may affect input capacitance.

d. Subgroups 7 and 8 shall include verification of the programming set.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0547.

6.6 Terminal descriptions. See table III herein

TABLE III. Terminal descriptions.

SYMBOL	DESCRIPTION
$\overline{RD}$	READ: The $\overline{RD}$ input causes the device to output data to the data bus (D0-D7). The data output depends upon the state of the address inputs (A0, A1). $\overline{CSO}$ enables the $\overline{RD}$ input.
$\overline{WR}$	WRITE: The $\overline{WR}$ input causes data from the data bus (D0-D7) to be input to the device. Addressing and chip select action is the same as for read operations.
D0-D7	DATA BITS 0-7: The Data Bus provides eight, 3-state input/output lines for the transfer of data, control, and status information between the device and the CPU. For character formats of less than 8 bits, the corresponding D7 , D6 and D5 are considered “don’t cares” for data WRITE operations and are 0 for data READ operations. D0 is the least significant bit (LSB) and is the first serial data bit to be received or transmitted.
A0, A1	ADDRESS INPUTS: The address lines select the various internal registers during CPU bus operations.
IX, OX	CRYSTAL/CLOCK: Crystal connections for the internal Baud Rate Generator. IX can also be used as an external clock input in which case OX should be left open.
SDO	SERIAL DATA OUTPUT: Serial data output from the device transmitter circuitry. A Mark (1) is a logic one (high) and Space (0) is a logic zero (low). SDO is held in the Mark condition when $\overline{CTS}$ is false, when RST is true, when the Transmitter Register is empty, or when in the Loop Mode.
GND	GROUND: Power supply ground connection.
$\overline{CTS}$	CLEAR TO SEND: The logical state of the $\overline{CTS}$ line is reflected in the $\overline{CTS}$ bit of the Modem Status Register. Any change of state in $\overline{CTS}$ causes INTR to be set true when INTEN and MIEN are true. A false level on $\overline{CTS}$ will inhibit transmission of data on the SDO output and will hold SDO in the Mark (high) state. If $\overline{CTS}$ goes false during transmission, the current character being transmitted will be completed. $\overline{CTS}$ does not affect Loop Mode operation.
$\overline{DSR}$	DATA SET READY: The logical state of the $\overline{DSR}$ line is reflected in the Modem Status Register. Any change of state of $\overline{DSR}$ will cause INTR to be set if INTEN and MIEN are true. The state of this signal does not affect any other circuitry within the device.
$\overline{DTR}$	DATA TERMINAL READY: The $\overline{DTR}$ signal can be set (low) by writing a logic 1 to the appropriate bit in the Modem Control Register (MCR). This signal is cleared (high) by writing a logic 0 to the $\overline{DTR}$ bit in the MCR or whenever a reset (RST = high) is applied to the device.
RTS	REQUEST TO SEND: The RTS signal can be set (low) by writing a logic 1 to the appropriate bit in the MCR. This signal is cleared (high) by writing a logic 0 to the RTS bit in the MCR or whenever a reset (RST = high) is applied to the device.
CO	CLOCK OUT: This output is user programmable to provide either a buffered IX output or a buffered Baud Rate Generator (16x) clock output. The buffered IX (Crystal or external clock source) output is provided when the Baud Rate Select Register (BRSR) bit 7 is set to a zero. Writing a logic one to BRSR bit 7 causes the CO output to provide a buffer version of the internal Baud Rate Generator clock which operates at sixteen times the programmed baud rate.On reset, BRSR bit 7 is reset to a zero (buffered IX output selected).
TBRE	TRANSMITTER BUFFER REGISTER EMPTY: The TBRE output is set (high) whenever the Transmitter Buffer Register (TBR) has transferred its data to the Transmit Register. Application of a reset (RST) to the device will also set the TBRE output. TBRE is cleared (low) whenever data is written to the TBR.
RST	RESET: The RST input forces the device into an “idle” mode in which all serial data activities are suspended. The Modem Control Register (MCR) along with its associated outputs are cleared. The UART Status Register (USR) is cleared except for the TBRE and TC bits, which are set. The device remains in an “idle” state until programmed to resume serial data activities. The RST input is a Schmitt trigger input.

TABLE III. Terminal descriptions - Continued.

SYMBOL	DESCRIPTION
INTR	INTERRUPT REQUEST: The INTR output is enabled by the INTEN bit in the Modem Control Register (MCR). The MIEN bit selectively enables modem status changes to provide an input to the INTR logic.
SDI	SERIAL DATA INPUT: Serial data input to the device receiver circuits. A Mark (1) is high, and a Space (0) is low. Data inputs on a SDI are disabled when operating in the loop mode or when RST is true.
DR	DATA READY: A true level indicates that a character has been received, transferred to the RBR and is ready for transfer to the CPU. DR is reset on a data READ of the Receiver Buffer Register (RBR) or when RST is true.
$\overline{CSO}$	CHIP SELECT; The chip select input acts as an enable signals for the $\overline{RD}$ and $\overline{WR}$ input signals.
V_{CC}	POWER: The +5.0 V power supply pin. A 0.1 µF capacitor between V_{CC} and GND is recommended for decoupling.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 05-02-23

Approved sources of supply for SMD 85015 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DSCC maintains an online database of all current sources of supply at http://www.dscc.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
8501501XA	34371	MD82C52/883
85015013A	34371	MR82C52/883

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
34371	Intersil Corporation P. O. Box 883 Melbourne, FL 32902-883