ML2500

1 Megacell Analog Storage Speech Recording LSI

GENERAL DESCRIPTION

The ML2500 utilises analog storage of speech and sound effects into Flash memory cells. The term "analog" refers to a method that involves the charging of Flash cells corresponding to the input waveform with an analog voltage level at a given sampling point per memory cell. Compared with conventional digitalisation, this corresponds to approximately 8 bit data per speech sample. Analog storage, therefore, requires only about 1/8th of memory.

The ML2500 incorporates over a million cells equivalent to 1 Megabit memory. A sampling frequency of 8kHz provided, 128 seconds recording time are available, while 8-bit PCM data would yield only 16 seconds.

Operation control is facilitated by means of a serial peripheral interface (SPI) which accepts command data and provides status information from and to an external MCU. Command data controls recording, stop, playback, start and stop addresses, sampling frequencies, etc. Up to 320 recording channels can be defined each recorded at another sampling frequency if so desired.

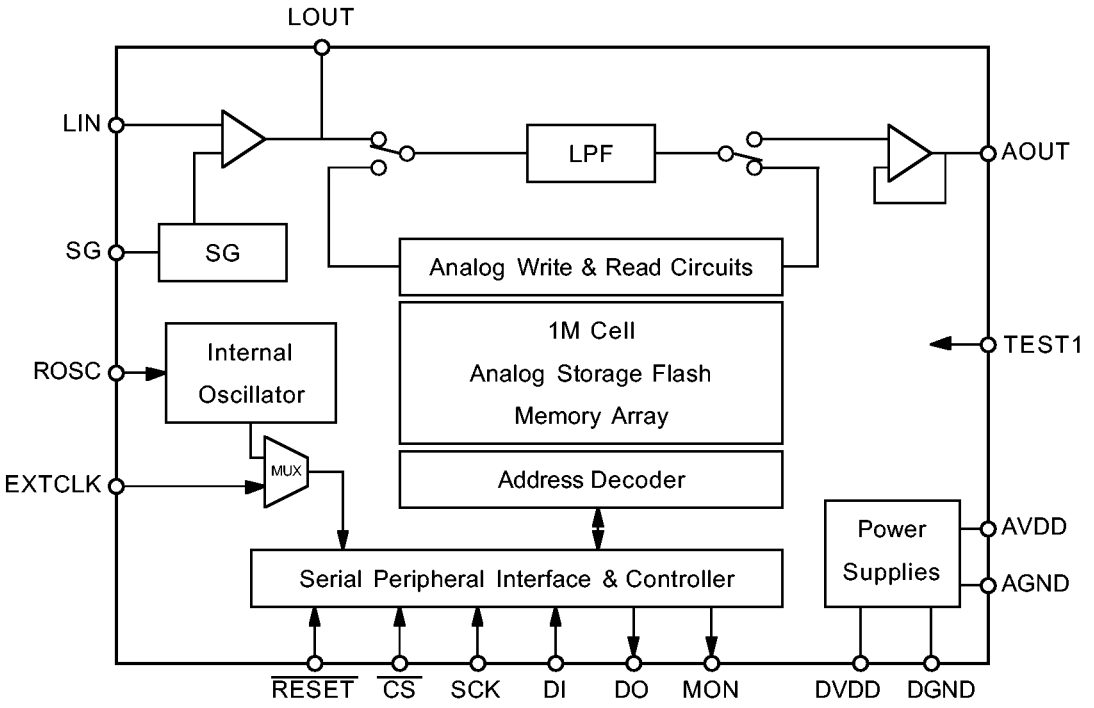
An internal oscillation circuit is included in that the device does not need a master clock. Alternatively an external clock can be applied.

Typical applications are for handy phones, answering machines, voice memos, and many more.

FEATURES

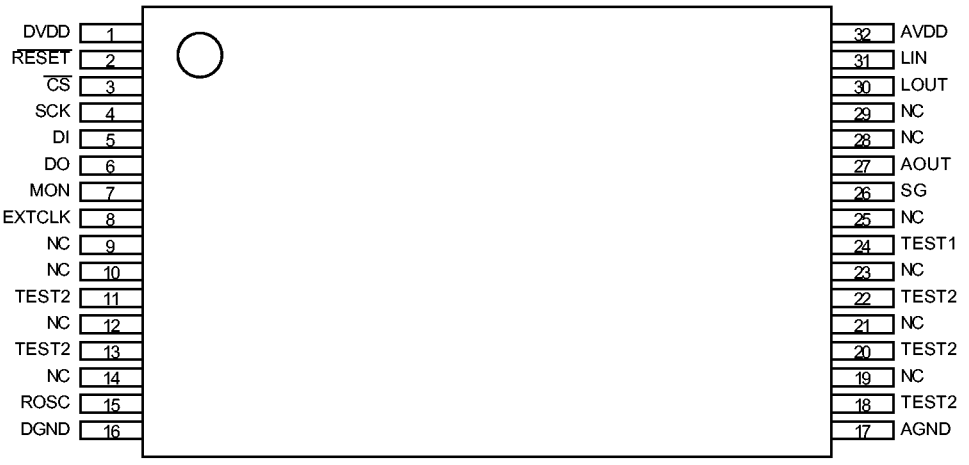
- Internal 1 megacell analog storage Flash
  - 10000 (min.) erase/write cycles
  - 10 years (min.) data retention
  - Write/read accuracy approx. 8-bit (10mV reference level)
- Serial peripheral interface (mode 0), requires external MCU
- Sampling frequencies: 4.0, 5.3, 6.4 and 8.0kHz
- Recording times:
  - ca. 128 sec (@8.0kHz)
  - ca. 160 sec (@6.4kHz)
  - ca. 193 sec (@5.3kHz)
  - ca. 256 sec (@4.0kHz)
- Recording channels: 320
- Internal LPF (-40dB/oct.)
- Internal generation of oscillation
- External clock frequency range: 4.0 ~ 8.192MHz
- Power supply voltage: +2.7 ~ 3.6V
- Typical current: 30mA (when recording)
- Operating temperature: -20 ~ +85°C
- Package: 32-TSOP I (TSOPI32-P-814-0.50-1K)
- Order number: ML2500TA

BLOCK DIAGRAM



PIN ASSIGNMENT

32-lead TSOP (Type I)
(top view)



'NC' labelled pins are not connected

PIN DESCRIPTIONS

Pin #	Name	Type	Description
5	DI	I	Serial input pin for commands and data.
6	DO	O	Serial output for status data.
4	SCK	I	Shift clock input for DI and DO.
3	$\overline{CS}$	I	Chip select pin. When set to "L", serial data input and output are enabled.
2	$\overline{RESET}$	I	Reset input only for the serial interface circuit. When set to "L", the serial interface assumes standby mode. After power-on, make sure to apply a reset pulse.
15	ROSC	I	Connect a 30kΩ resistor across this pin and DGND. The resistor value determines the frequency of the built-in oscillator circuit. The maximum tolerance allowed is ±1%.
8	EXTCLK	I	External clock input for 4.0 to 8.192MHz. When external clock is not used, connect this pin to DGND. EXTCLK is internally pulled down.
7	MON	O	Outputs "H" during recording and playback operations.
26	SG	O	Analog reference voltage output (signal ground).
31	LIN	I	Inverting input of the internal OpAmp. The non-inverting input of the OpAmp is internally wired to SG.
30	LOUT	O	Output of the internal OpAmp.
27	AOUT	O	Playback analog output, typically connected to an external amplifier
11, 13, 18, 20, 22	TEST2	O	These are test outputs for factory testing purposes. Leave them all open.
24	TEST1	I	A test input for factory testing purposes. Connect it to DGND.
1	DVDD	-	Digital supply voltage pin. Connect a 0.1μF capacitor across this pin and DGND.
16	DGND	-	Digital ground terminal.
32	AVDD	-	Analog supply voltage pin. Connect a 0.1μF capacitor across this pin and AGND.
17	AGND	-	Analog ground terminal.
9, 10, 12, 14, 19, 21, 23, 25, 28, 29	NC	-	These pins are not connected.

ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Condition	Rating	Unit
Supply voltage	V_{DD}	Ta = 25°C	-0.3 ~ +5.0	V
Input voltage	V_{IN}	-	-0.3 ~ V_{DD}+0.3	V
Storage temperature	T_{STG}	-	-55 ~ +150	°C

RECOMMENDED OPERATING CONDITIONS

Item	Symbol	Condition	Rating	Unit
Supply voltage	V_{DD}	DGND=AGND=0V	+2.7 ~ 3.6	V
Operating temperature	T_{OP}	-	-20 ~ +85	°C
External clock frequency	f_{CLK}	-	4.0 ~ 8.192	MHz

DC CHARACTERISTICS

DVDD = AVDD = +2.7~3.6V, DGND = AGND = 0V, Ta = -20 ~ +85°C

Item	Symbol	Condition	Min	Typ	Max	Unit
'H' input voltage	V_{IH}	DGND = AGND = 0V	0.8 x V_{DD}	-	-	V
'L' input voltage	V_{IL}	-	-	-	0.2 x V_{DD}	V
'H' output voltage	V_{OH}	I_{OH}= -40µA	V_{DD}-0.3	-	-	V
'L' output voltage	V_{OL}	I_{OL}= 2mA	-	-	0.45	V
'H' input current	I_{OH}	V_{IH}= VDD	-	-	10	µA
'L' input current	I_{OL}	V_{IL} = 0V, applies to all inputs, except EXTCLK	-10	-	-	µA
Operation current 1	I_{DD1}	When recording	-	30	TBA	mA
Operation current 2	I_{DD2}	When playing back	-	20	TBA	mA
Operation current 3	I_{DD3}	In standby (no rec/play operation)	-	5	TBA	mA
Power-down current	I_{DDS}	-	-	-	10	µA

ANALOG CHARACTERISTICS

AVDD = +2.7~3.6V, AGND = 0V, Ta = -20 ~ +85°C

Item	Symbol	Condition	Min	Typ	Max	Unit
LIN input impedance	R_{LIN}	-	1	-	-	MΩ
OpAmp open loop gain	G_{OP}	f_{IN} = 0~4kHz	40	-	-	dB
LOUT load resistance	R_{LOUT}	-	200	-	-	kΩ
AOUT load resistance	R_{AOUT}	-	50	-	-	kΩ
LOUT permissable voltage range	V_{LOUT}	-	0.5	-	2.2	V

RECORDING & PLAYBACK CONTROL COMMANDS

Command	1	2	3	4	5	6	7	8	Function
NOP	0	0	0	0	-	-	-	-	No function
REC	0	0	0	1	0	0	0	0	Recording at 4.0kHz sampling, internal or external 8.192MHz clock.
REC	0	0	0	1	0	0	0	1	Recording at 5.3kHz sampling, internal or external 8.192MHz clock.
REC	0	0	0	1	0	0	1	0	Recording at 6.4kHz sampling, internal or external 8.192MHz clock.
REC	0	0	0	1	0	0	1	1	Recording at 8.0kHz sampling, internal or external 8.192MHz clock.
REC	0	0	0	1	0	1	0	0	Recording at 5.3kHz sampling, external 4.096MHz clock. *1
REC	0	0	0	1	0	1	0	1	Recording at 6.4kHz sampling, external 4.096MHz clock *1
REC	0	0	0	1	0	1	1	0	Recording at 8.0kHz sampling, external 4.096MHz clock. *1
REC	0	0	0	1	0	1	1	1	Recording at 16.0kHz sampling, external 4.096MHz clock. *2
PLAY	0	0	1	0	0	0	0	0	Playback at 4.0kHz sampling, internal or external 8.192MHz clock.
PLAY	0	0	1	0	0	0	0	1	Playback at 5.3kHz sampling, internal or external 8.192MHz clock.
PLAY	0	0	1	0	0	0	1	0	Playback at 6.4kHz sampling, internal or external 8.192MHz clock.
PLAY	0	0	1	0	0	0	1	1	Playback at 8.0kHz sampling, internal or external 8.192MHz clock.
PLAY	0	0	1	0	0	1	0	0	Playback at 5.3kHz sampling, external 4.096MHz clock. *1
PLAY	0	0	1	0	0	1	0	1	Playback at 6.4kHz sampling, external 4.096MHz clock. *1
PLAY	0	0	1	0	0	1	1	0	Playback at 8.0kHz sampling, external 4.096MHz clock. *1
PLAY	0	0	1	0	0	1	1	1	Playback at 16.0kHz sampling, external 4.096MHz clock. *2
STOP	0	0	1	1	-	-	-	-	Stop recording or playback
PAUSE	0	1	0	0	-	-	-	-	Pause recording or playback
STADR	0	1	0	1	X	X	X	X	Sets start address for recording and playback *3
SPADR	0	1	1	0	X	X	X	X	Sets stop address for recording and playback *3
RDADR	0	1	1	1	X	X	X	X	Reads out memory address counter, MSB presented first. *3
RDSTAT	1	0	0	0	X	X	X	X	Reads out status register *3
PDWN	1	0	0	1	-	-	-	-	Power down mode
NOP	1	0	1	0	-	-	-	-	No function

*1 Not guaranteed with internal clock
*2 Not guaranteed
*3 Data to follow, see table below

9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	Description of Data
X	X	X	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	Data to send as start address after STADR command
X	X	X	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	Data to send as stop address after SPADR command
X	X	X	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	Address counter data received after RDADR command
03	02	01	00	0	0	0	0	-	-	-	-	-	-	-	-	Status register data received after RDSTAT command

NOTES:
1. When no sampling frequency is determined for recording or playback (4-bit command only sent), then the last selected sampling frequency will remain valid. If there was no previous selection, the default of 6.4kHz will be used.
2. If no start and stop addresses are set, then the previously set range will be used. After a record command, this will entail erasure of the previous recording.

STATUS REGISTER

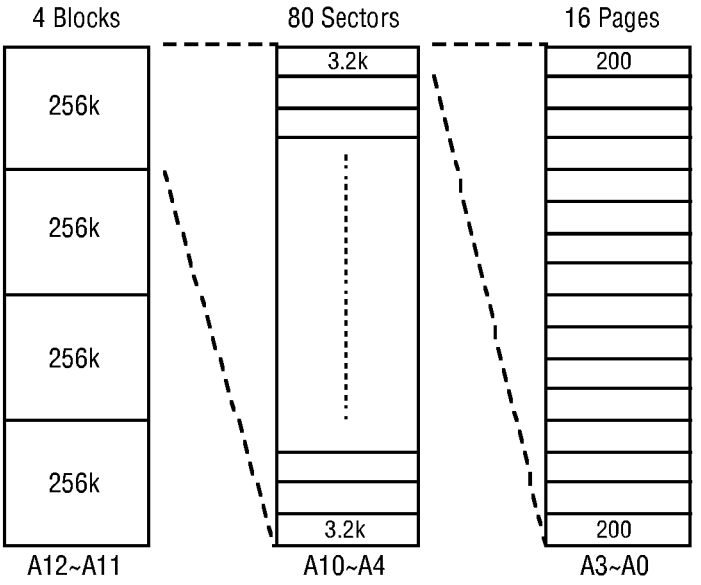
Bit	Name	Function
03	MON	is 'H' during recording and playback, also available as hardware output, pin MON.
02	VPM	is 'H' when recording or playback is paused.
01	RPM	is 'H' during the exact recording and playback time without considering memory control time overheads. RPM is therefore more exact than the MON timing.
00	FULL	is 'H' when the last memory address is reached and recording or playback stopped.

MEMORY STRUCTURE

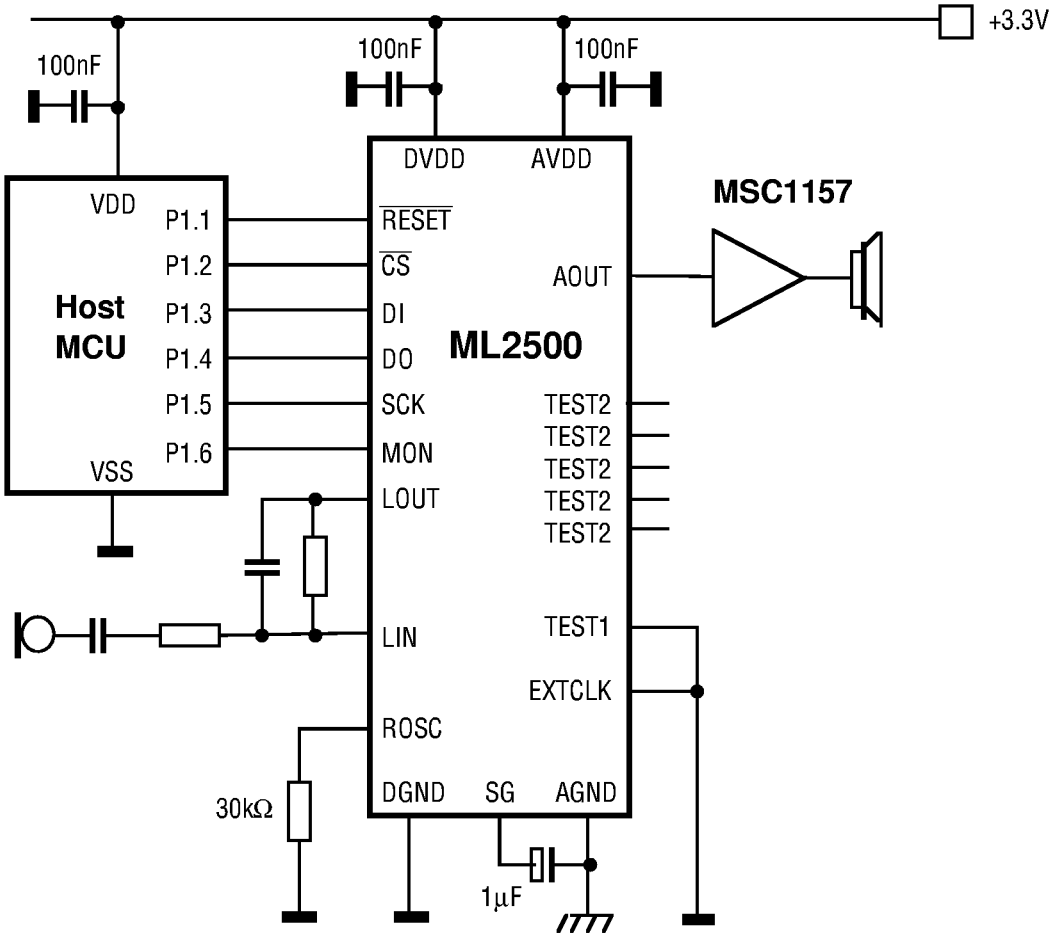
The megacell Flash is structured in four blocks with 256k cells each. A block is further divided into 80 sectors of 3.2k cells each. A sector has 16 pages each of which houses 200 cells. In reverse calculation:

200 cells x 16 pages x 80 sectors x 4 blocks = 1.024k cells

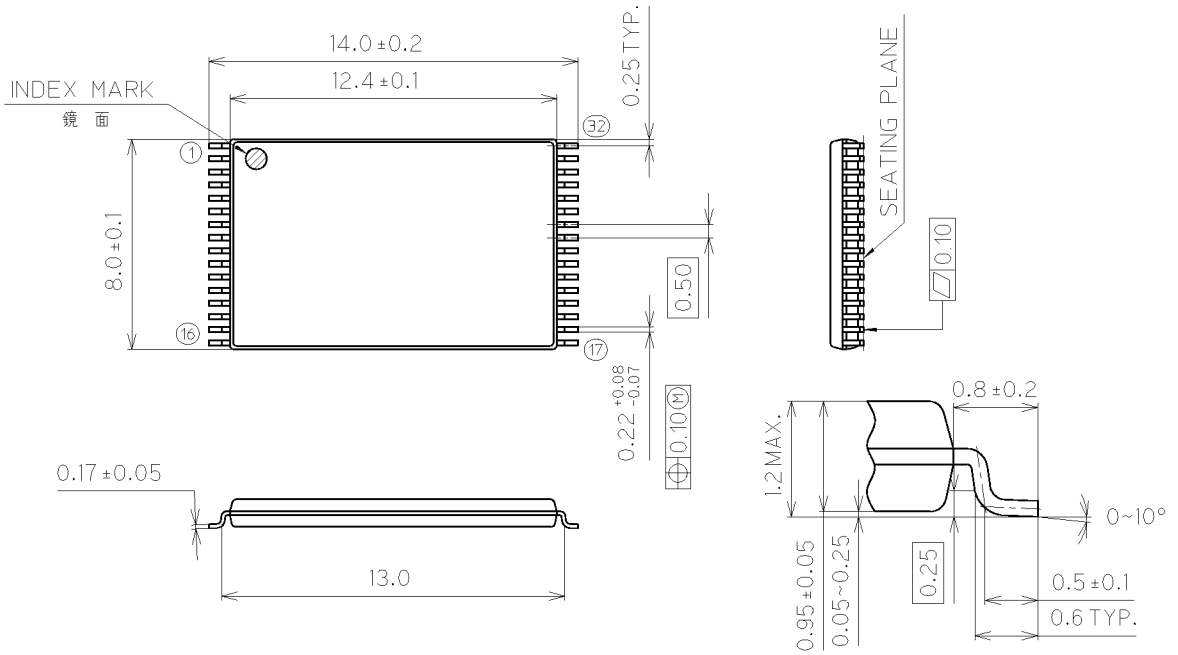
A memory address is composed of 13 bits, while A12 and A11 address a block, A10~A4 a sector and A3~A0 a page. Since a page address is the smallest addressable range containing 200 cells, the minimum recording or playback time unit is 0.025 sec at 8kHz sampling or proportionally 0.05 sec at 4kHz. When serially reading the address counter with the RDADR command, the block address is provided first.



TYPICAL APPLICATION DIAGRAM



PACKAGE DIMENSIONS



Unit in millimeters typically, unless otherwise specified.

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