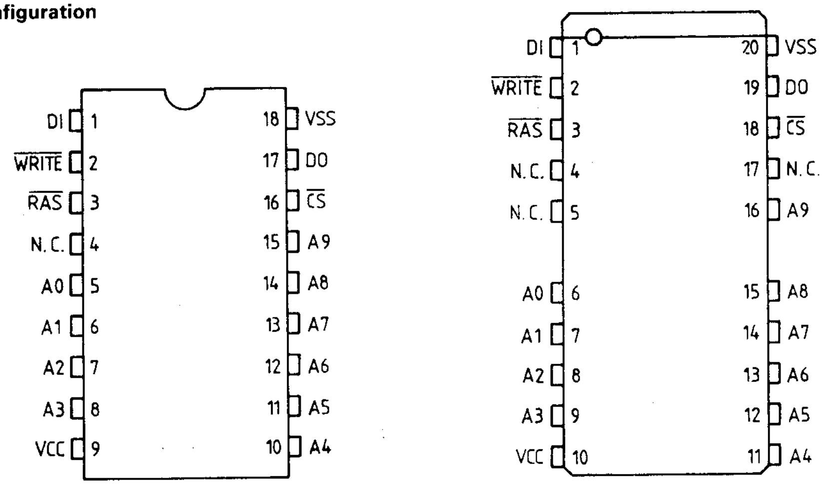
HYB 511002-10/-12 1 048 576 Bit Static Column Dynamic RAM

- 1 048 576 words by 1 bit organization
- Fast access and cycle time
  100 ns access time
  190 ns cycle time (HYB 511002-10)
  120 ns access time
  220 ns cycle time (HYB 511002-12)
- Static column mode cycle time
  55 ns (HYB 511002-10)
  65 ns (HYB 511002-12)
- Single +5V (±10%) supply with a built-in VBB generator
- Low power dissipation
  max. 330 mW active (HYB 511002-10)
  max. 275 mW active (HYB 511002-12)
  max. 5.5 mW standby
- Output unlatched at cycle end allows two-dimensional chip selection
- Common I/O capability
- Read-modify-write, $\overline{\text{CS}}$-before-$\overline{\text{RAS}}$ refresh, $\overline{\text{RAS}}$-only refresh, hidden refresh and static column mode capability
- All inputs and output TTL-compatible
- 512 refresh cycles/8 ms

Pin Configuration

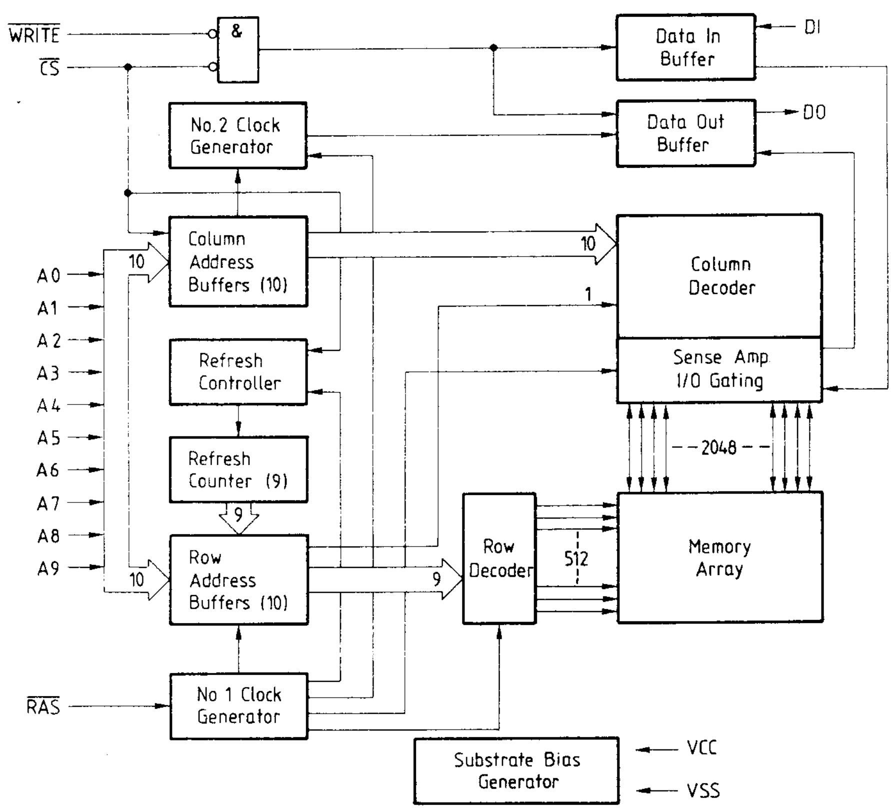


The HYB 511002 is the new generation dynamic RAM organized as 1 048 576 words by 1 bit. The HYB 511002 utilizes CMOS silicon gate process technology as well as advanced techniques to provide wide operating margins, both internally and for the system user. Multiplexed address inputs permit the HYB 511002 to be packaged in a standard 18-pin or in a 20-pin (SOJ) plastic package. This package size provides high system bit densities and is compatible with commonly used automatic testing and insertion equipment. System-oriented features include single +5V (±10%) power supply, direct interfacing with high-performance logic device families such as Schottky TTL.

Pin Names

A0 – A9	Address Inputs
$\overline{RAS}$	Row Address Strobe
DI	Data In
DO	Data Out
$\overline{CS}$	Chip Select Input
$\overline{WRITE}$	Read/Write Input
VCC	Power Supply (+5 V)
VSS	Ground (0 V)
NC	No Connection

Block Diagram



Absolute Maximum Ratings [1]

Operating temperature range	0 to 70°C
Storage temperature range	−55 to +150°C
Soldering temperature	260°C
Soldering time	10 s
Input/Output voltage	−1 to +7 V
Power supply voltage	−1 to +7 V
Power dissipation	0,6 W
Data out current (short circuit)	50 mA

DC Characteristics

TA = 0 to 70°C, VSS = 0 V, VCC = 5 V ± 10%

Symbol	Parameter	Limit values		Unit	Test condition
		min.	max.		
VIH	Input high voltage	2.4	6.5	V	–
VIL	Input low voltage	−1.0	0.8	V	–
VOH	Output high voltage (IOUT = −5 mA)	2.4	–	V	–
VOL	Output low voltage (IOUT = 4.2 mA)	–	0.4	V	–
II(L)	Input leakage current, any input (0 V ≤ VIN ≤ 6.5 V, all other pins = 0 V)	−10	10	µA	–
IO(L)	Output leakage current (DO is disabled, 0 V ≤ VOUT ≤ VCC)	−10	10	µA	–
ICC1	Average VCC supply current: HYB 511002-10	–	60	mA	2) 3)
	HYB 511002-12	–	50	mA	2) 3)
	($\overline{RAS}$, $\overline{CS}$, address cycling: tRC = tRC min.)				
ICC2	Standby VCC supply current ($\overline{RAS}$ = $\overline{CS}$ = VIH)	–	2	mA	–
ICC3	Average VCC supply current during $\overline{RAS}$-only refresh cycles: HYB 511002-10	–	60	mA	2)
	HYB 511002-12	–	50	mA	2)
	($\overline{RAS}$ cycling, $\overline{CS}$ = VIH: tRC = tRC min.)				
ICC4	Average VCC supply current, during fast page mode: HYB 511002-10	–	40	mA	2) 3)
	HYB 511002-12	–	30	mA	2) 3)
	($\overline{RAS}$ = VIL, $\overline{CS}$ address cycling: tPC = tPC min.)				
ICC5	Standby VCC supply current ($\overline{RAS}$ = $\overline{CS}$ = VCC−0.2V)	–	1	mA	–
ICC6	Average VCC supply current during $\overline{CS}$-before-$\overline{RAS}$ refresh mode: HYB 511002-10	–	60	mA	2)
	HYB 511002-12	–	50	mA	2)
	($\overline{RAS}$, $\overline{CS}$ cycling: tRC =tRC (min.)				

1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2) ICC1, ICC3, ICC4 depend on cycle rate.

3) ICC1, ICC4 depend on output loading. Specified values are measured with the output open.

6

AC Characteristics [4) 5)]

TA = 0 to 70°C; VCC = 5 V ± 10%; tT = 5 ns

Symbol	Parameter	Limit values HYB 511002-10 min.	HYB 511002-10 max.	HYB 511002-12 min.	HYB 511002-12 max.	Unit
tRC	Random read or write cycle time	190	–	220	–	ns
tRWC	Read-write cycle time	220	–	255	–	ns
tSC	Static column mode cycle time	55	–	65	–	ns
tSRWC	Static column mode read-write cycle time	100	–	120	–	ns
tT	Transition time (rise and fall) [5)]	3	50	3	50	ns
tRAC	Access time from $\overline{RAS}$ [6) 11)]	–	100	–	120	ns
tAA	Access time from column address [6) 12)]	–	50	–	60	ns
tAOH	Output data hold time from column address	5	–	5	–	ns
tCAC	Access time from $\overline{CS}$ [6) 11)]	–	35	–	45	ns
tOW	Output data enable time from $\overline{WRITE}$	–	30	–	35	ns
tALW	Access time from last write [6) 13)]	–	95	–	115	ns
tCLZ	$\overline{CS}$ to output in low-Z [6)]	5	–	5	–	ns
tOFF	Output buffer turn-off delay [7)]	0	30	0	35	ns
tWOH	Output data hold time from $\overline{WRITE}$	0	–	0	–	ns
tRP	$\overline{RAS}$ precharge time	80	–	90	–	ns
tRAS	$\overline{RAS}$ pulse width	100	10000	120	10000	ns
tRASC	$\overline{RAS}$ pulse width (static column mode)	100	100000	120	100000	ns
tRSH	$\overline{CS}$ to $\overline{RAS}$ hold time	25	–	30	–	ns
tCSH	$\overline{RAS}$ to $\overline{CS}$ hold time	100	–	120	–	ns
tCS	$\overline{CS}$ pulse width	35	–	45	–	ns
tRCD	$\overline{RAS}$ to $\overline{CS}$ delay time [11)]	25	65	25	75	ns
tASR	Row address setup time	0	–	0	–	ns
tRAH	Row address hold time	15	–	15	–	ns
tASC	Column address setup time	0	–	0	–	ns
tCAH	Column address hold time	20	–	25	–	ns
tRAD	$\overline{RAS}$ to column address delay time [12)]	20	50	20	60	ns
tCRP	$\overline{CS}$ to $\overline{RAS}$ precharge time	10	–	10	–	ns
tCP	$\overline{CS}$ precharge time (static column mode)	10	–	15	–	ns
tAR	Column address hold time referenced to $\overline{RAS}$	115	–	140	–	ns

Notes see page 6-84

Symbol	Parameter	Limit values				Unit
		HYB 511002-10		HYB 511002-12		
		min.	max.	min.	max.	
tRAL	Column address to $\overline{RAS}$ lead time (read cycle)	50	–	60	–	ns
tAH	Column address hold time referenced to $\overline{RAS}$ rise [14]	10	–	15	–	ns
tCWL	Write command to $\overline{CS}$ lead time	25	–	30	–	ns
tLWAD	Last write to column address delay time [13]	25	45	30	55	ns
tAHLW	Last write to column address hold time	95	–	115	–	ns
tRCS	Read command setup time referenced to $\overline{CS}$	0	–	0	–	ns
tRRH	Read command hold time referenced to $\overline{RAS}$ [8]	0	–	0	–	ns
tRCH	Read command hold time referenced to $\overline{CS}$ [8]	0	–	0	–	ns
tWP	Write command pulse width	20	–	25	–	ns
tWI	Write command inactive time	10	–	15	–	ns
tRWL	Write command to $\overline{RAS}$ lead time	25	–	30	–	ns
tRWD	$\overline{RAS}$ to $\overline{WRITE}$ delay time (read-write cycle) [10]	100	–	120	–	ns
tAWD	Column address to $\overline{WRITE}$ delay time [10]	50	–	60	–	ns
tCSR	$\overline{CS}$ setup time ($\overline{CS}$ before $\overline{RAS}$)	10	–	10	–	ns
tCHR	$\overline{CS}$ hold time ($\overline{CS}$ before $\overline{RAS}$)	30	–	30	–	ns
tRPC	$\overline{RAS}$ precharge to $\overline{CS}$ active time	0	–	0	–	ns
tCPT	$\overline{CS}$ precharge time ($\overline{CS}$ before $\overline{RAS}$ counter test)	50	–	60	–	ns
tCPN	$\overline{CS}$ precharge time	15	–	20	–	ns
tWCR	Write command hold time referenced to $\overline{RAS}$	75	–	90	–	ns
tWS	Write command setup time (output data disable) [10]	0	–	0	–	ns
tCWD	$\overline{CS}$ to $\overline{WRITE}$ delay time (Read-Write Cycle) [10]	35	–	45	–	ns
tWH	Write command hold time (output data disable) [10]	0	–	0	–	ns
tAWR	Write address hold time referenced to $\overline{RAS}$	75	–	90	–	ns
tDS	Data in setup time [9]	0	–	0	–	ns
tDH	Data in hold time [9]	20	–	25	–	ns
tDHR	Data in hold time referenced to $\overline{RAS}$	75	–	90	–	ns
tREF	Refresh period	–	8	–	8	ms

Notes see page 6-84

Capacitance

TA = 0 to 70°C, VCC = 5 V ±10%, f = 1 MHz

Symbol	Parameter	Limit values		Unit
		min.	max.	
CI1	Input capacitance (A0 to A9, DI)	–	5	pF
CI2	Input capacitance ($\overline{RAS}$, $\overline{CS}$, $\overline{WRITE}$)	–	7	pF
CO	Output capacitance (DO)	–	7	pF

Notes

4) An initial pause of 200 μs is required after power up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved.

5) VIH (min.) and VIL (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between VIH and VIL.

6) Measured with a load equivalent to 2 TTL loads and 100 pF.

7) tOFF (max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

8) Either tRCH or tRRH must be satisfied for a read cycle.

9) These parameters are referenced to $\overline{CS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in read-write cycles.

10) tWS, tWH, tRWD, tCWD and tAWD are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If tWS ≥ tWS (min.) and tWH ≥ tWH (min.), the data out pin will remain open circuit (high impedance) through the entire cycles; If tRWD ≥ tRWD (min.), tCWD ≥ tCWD (min.) and tAWD ≥ tAWD (min.), the cycle is a read-write cycle and the data out will contain data read from the selected cell: If neither of the above sets of conditions is statisfied, the condition of the data out (at access time) is indeterminate.

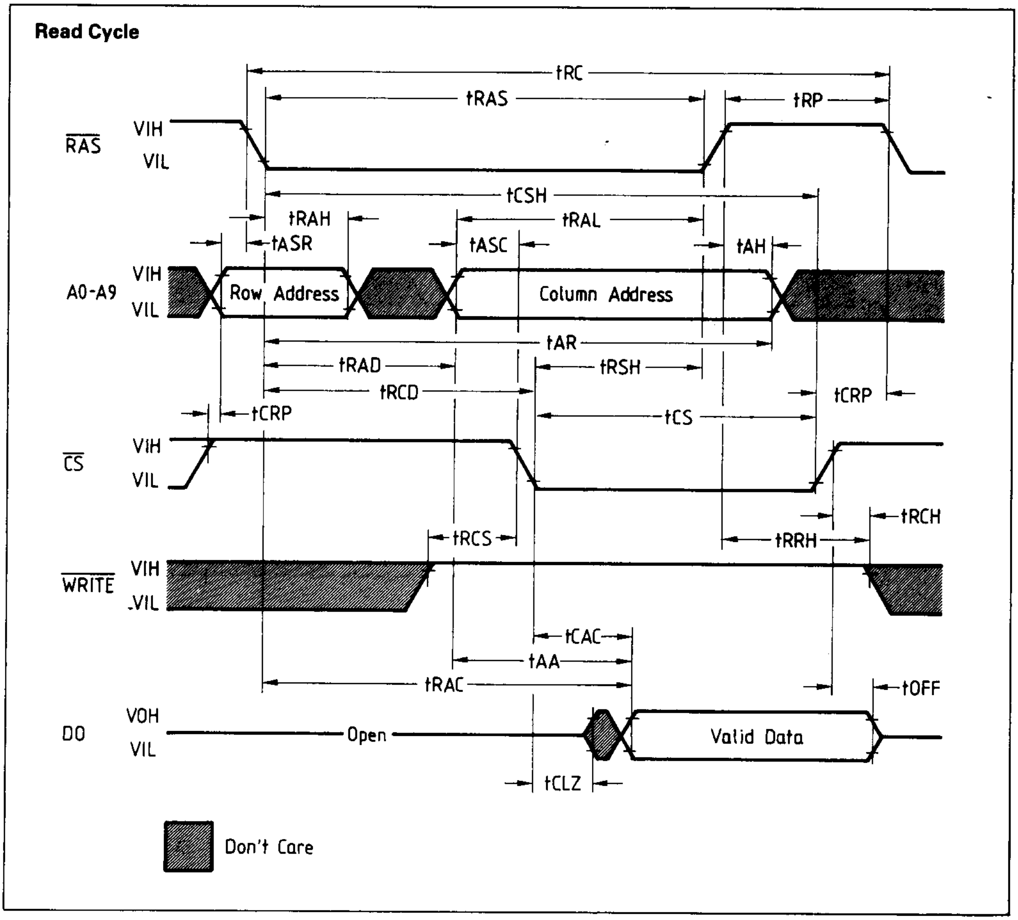
11) Operation within the tRCD (max.) limit insures that tRAC (max.) can be met. tRCD (max.) is specified as a reference point only: If tRCD is greater than the specified tRCD (max.) limit, then access time is controlled by tCAC.

12) Operation within the tRAD (max.) limit insures that tRAC (max.) can be met. tRAD (min.) is specified as a reference point only: If tRAD is greater than the specified tRAD (max.) limit, then access time is controlled exclusively by tAA.

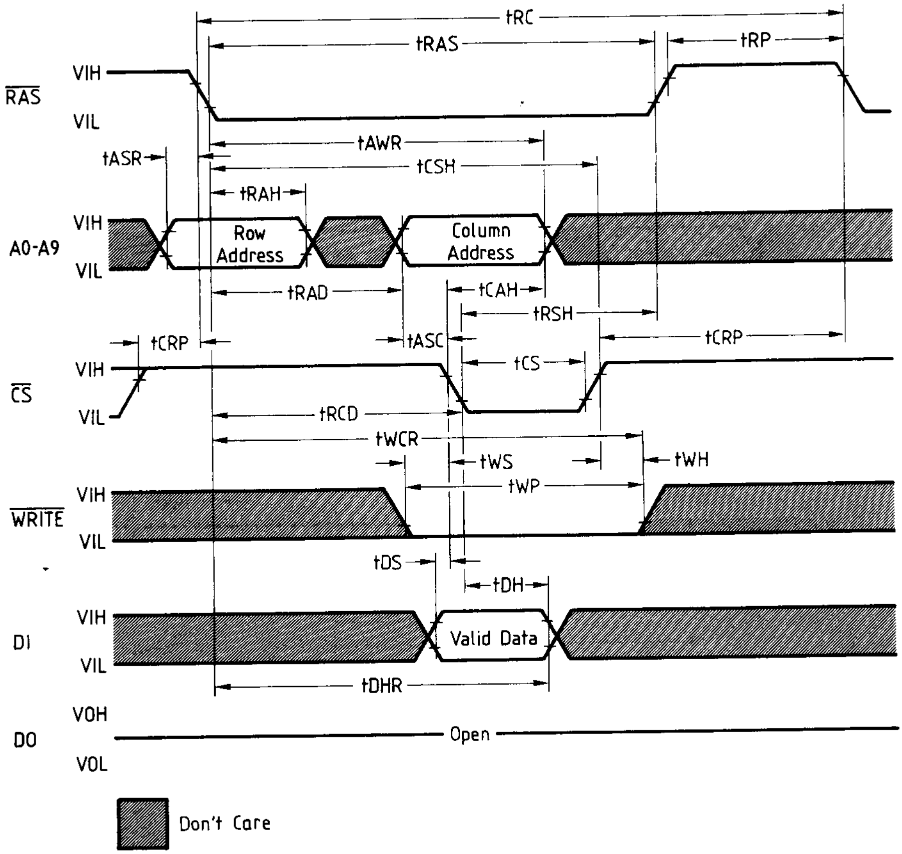
13) Operation within the tLWAD (max.) limit insures that tALW (max.) can be met. tLWAD (max.) is specified as a reference point only: If tLWAD is greater than the specified tLWAD (max.) limit, then access time is controlled exclusively by tAA.

14) tAH is the condition to latch column address when $\overline{RAS}$ has risen up.

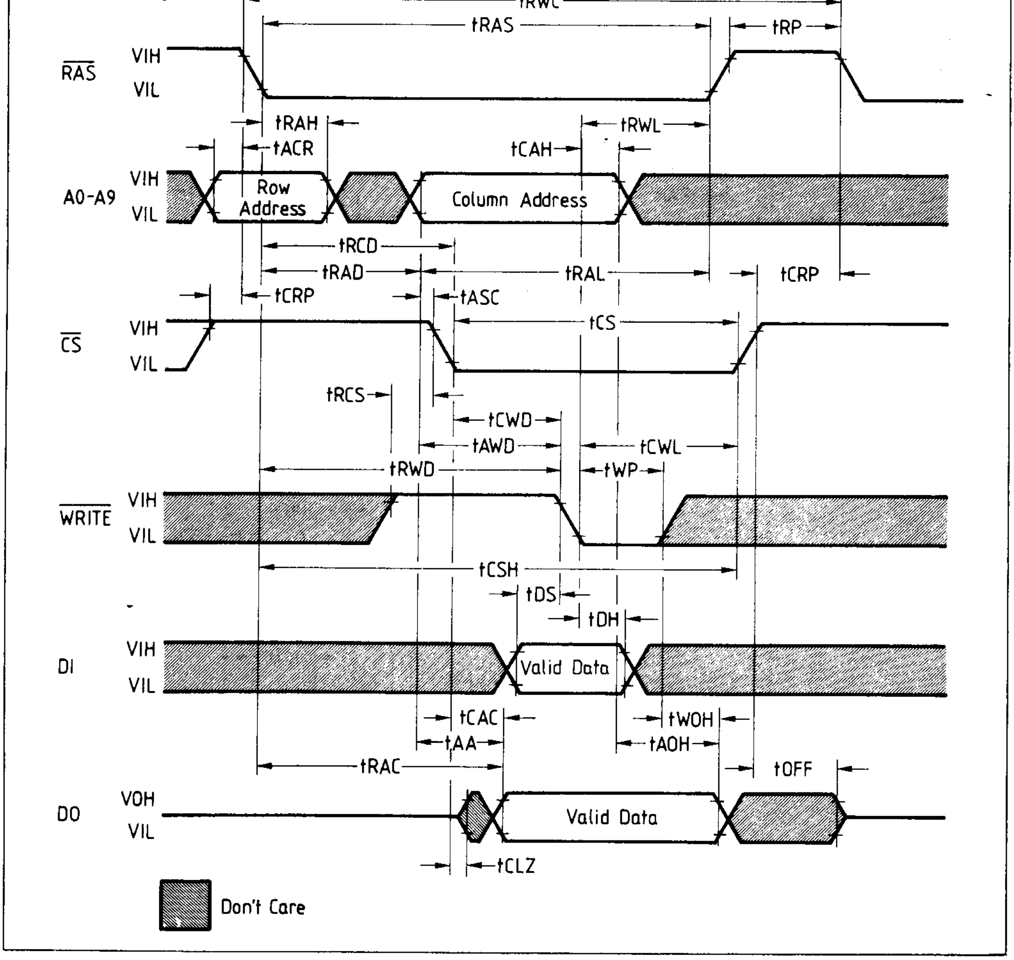
Waveforms


Read Cycle
tRC
tRAS
tRP
RAS
VIH
VIL
tCSH
tRAH
tRAL
tASR
tASC
tAH
A0-A9
VIH
VIL
Row Address
Column Address
tAR
tRAD
tRSH
tRCD
tCRP
tCRP
tCS
CS
VIH
VIL
tRCH
tRCS
tRRH
WRITE
VIH
VIL
tCAC
tAA
tRAC
tOFF
DO
VOH
VIL
Open
Valid Data
tCLZ
Don't Care

Write Cycle (early write)



Read-Write Cycle



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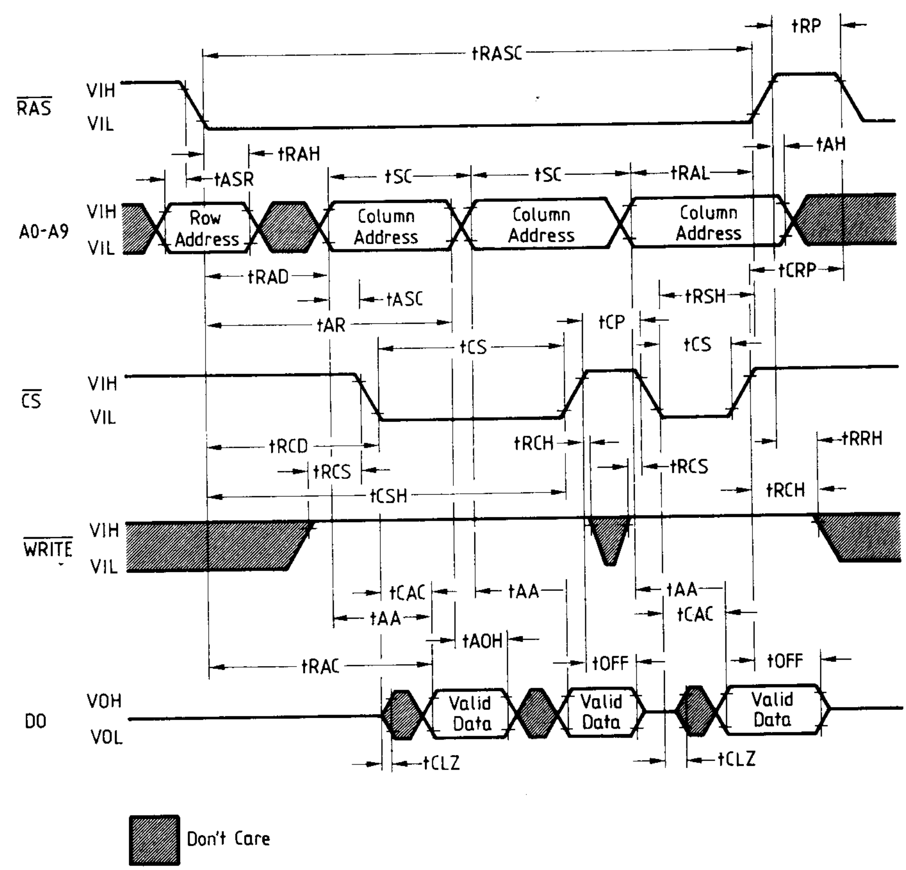
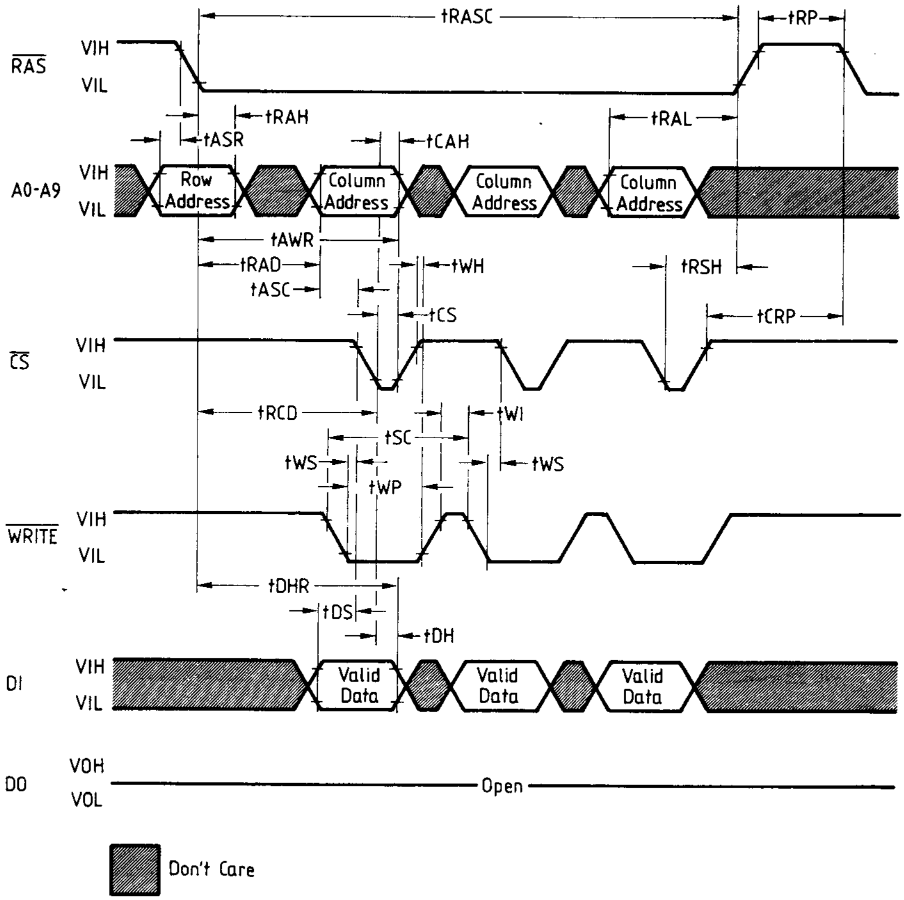
Static Column Mode Read Cycle



Static Column Mode Write Cycle (early write)



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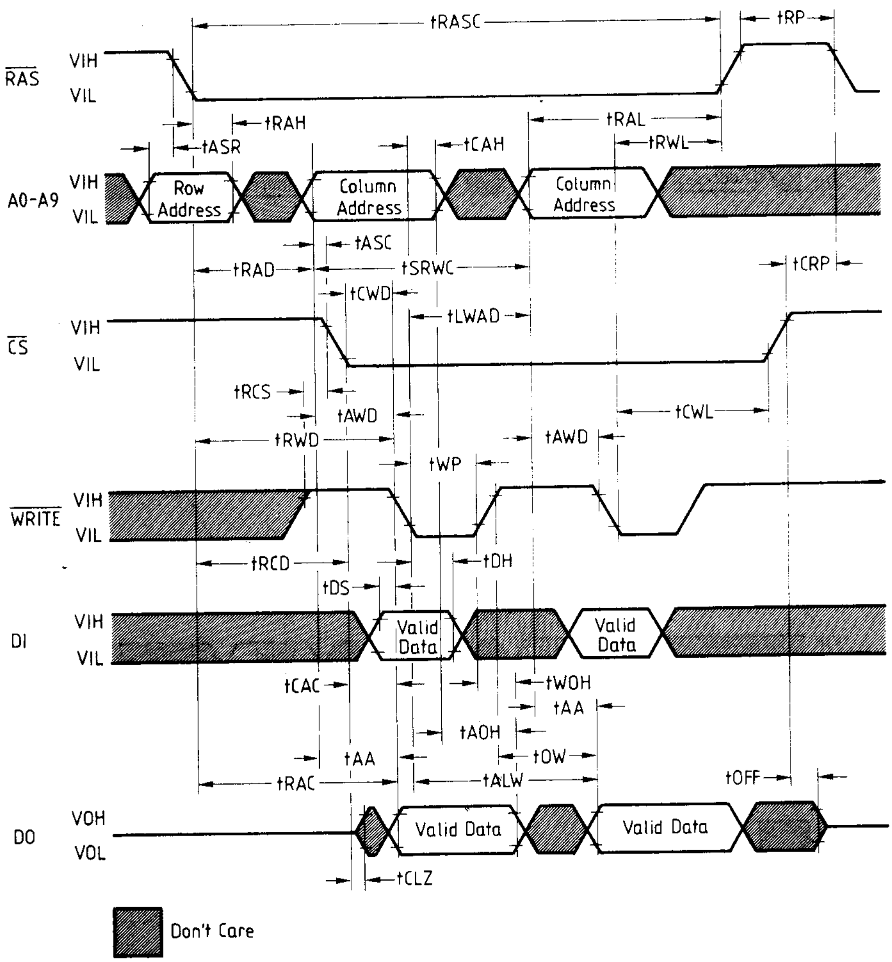
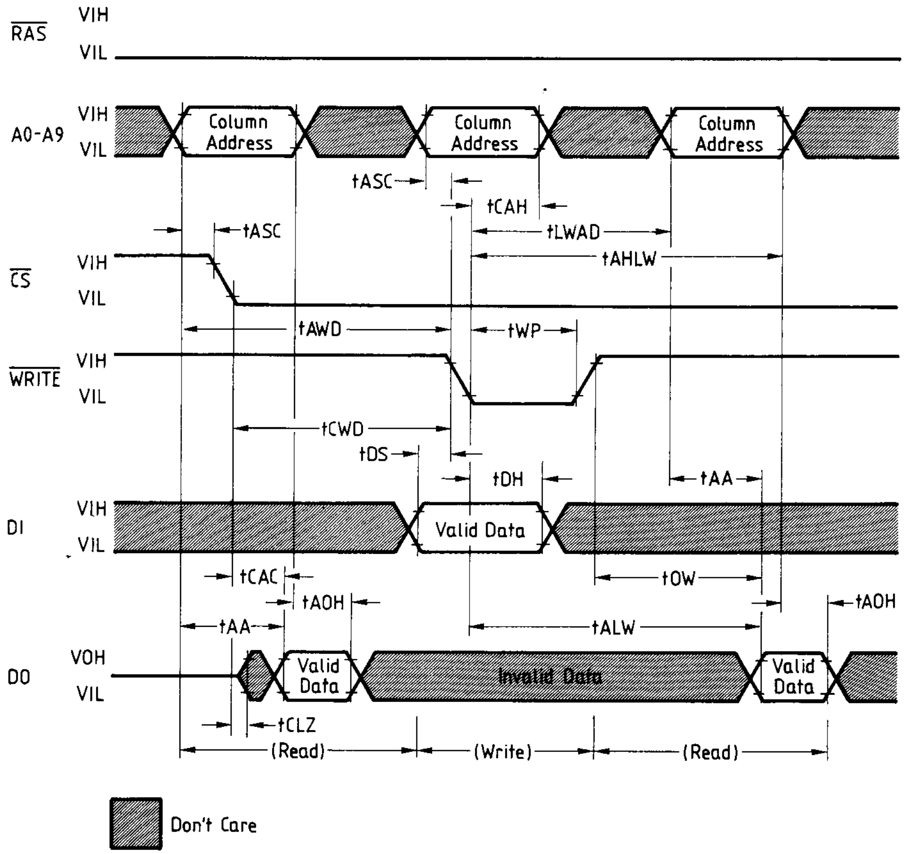
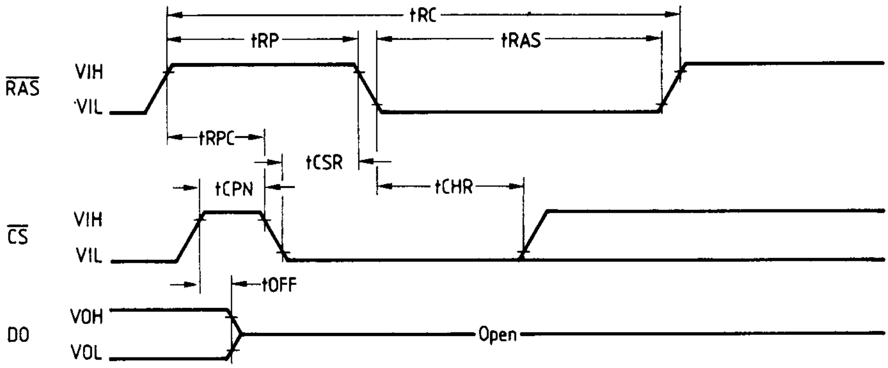
Static Column Mode Read-Write Cycle



Static Column Mode Read/Write Mixed Cycle

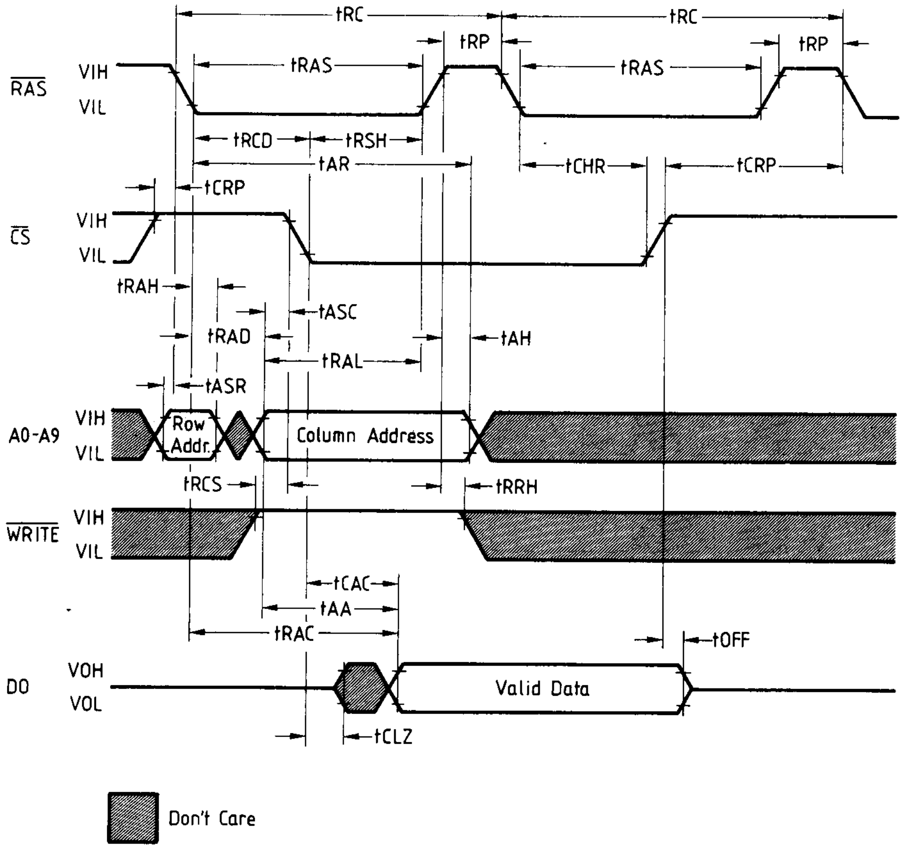


$\overline{CS}$-Before-$\overline{RAS}$ Refresh Cycle



Note: $\overline{WRITE}$=Don't Care, A0-A9=Don't Care

Hidden Refresh Cycle (read)



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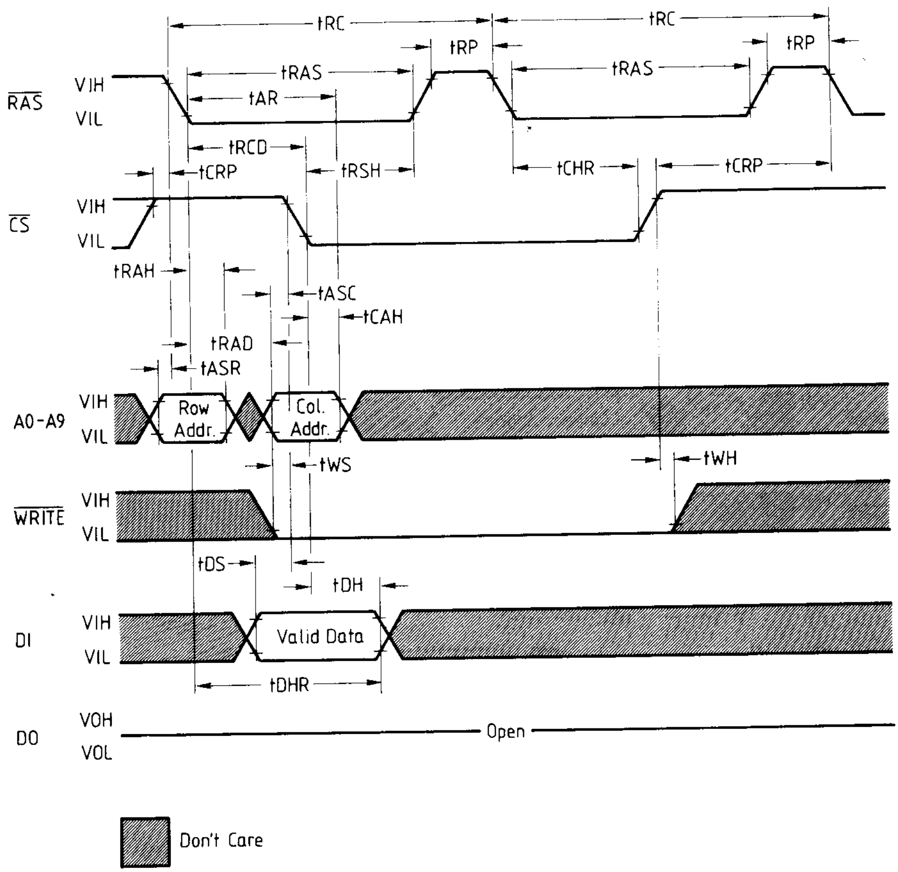
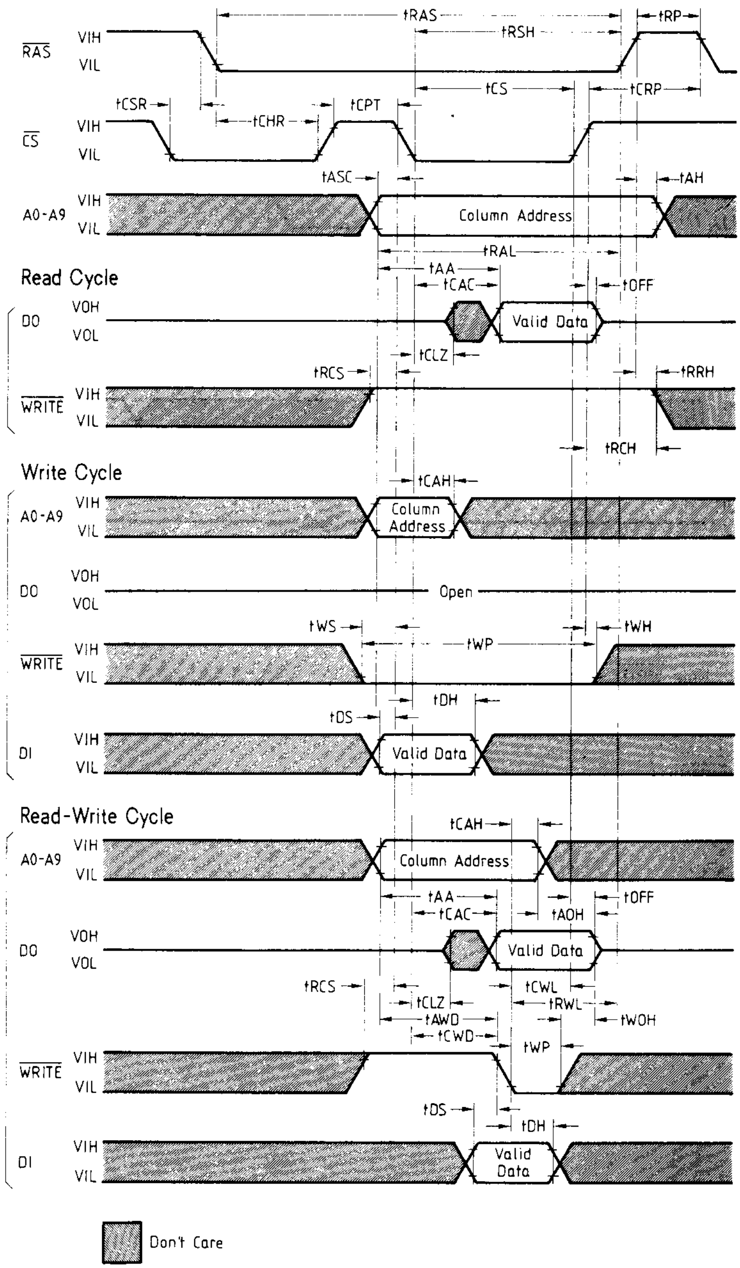
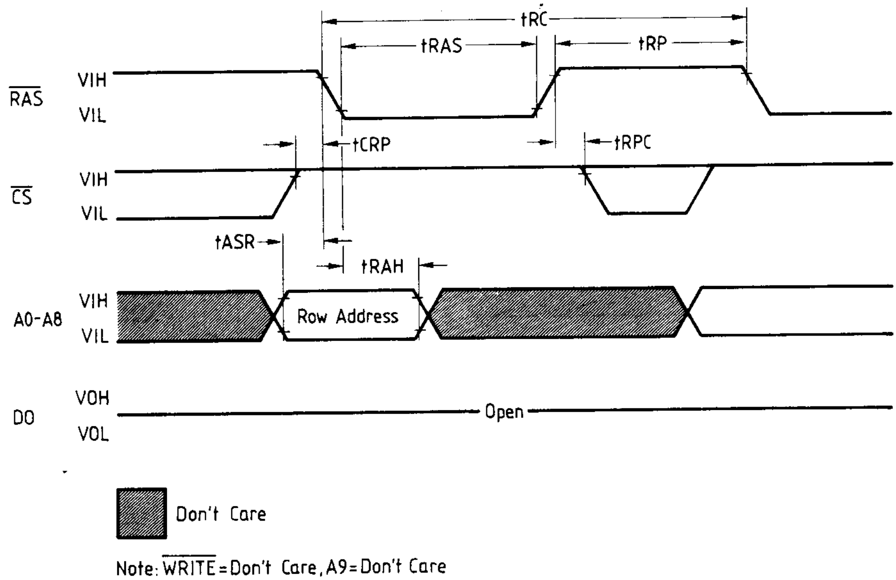
Hidden Refresh Cycle (write)



$\overline{CS}$-Before-$\overline{RAS}$ Refresh Counter Test Cycle



$\overline{RAS}$-Only Refresh Cycle



Address Decoder Scrambling of HYB 511002

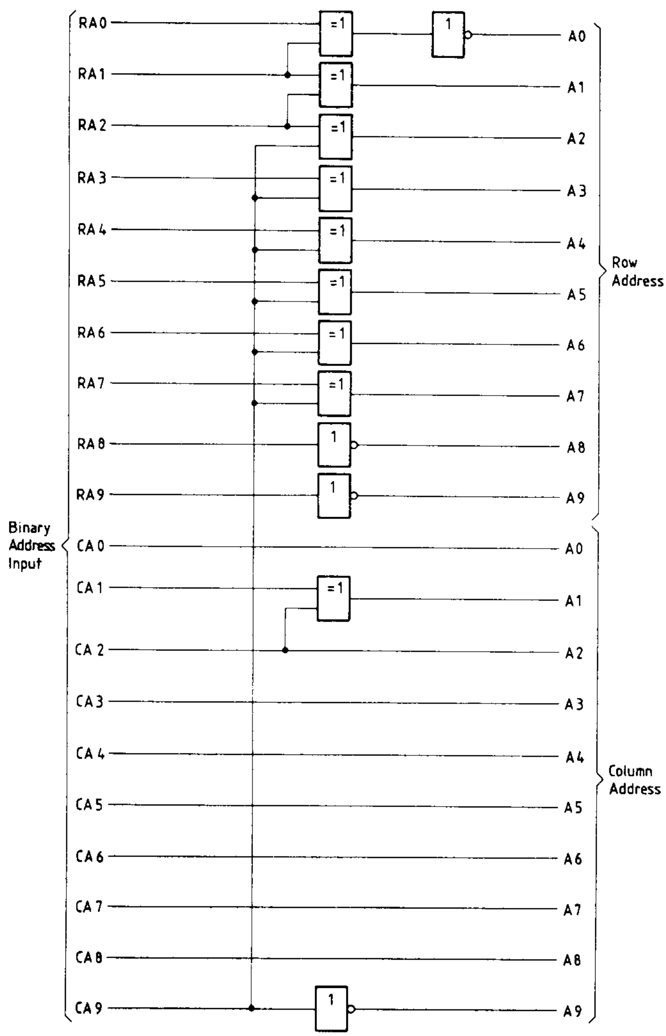
Internal Address Scrambling

The labels for address pins as given on the HYB 511002 data sheet were selected for marking convenience and do not reflect the internal least significant bit (LSB) to most significant bit (MSB) layout.

Address Decoder Scrambling

Efficient layout of the row and column decoders results in a scramble of the address inputs which must be observed if, for example, it is required that rows and columns be accessed in a "nearest neighbor" manner. The logic necessary to descramble is given in the next figure.

External Address Transformation Required to Descramble the HYB 511002 Internal Decoder (multiplexer not shown)



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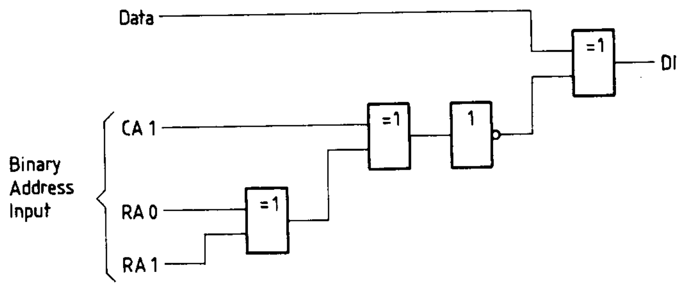
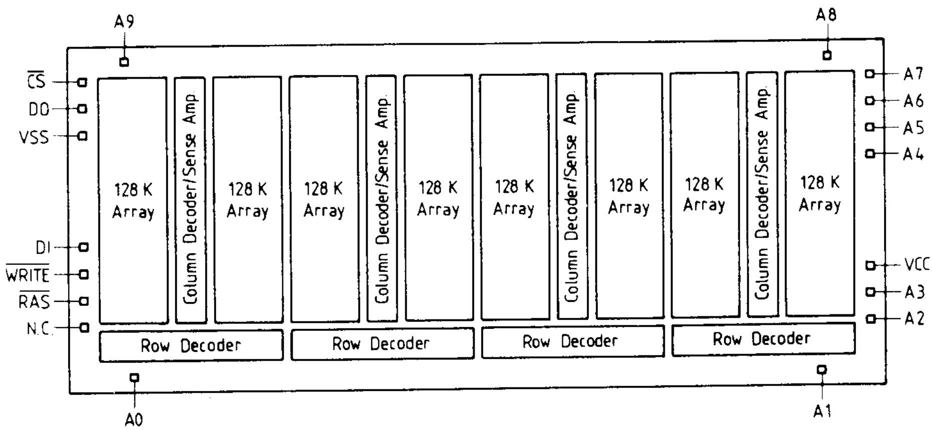
Data Polarity

Utilization of balanced sense amplifiers requires that one of the two halves of the matrix inverts data (this inversion is comprehended by internal circuitry so that it is transparent to user). If it is necessary, for example, to set all 1 megabits to a charged state, the data polarity in the next figure must be observed.

External Transformation Necessary to Counteract the Internal Inversion of Data within HYB 511002



Chip Layout of HYB 511002



Ordering Information

Type	Description
HYB511002-10	DRAM, access time 100 ns (P-DIP 18)
HYB511002-12	DRAM, access time 120 ns (P-DIP 18)

6