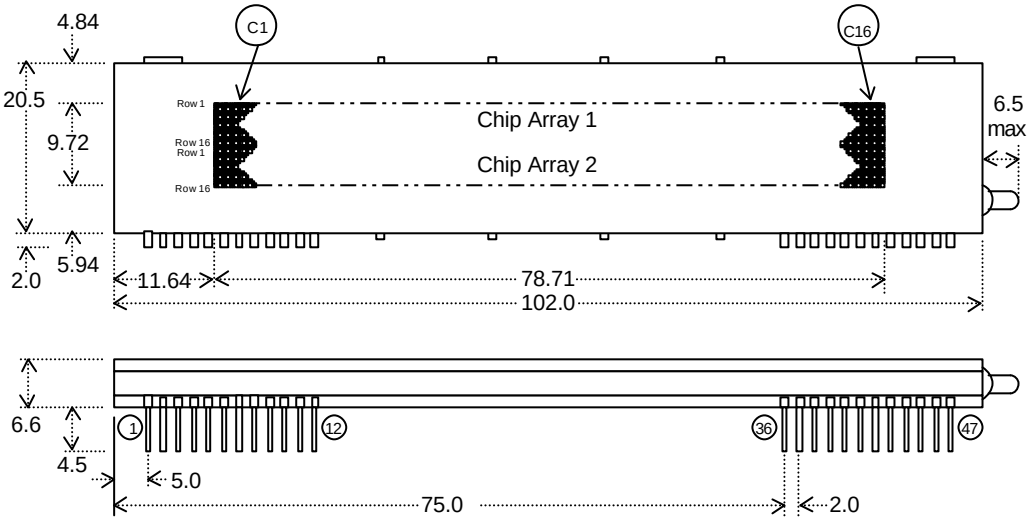
Active Matrix Graphic VFD — MW25632EB

- 256 x 32 Fine Dot Matrix
- Low Operating Voltage
- Ultra High Brightness Display
- Low RFI Static Drive
- Wide Operating Temperature

This compact high brightness active matrix VF display has 32 chips. Each chip has a 256 bit shift register latch driver organised as a 16 x 16 array. No refresh is required once the data is loaded. Consult our application notes for further information.



Dimensions in mm.
See full spec for tolerances.

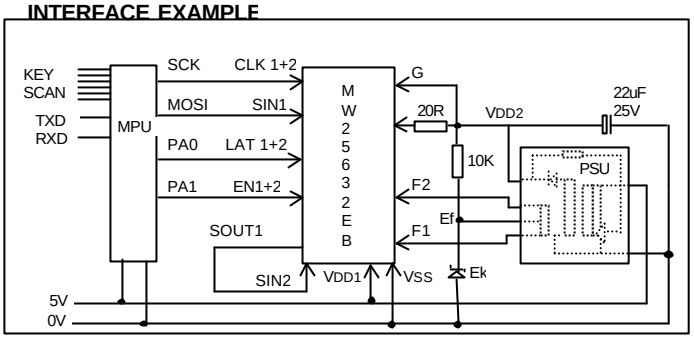
PIN OUT

Pin	Sig	Pin	Sig
1	F1	36	SIN1
2	F1	37	CLK1
3	F1	38	LAT1
4	SIN2	39	G
5	G	40	SOUT1
6	CLK2	41	V_{DD1}
7	LAT2	42	EN1
8	EN2	43	G
9	G	44	SOUT2
10	G_{ND}	45	F2
11	V_{DD2}	46	F2
12	NC	47	F2

ELECTRICAL SPECIFICATION

Parameter	Sym	Min	Typ	Max	Unit	Condition
Logic Voltage	V_{DD1}	4.5	5.0	5.5	V	V_{SS}=0V
Logic Current	I_{DD1}	-	30.0	45.0	mA	V_{DD1}=5V
Filament Voltage	Ef	4.0	4.4	4.8	Vac	G,V_{DD2}=0V
Filament Current	If	83.0	92.0	101.0	mAac	G,V_{DD2}=0V
Display Voltage	G,V_{DD2}	13.0	15.0	17.0	V	V_{SS}=0V
Display Current	I_C+I_{DD2}	-	24.0	36.0	mA	G,V_{DD2}=15V
Filament Bias	E_K	0.0	0.6	1.0	V	V_{SS}=0V
Logic High Input	V_{IH}	3.7	-	V_{DD1}	V	V_{SS}=0V
Logic Low Input	V_{IL}	0	-	1.3	V	V_{SS}=0V
Logic High Input	I_{IH}	-	-	0.5	µA	V_{DD1}=5V
Logic Low Input	I_{IL}	-1600	-342	-96	µA	V_{DD1}=5V

INTERFACE EXAMPLE

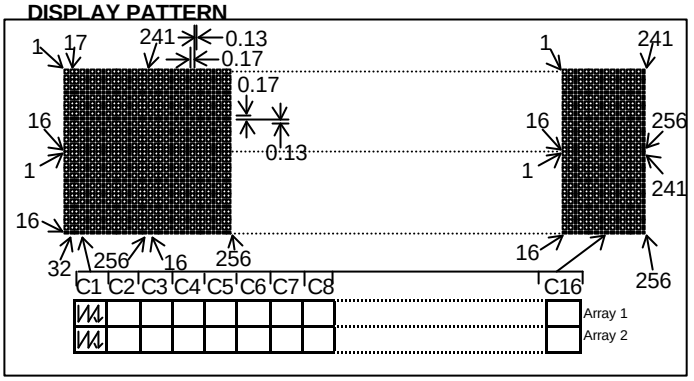


ENVIRONMENTAL and OPTICAL SPECIFICATION

Parameter	Value
Display Area (XxY mm)	78.71 x 9.72
Dot Size/Pitch (XxY mm)	0.17 x 0.17/0.308 x 0.308
Luminance	3500 cd/m^2 Typ
Colour of Illumination	Blue-Green (Filter for colours)
Operating Temperature	-40°C to +85°C
Storage Temperature	-50°C to +85°C
Operating Humidity (non condensing)	5 to 95% @ 25°C

1. The power on rise time should be less than 50ms.
2. Do not switch EN during a rising data hold.
3. The 20R resistor at the V_{DD2} input is required to prevent current surge during switching.
4. The filament supply (Ef) can be achieved by using semiconductor push-pull technology.

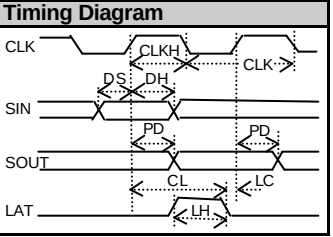
DISPLAY PATTERN



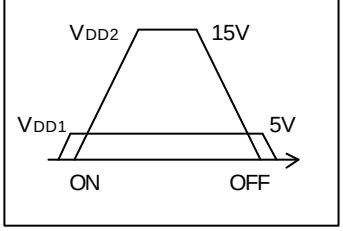
INTERFACE TIMING

Parameter	Time
CLK Cycle (CLK)	250ns min
CLK High (CLKH)	80ns min
SIN Setup (DS)	60ns min
SIN Hold (DH)	50ns min
SOUT Delay (PD)	50ns min
LAT High (LH)	220ns min
CLK then LAT (CL)	500ns min
LAT then CLK (LC)	120ns min

Timing Diagram



POWER SEQUENCE



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