OKI Semiconductor

MSC23837-xxBS18/DS18

Preliminary

8,388,608-Word by 36-Bit DRAM Module: Fast Page Mode

DESCRIPTION

The OKI MSC23837-xxBS18/DS18 is a fully decoded 8,388,608-word x 36-bit CMOS Dynamic Random Access Memory Module composed of eighteen 16-Mb DRAMs in SOJ (MSM5116400) packages mounted with eighteen 0.2 μF decoupling capacitors on a 72-pin glass epoxy single-inline package. This module is generally used for memory expansion in parity applications such as workstations.

FEATURES

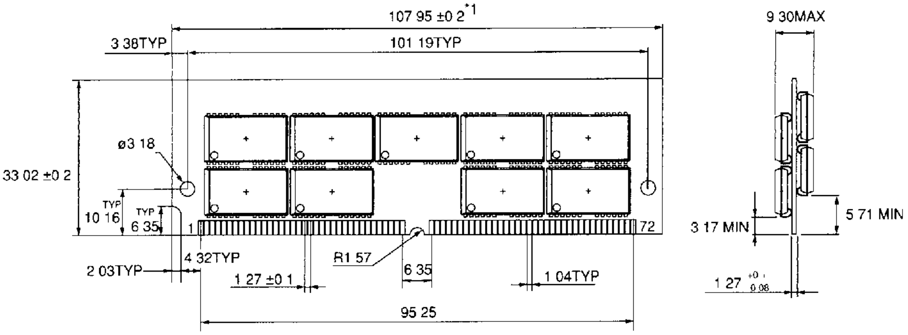
- 8-Meg x 36-bit organization
- 72-pin socket insertable module
  - MSC23837-xxBS18: Gold tab
  - MSC23837-xxDS18: Solder tab
- Single +5V supply ±5% tolerance
- Access times: 60, 70, 80 ns
- Input: TTL compatible
- Output: TTL compatible, three-state
- Refresh: 4096 cycles/64 ms
- $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh, $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ hidden refresh, $\overline{\text{RAS}}$-only refresh capability

Family Organization

Part Number	Access Time (Max)			Cycle Time (Min)	Power Dissipation (Max)	
	t_{RAC}	t_{AA}	t_{CAC}		Operating	Standby
MSC23837-60BS18/DS18	60 ns	30 ns	15 ns	110 ns	5198 mW	99 mW (MOS level)
MSC23837-70BS18/DS18	70 ns	35 ns	20 ns	130 ns	4703 mW	
MSC23837-80BS18/DS18	80 ns	40 ns	20 ns	150 ns	4208 mW	

PIN CONFIGURATION

MSC23837-xxBS18/DS18



*1 The common size difference of the board width 12 5mm of its height is specified as ±0 2 The value above 12 5mm is specified as ±0 5.

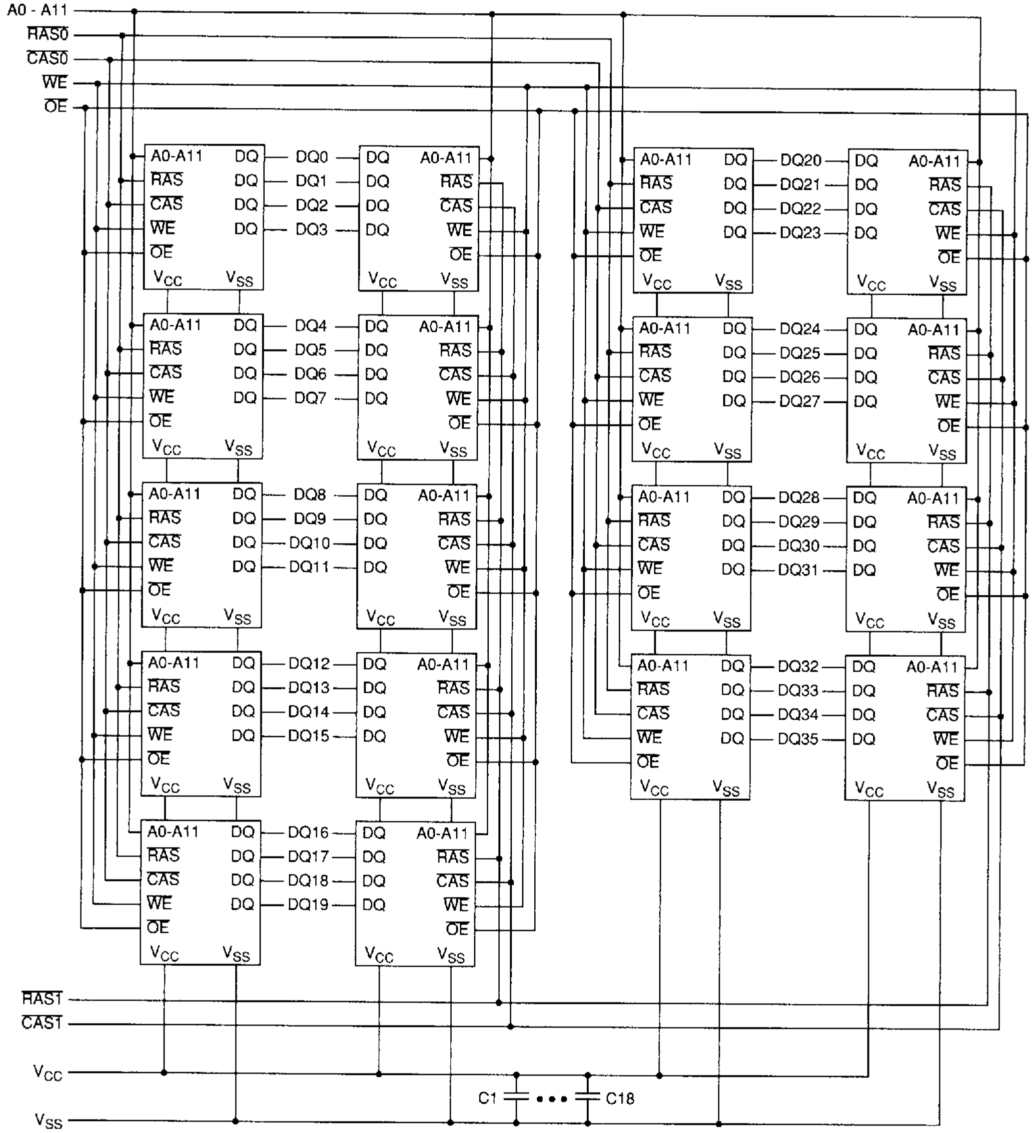
Pin Configuration

Pin Number	Pin Name	Pin Number	Pin Name	Pin Number	Pin Name	Pin Number	Pin Name	Pin Number	Pin Name
1	V_{SS}	16	A4	31	A8	46	DQ21	61	DQ33
2	DQ0	17	A5	32	A9	47	$\overline{WE}$	62	DQ34
3	DQ1	18	A6	33	N.C	48	N C	63	DQ35
4	DQ2	19	$\overline{OE}$	34	N.C	49	DQ22	64	N.C
5	DQ3	20	DQ8	35	DQ17	50	DQ23	65	N C
6	DQ4	21	DQ9	36	DQ18	51	DQ24	66	N.C
7	DQ5	22	DQ10	37	DQ19	52	DQ25	67	PD0
8	DQ6	23	DQ11	38	DQ20	53	DQ26	68	PD1
9	DQ7	24	DQ12	39	V_{SS}	54	DQ27	69	PD2
10	V_{CC}	25	DQ13	40	$\overline{CAS0}$	55	DQ28	70	PD3
11	PD4	26	DQ14	41	A10	56	DQ29	71	N C
12	A0	27	DQ15	42	A11	57	DQ30	72	V_{SS}
13	A1	28	A7	43	$\overline{CAS1}$	58	DQ31		
14	A2	29	DQ16	44	$\overline{RAS0}$	59	V_{CC}		
15	A3	30	V_{CC}	45	$\overline{RAS1}$	60	DQ32		

Presence Detect Pins

Pin Number	Pin Name	60 ns	70 ns	80 ns
67	PD0	N C.	N C	N C.
68	PD1	V_{SS}	V_{SS}	V_{SS}
69	PD2	N C.	V_{SS}	N C.
70	PD3	N C.	N C	V_{SS}
11	PD4	V_{SS}	V_{SS}	V_{SS}

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings [1]

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-1.0 ~ +7.0	V
Voltage V_{CC} supply relative to V_{SS}	V_{CC}	-1.0 ~ +7.0	V
Short circuit output current	I_{OS}	50	mA
Power dissipation	P_D	18	W
Operating temperature	T_{OPR}	0 ~ +70	°C
Storage temperature	T_{STG}	-40 ~ +125	°C

1 Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions (T_a = 0 ~ +70°C)

Parameter	Symbol	Rated Value			Unit
		Min	Typ	Max	
Power supply voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input high voltage	V_{IH}	2.4	-	6.5	V
Input low voltage	V_{IL}	-1.0	-	0.8	V

Capacitance (T_a = 25°C, f = 1 MHz) [1]

Parameter	Symbol	Typ	Max	Unit
Input capacitance (A0 ~ A11)	C_{IN1}	-	144	pF
Input capacitance ($\overline{\text{RAS0}}$, $\overline{\text{RAS1}}$, $\overline{\text{CAS0}}$, $\overline{\text{CAS1}}$)	C_{IN2}	-	83	pF
Input capacitance ($\overline{\text{WE}}$, $\overline{\text{OE}}$)	C_{IN3}	-	146	pF
I/O capacitance (DQ0~DQ35)	C_{DQ1}	-	30	pF

1 Capacitance measured with Boonton Meter

DC Characteristics (V_{CC} = 5 V ±10%, T_a = 0°C ~ +70°C)

Parameter	Symbol	Condition		60 ns		70 ns		80 ns		Unit	Note
				Min	Max	Min	Max	Min	Max		
Input leakage current	I_{LI}	0 V ≤ V_I ≤ 6 5 V; All other pins not under test = 0 V		-180	180	-180	180	-180	180	μA	
Output leakage current	I_{LO}	D_{OUT} disable 0 V ≤ V_O ≤ 5 5 V		-20	20	-20	20	-20	20	μA	
Output high voltage	V_{OH}	I_{OH} = -5 0 mA		2 4	V_{CC}	2 4	V_{CC}	2 4	V_{CC}	V	
Output low voltage	V_{OL}	I_{OL} = 4 2 mA		0	0 4	0	0 4	0	0 4	V	
Average power supply current (Operating)	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ cycling, t_{RC} = min.		-	945	-	855	-	765	mA	[1] [2]
Power supply current (Standby)	I_{CC2}	$\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IH}, D_{OUT} = Hi-Z	TTL	-	36	-	36	-	36	mA	
			MOS	-	18	-	18	-	18	mA	
Average power supply current ($\overline{RAS}$-only refresh)	I_{CC3}	$\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}, t_{RC} = min		-	945	-	855	-	765	mA	[1] [2]
Average power supply current ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	I_{CC6}	$\overline{RAS}$ cycling, $\overline{CAS}$-before-$\overline{RAS}$, t_{RC} = min		-	945	-	855	-	765	mA	[1]
Average power supply current (Fast Page Mode)	I_{CC7}	$\overline{RAS}$ = V_{IL} $\overline{CAS}$ cycling, t_{PC} = min		-	855	-	765	-	675	mA	[1] [3]

1. I_{CC} depends on output loading and cycle rates Specified values are obtained with the output open
2. Address can be changed once or less while $\overline{RAS}$ = V_{IL}
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}

AC Characteristics (V_{CC} = 5 V ±10%, T_a = 0°C ~ +70°C) [1] [2] [3]

Parameter	Symbol	60 ns		70 ns		80 ns		Unit	Note
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	110	-	130	-	150	-	ns	
Read modify write cycle time	t_{RMW}	155	-	185	-	205	-	ns	
Fast Page Mode cycle time	t_{PC}	40	-	45	-	50	-	ns	
Fast Page Mode read modify write cycle time	t_{PRMW}	85	-	100	-	105	0	ns	
Access time from $\overline{RAS}$	t_{RAC}	-	60	-	70	-	80	ns	[4] [5] [6]
Access time for $\overline{CAS}$	t_{CAC}	-	15	-	20	-	20	ns	[4] [5]
Access time from column address	t_{AA}	-	30	-	35	-	40	ns	[6]
Access time from $\overline{OE}$	t_{OEA}	-	15	-	20	-	20	ns	[4]
Access time from $\overline{CAS}$ precharge	t_{CPA}	-	35	-	40	-	45	ns	[4]
Output low impedance time from $\overline{CAS}$	t_{CLZ}	0	-	0	-	0	-	ns	
Output buffer turn-off delay time	t_{OFF}	0	15	0	20	0	20	ns	[7]
$\overline{OE}$ to data output buffer turn-off delay	t_{OEZ}	0	15	0	20	0	20	ns	[7]
Transition time	t_T	3	50	3	50	3	50	ns	[3]
Refresh period	t_{REF}	-	64	-	64	-	64	ms	
$\overline{RAS}$ precharge time	t_{RP}	40	-	50	-	60	-	ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10K	70	10K	80	10K	ns	
$\overline{RAS}$ pulse width (Fast Page Mode)	t_{RASP}	60	100K	70	100K	80	100K	ns	
$\overline{RAS}$ hold time	t_{RSH}	15	-	20	-	20	-	ns	
$\overline{RAS}$ hold time referenced to $\overline{OE}$	t_{ROH}	10	-	10	-	10	-	ns	
$\overline{CAS}$ precharge time (Fast Page Mode)	t_{CP}	10	-	10	-	10	-	ns	
$\overline{CAS}$ pulse width	t_{CAS}	15	10K	20	10K	20	10K	ns	
$\overline{CAS}$ hold time	t_{CSH}	60	-	70	-	80	-	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10	-	10	-	10	-	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	45	20	50	20	60	ns	[5]
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	15	40	ns	[6]
Row address set-up time	t_{ASR}	0	-	0	-	0	-	ns	
Row address hold time	t_{RAH}	10	-	10	-	10	-	ns	
Column address set-up time	t_{ASC}	0	-	0	-	0	-	ns	
Column address hold time	t_{CAH}	15	-	15	-	15	-	ns	
Column address hold time from $\overline{RAS}$	t_{AR}	50	-	55	-	60	-	ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	30	-	35	-	40	-	ns	
Read command set-up time	t_{RCS}	0	-	0	-	0	-	ns	
Read command hold time	t_{RCH}	0	-	0	-	0	-	ns	[8]
Read command hold time reference to $\overline{RAS}$	t_{RRH}	0	-	0	-	0	-	ns	[8]
Write command set-up time	t_{WCS}	0	-	0	-	0	-	ns	[9]
Write command hold time	t_{WCH}	10	-	15	-	15	-	ns	
Write command hold time from $\overline{RAS}$	t_{WCR}	45	-	55	-	60	-	ns	

AC Characteristics (V_{CC} = 5 V ±10%, T_a = 0°C ~ +70°C) [1] [2] [3] (Continued)

Parameter	Symbol	60 ns		70 ns		80 ns		Unit	Note
		Min	Max	Min	Max	Min	Max		
Write command pulse width	t_{WP}	10	-	10	-	10	-	ns	
$\overline{\text{OE}}$ command hold time	t_{OEH}	15	-	20	-	20	-	ns	
Write command to $\overline{\text{CAS}}$ lead time	t_{CWL}	15	-	20	-	20	-	ns	
Write command to $\overline{\text{RAS}}$ lead time	t_{RWL}	15	-	20	-	20	-	ns	
Data-in set-up time	t_{DS}	0	-	0	-	0	-	ns	
Data-in hold time	t_{DH}	15	-	15	-	15	-	ns	
Data-in hold time from $\overline{\text{RAS}}$	t_{DHR}	50	-	55	-	60	-	ns	
$\overline{\text{OE}}$ delay time	t_{OED}	15	-	20	-	20	-	ns	
$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ delay time	t_{CWD}	40	-	50	-	50	-	ns	[9]
$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ delay time	t_{RWD}	85	-	100	-	110	-	ns	[9]
Column address to $\overline{\text{WE}}$ delay time	t_{AWD}	55	-	65	-	70	-	ns	[9]
$\overline{\text{CAS}}$ active delay from $\overline{\text{RAS}}$ precharge	t_{RPC}	10	-	10	-	10	-	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ set-up time ($\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$)	t_{CSR}	10	-	10	-	10	-	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ hold time ($\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$)	t_{CHR}	20	-	20	-	20	-	ns	
$\overline{\text{CAS}}$ precharge time (Refresh counter test)	t_{CPT}	40	-	40	-	40	-	ns	
$\overline{\text{WE}}$ to $\overline{\text{RAS}}$ precharge time ($\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$)	t_{WRP}	10	-	10	-	10	-	ns	
$\overline{\text{WE}}$ hold time from $\overline{\text{RAS}}$ ($\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$)	t_{WRH}	10	-	10	-	10	-	ns	
$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ set-up time (Test mode)	t_{WSR}	10	-	10	-	10	-	ns	[10] [11]
$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ hold time (Test mode)	t_{WHR}	20	-	20	-	20	-	ns	[10] [11]
$\overline{\text{CAS}}$ precharge to $\overline{\text{WE}}$ delay time	t_{CPWD}	60	-	70	-	75	-	ns	[9]

1 A start-up delay of 200 µs is required after power-up followed by a minimum of eight initialization cycles ($\overline{\text{RAS}}$-only refresh or $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh) before proper device operation is achieved When using the internal refresh counter, a minimum of eight $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ initialization cycles is required

2 AC measurements assume t_T = 5 ns

3 V_{IH} (min) and V_{IL} (max) are reference levels for measuring input timing signals Transition times are measured between V_{IH} and V_{IL}

4 Measured with a load circuit equivalent to 2 TTL + 100 pF

5 Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met t_{RCD} (max) is specified as a reference point only If t_{RCD} is greater than the specified t_{RCD} (max) limit, access time is controlled by t_{CAC}

6 Operation within the t_{RAD} (max.) limit ensures that t_{RAC} (max.) can be met t_{RAD} (max.) is specified as a reference point only If t_{RAD} is greater than the specified t_{RAD} (max) limit, access time is controlled by t_{AA}

7. t_{OFF} (max) and t_{OEZ} (max) defines the time at which the output achieves an open circuit condition and is not referenced to output voltage levels

8 t_{RCH} or t_{RRH} must be satisfied for a read cycle

9 t_{WCS}, t_{CWD}, t_{RWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameters They are included in the data sheet as electrical characteristics only. If $t_{WCS} \ge t_{WCS}$ (min), the cycle is an early write cycle and the data output pin will remain in a high impedance state throughout the entire cycle If t_{CWD} (min), $t_{RWD} \ge t_{RWD}$ (min.), $t_{AWD} \ge t_{AWD}$ (min) and tCPWD ≥ tCPWD (min), the cycle is a read modify write cycle and the data output pin will contain data read from the selected cell If neither condition is satisfied, the data output logic state (at access time) is undefined

10 The test mode is initiated by performing a $\overline{\text{WE}}$ and $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh cycle This mode is latched and remains in effect until the exit cycle is generated The test mode specified in this data sheet is a 4-bit parallel test function. CA1 and CA0 are not used In a read cycle, if all internal bits are equal the data I/O pin will indicate a high level If any internal bits are not equal, the data I/O pin will indicate a low level The test mode is cleared and the memory device returned to its normal operating state by performing a $\overline{\text{RAS}}$-only refresh cycle or a $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh cycle

11 In a test mode read cycle, the access time parameters are delayed by 5 ns Test mode parameters are obtained by adding 5 ns to the normal read cycle values