



**PIN NAME**

#	NAME	#	NAME	#	NAME	#	NAME
1	Vss	43	Vss	85	Vss	127	Vss
2	DQ0	44	OE2	86	DQ32	128	NC
3	DQ1	45	RAS2	87	DQ33	129	NC
4	DQ2	46	CAS4	88	DQ34	130	CAS5
5	DQ3	47	CAS6	89	DQ35	131	CAS7
6	Vcc	48	WE2	90	Vcc	132	PDE
7	DQ4	49	Vcc	91	DQ36	133	Vcc
8	DQ5	50	NC	92	DQ37	134	NC
9	DQ6	51	NC	93	DQ38	135	NC
10	DQ7	52	DQ16	94	DQ39	136	DQ48
11	NC	53	DQ17	95	NC	137	DQ49
12	Vss	54	Vss	96	Vss	138	Vss
13	DQ8	55	DQ18	97	DQ40	139	DQ50
14	DQ9	56	DQ19	98	DQ41	140	DQ51
15	DQ10	57	DQ20	99	DQ42	141	DQ52
16	DQ11	58	DQ21	100	DQ43	142	DQ53
17	DQ12	59	Vcc	101	DQ44	143	Vcc
18	Vcc	60	DQ22	102	Vcc	144	DQ54
19	DQ13	61	NC	103	DQ45	145	NC
20	DQ14	62	NC	104	DQ46	146	NC
21	DQ15	63	NC	105	DQ47	147	NC
22	NC	64	NC	106	NC	148	NC
23	Vss	65	DQ23	107	Vss	149	DQ55
24	NC	66	NC	108	NC	150	NC
25	NC	67	DQ24	109	NC	151	DQ56
26	Vcc	68	Vss	110	Vcc	152	Vss
27	WE0	69	DQ25	111	NC	153	DQ57
28	CAS0	70	DQ26	112	CAS1	154	DQ58
29	CAS2	71	DQ27	113	CAS3	155	DQ59
30	RAS0	72	DQ28	114	NC	156	DQ60
31	OE0	73	Vcc	115	NC	157	Vcc
32	Vss	74	DQ29	116	Vss	158	DQ61
33	A0	75	DQ30	117	A1	159	DQ62
34	A2	76	DQ31	118	A3	160	DQ63
35	A4	77	NC	119	A5	161	NC
36	A6	78	Vss	120	A7	162	Vss
37	A8	79	PD1	121	A9	163	PD2
38	A10	80	PD3	122	A11	164	PD4
39	NC	81	PD5	123	NC	165	PD6
40	Vcc	82	PD7	124	Vcc	166	PD8
41	NC	83	ID0(Vss)	125	NC	167	ID1
42	NC	84	Vcc	126	B0	168	Vcc

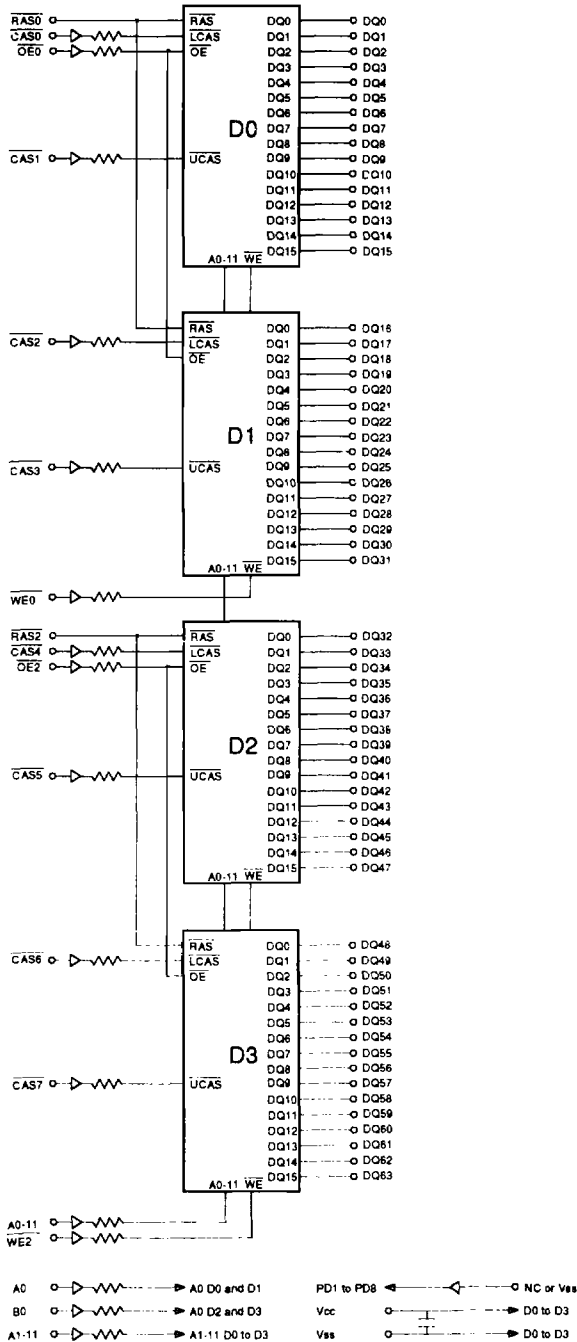
**PRESENCE DETECT PINS**

PIN	PD1	PD2	PD3	PD4	PD5	PD6	PD7	PD8	ID0	ID1
-60	Vss	NC	NC	Vss	NC	NC	NC	NC	Vss	Vss or NC
-70	Vss	NC	NC	Vss	NC	Vss	NC	NC	Vss	Vss or NC
-80	Vss	NC	NC	Vss	NC	NC	Vss	NC	Vss	Vss or NC

**NOTE :**

1. PDs are either open NC or driven to Vss via on-board buffer circuits.
2. IDs are connected directly to NC or Vss without a buffer.
3. ID1 will be either open NC for Self-Refresh or driven to Vss for standard.

BLOCK DIAGRAM



NOTE : All resistors are 25 Ohm± 5%

**ABSOLUTE MAXIMUM RATINGS**

SYMBOL	PARAMETER	RATING	UNIT
TA	Ambient Temperature	0 to 70	°C
TSTG	Storage Temperature	-55 to 150	°C
VIN, VOUT	Voltage on Any Pin Relative to Vss	-0.5 to 4.6	V
VCC	Voltage on VCC Relative to Vss	-0.5 to 4.6	V
Ios	Short Circuit Output Current	50	mA
Pd	Power Dissipation	7.7	W

NOTE : Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

**RECOMMENDED DC OPERATING CONDITIONS**

(TA= 0°C to 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
VCC	Supply Voltage	3.0	3.3	3.6	V
VSS	Ground	0	0	0	V
VIH	Input High Voltage	2.0	-	VCC+ 0.3	V
VIL	Input Low Voltage	-0.3	-	0.8	V

NOTE : All voltages are referenced to Vss.

**DC CHARACTERISTICS**

(TA= 0°C to 70°C, VCC= 3.3V± 10%, VSS= 0V, unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS	SPEED/ POWER	MIN.	MAX.	UNIT	NOTE
ILI	Input Leakage Current (Any Input Pin)	VSS ≤ VIN ≤ VCC + 0.3V, other pins not under test = VSS	All but RAS RAS	-10 -20	10 20	μA	
ILO	Output Leakage Current (High Impedance State)	VSS ≤ VOUT ≤ VCC, RAS & CAS at VIH		-10	10	μA	
ICC1	VCC Supply Current, Operating	tRC = tRC (min.)	60 70 80	- - -	400 360 320	mA	1,2,3
ICC2	VCC Supply Current, TTL Standby	RAS & CAS at VIH, other inputs ≥ VSS		-	4.43	mA	
ICC3	VCC Supply Current, RAS-only refresh	tRC = tRC (min.)	60 70 80	- - -	400 360 320	mA	1,3
ICC4	VCC Supply Current, EDO mode	tHPC = tHPC (min.)	60 70 80	- - -	400 360 320	mA	1,2,3
ICC5	VCC Supply Current, CMOS Standby	RAS & CAS ≥ VCC - 0.2V	SL-part	- -	4.43 1.23	mA	
ICC6	VCC Supply Current, CAS-before-RAS refresh	tRC = tRC (min.)	60 70 80	- - -	400 360 320	mA	1,3
ICC7	VCC Supply Current, Battery Back Up (SL-part only)	tRC = 62.5μs CAS = CBR cycling or 0.2V, WE = VCC - 0.2V, A0-A11 = VCC - 0.2V or 0.2V DQ0-DQ63 = VCC 0.2V, 0.2V or open	tRAS ≤ 300ns  tRAS ≤ 1μs	- - -	1.83 2.23	mA	1,4,5
ICC8	VCC Supply Current, Self-Refresh (SL-part only)	RAS & CAS ≤ 0.2V other pins same as ICC7		-	1.83	mA	5
VOL	Output Low Voltage	IOL = 2.0mA		-	0.4	V	
VOH	Output High Voltage	IOH = -2.0mA		2.4			

**NOTE:**

1. ICC1, ICC3, ICC4, ICC6 and ICC7 depend on cycle rate.
2. ICC1, ICC3, ICC4, and ICC6 depend on output loading. Specified values are obtained with the output open.
3. ICC is specified as average current. For ICC1, ICC3 and ICC6, address can be changed maximum two times while RAS = VIL. For ICC4, address can be changed maximum once while CAS = VIH.
4. tRAS (max.) = 1μs only applied to refresh of battery backup but tRAS (max.) = 10μs is applied to normal functional operating.
5. ICC5 (max.) = 1.23mA, ICC7 and ICC8 are applied to SL-part only (HYM5V64104ASLXG/ASLTXG)

**AC CHARACTERISTICS**

(TA= 0°C to 70°C, VCC= 3.3V± 10%, VSS= 0V, unless otherwise noted.) NOTE : 1, 2, 3

#	SYMBOL	PARAMETER	HYM5V64104A X-Series						UNIT	NOTE
			-60		-70		-80			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
1	tRC	Random Read or Write Cycle Time	105	-	125	-	145	-	ns	
2	tRWC	Read-Modify-Write Cycle Time	150	-	175	-	195	-	ns	14,15
3	tHPC	EDO Mode Cycle Time	25	-	30	-	35	-	ns	
4	tHPRWC	EDO Mode Read-Modify-Write Cycle Time	68	-	73	-	78	-	ns	13,15
5	tRAC	Access Time from RAS	-	60	-	70	-	80	ns	4,9,10
6	tCAC	Access Time from CAS	-	22	-	25	-	25	ns	4,9,15
7	tAA	Access Time from Column Address	-	36	-	41	-	46	ns	4,10,15
8	tCPA	Access Time from CAS Precharge	-	40	-	40	-	45	ns	4,15
9	tCLZ	CAS to Output Low Impedance	2	-	2	-	2	-	ns	4,13
10	tOFF	Output Buffer Turn-off Delay	0	20	0	20	0	20	ns	5,17
11	tT	Transition Time (Rise and Fall)	2.5	50	2.5	50	2.5	50	ns	3,12
12	tRP	RAS Precharge Time	40	-	50	-	60	-	ns	
13	tRAS	RAS Pulse Width	60	10K	70	10K	80	10K	ns	
14	tRASP	RAS Pulse Width (EDO Mode)	60	100K	70	100K	80	100K	ns	
15	tRSH	RAS Hold Time	18	-	20	-	25	-	ns	15
16	tCSH	CAS Hold Time	38	-	48	-	58	-	ns	14
17	tCAS	CAS Pulse Width	13	10K	15	10K	20	10K	ns	
18	tRCD	RAS to CAS Delay	18	40	18	45	18	55	ns	9,16
19	tRAD	RAS to Column Address Delay Time	13	24	13	29	13	34	ns	10,16
20	tCRP	CAS to RAS Precharge Time	5	-	5	-	5	-	ns	15
21	tCP	CAS Precharge Time	7	-	10	-	10	-	ns	
22	tASR	Row Address Set-up Time	6	-	6	-	6	-	ns	15
23	tRAH	Row Address Hold Time	8	-	8	-	8	-	ns	14
24	tASC	Column Address Set-up Time	2	-	2	-	2	-	ns	13
25	tCAH	Column Address Hold Time	17	-	17	-	17	-	ns	13
26	tAR	Column Address Hold Time from RAS	28	-	28	-	28	-	ns	14
27	tRAL	Column Address to RAS Lead Time	36	-	41	-	46	-	ns	15
28	tRCS	Read Command Set-up Time	2	-	2	-	2	-	ns	13
29	tRCH	Read Command Hold Time Referenced to CAS	2	-	2	-	2	-	ns	6,13
30	tRRH	Read Command Hold Time Referenced to RAS	-2	-	-2	-	-2	-	ns	6,14
31	tWCH	Write Command Hold Time	12	-	17	-	17	-	ns	13
32	tWCR	Write Command Hold Time from RAS	53	-	53	-	58	-	ns	14
33	tWP	Write Command Pulse Width	10	-	10	-	10	-	ns	
34	tRWL	Write Command to RAS Lead Time	20	-	20	-	20	-	ns	15
35	tCWL	Write Command to CAS Lead Time	15	-	17	-	22	-	ns	13
36	tDS	Data-In Set-up Time	-2	-	-2	-	-2	-	ns	7,14
37	tDH	Data-In Hold Time	15	-	20	-	20	-	ns	7,15
38	tDHR	Data-In Hold Time Referenced to RAS	53	-	53	-	58	-	ns	14
39	tREF	Refresh Period (4096 cycles)		64		64		64	ms	18
		SL-part		256		256		256		
40	tWCS	Write Command Set-up Time	2	-	2	-	2	-	ns	8,13

**AC CHARACTERISTICS**

(continued)

#	SYMBOL	PARAMETER	HYM5V64104A X-Series						UNIT	NOTE
			-60		-70		-80			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
41	tCWD	CAS to WE Delay Time	47	-	55	-	55	-	ns	8,15
42	tRWD	RAS to WE Delay Time	83	-	98	-	108	-	ns	8,14,15
43	tAWD	Column Address to WE Delay Time	59	-	69	-	74	-	ns	8,14,15
44	tCSR	CAS Set-up Time (CBR Cycle)	10	-	10	-	10	-	ns	15
45	tCHR	CAS Hold Time (CBR Cycle)	8	-	8	-	8	-	ns	14
46	tRPC	RAS to CAS Precharge Time	3	-	3	-	3	-	ns	14
47	tCPT	CAS Precharge Time (CBR Counter Test)	30	-	35	-	40	-	ns	
48	tROH	RAS Hold Time Referenced to OE	15	-	15	-	15	-	ns	15
49	tOEA	OE Access Time	-	22	-	25	-	25	ns	15
50	tOED	OE to Data Delay	20	-	25	-	25	-	ns	15
51	tOEZ	Output Buffer Turn Off Delay Time from OE	2	20	2	20	2	20	ns	5,17
52	tOEH	OE Command Hold Time	15	-	20	-	20	-	ns	
53	tCPWD	WE Delay Time from CAS Precharge	63	-	73	-	83	-	ns	8,14,15
54	tRHCP	RAS Hold Time from CAS Precharge	42	-	42	-	52	-	ns	13
55	tPD	PDE to Valid Presence Detect Data	-	10	-	10	-	10	ns	11
56	tPDOFF	PDE Inactive to Presence Detects Inactive	2	-	2	-	2	-	ns	12
57	tWRP	WE to RAS Precharge Time (CBR Cycle)	10	-	10	-	10	-	ns	
58	tWRH	WE to RAS Hold Time (CBR Cycle)	8	-	8	-	8	-	ns	
59	tRASS	RAS Pulse Width (Self Refresh Cycle)	100	-	100	-	100	-	ns	
60	tRPS	RAS Precharge Time (Self Refresh Cycle)	110	-	130	-	150	-	ns	
61	tCHS	CAS Hold Time (Self Refresh Cycle)	48	-	48	-	48	-	ns	
62	tDOH	Output Data Hold Time	7	-	7	-	7	-	ns	
63	tREZ	Output Buffer Turn Off Delay Time from RAS	2	20	2	20	2	20	ns	5, 21
64	tWEZ	Output Buffer Turn Off Delay Time from WE	2	20	2	20	2	20	ns	5
65	tWED	WE to Data Delay Time	20	-	20	-	20	-	ns	
66	tOEP	OE High Pulse Width	10	-	10	-	10	-	ns	
67	tWPE	WE Pulse Width for Out Disable When CAS High	10	-	10	-	10	-	ns	
68	tOCH	OE to CAS Hold Time	0	-	0	-	0	-	ns	
69	tCHO	CAS Hold Time to OE	5	-	5	-	5	-	ns	

**NOTE :**

1. An initial pause of 200µs is required after power-up followed by 8  $\overline{RAS}$  cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8  $\overline{CAS}$ -before- $\overline{RAS}$  initialization cycles instead of 8  $\overline{RAS}$ -only refresh cycles are required. The device should be carefully initialized to be prevented from being entered into multi bit test mode.
2. If  $\overline{RAS} = V_{SS}$  during power-up, the HYM5V64104A could begin an active cycle. This condition results in higher power-up current than necessary demands from the power-up. It is recommended that  $\overline{RAS}$  and  $\overline{CAS}$  track with  $V_{CC}$  during power-up or be held at a valid  $V_{IH}$  in order to minimize the power-up current.
3. Refer to the HY51V16164A data sheet for detailed information.
4. Measured at  $V_{OH} = 2.4V$  and  $V_{OL} = 0.4V$  with a load equivalent to 1 TTL loads and 100pF. ( $V_{OH} = 2.0V$ ,  $V_{OL} = 0.8V$ )
5.  $t_{CEZ}(\text{max.})$ ,  $t_{OEZ}(\text{MAX.})$ ,  $t_{REZ}(\text{MAX.})$  and  $t_{WEZ}(\text{MAX.})$  define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
6. Either  $t_{RCH}$  or  $t_{RRH}$  must be satisfied for a read cycle.
7. These parameters are referenced to  $\overline{CAS}$  leading edge in early write cycles and to  $\overline{WE}$  leading edge in late write or read-modify-write cycles.
8.  $t_{WCS}$  is not a restrictive operating parameter. It is included in the data sheet as electrical characteristics only. If  $t_{WCS} \geq t_{WCS}(\text{min.})$ , the cycle is an early write cycle and data out pin will remain open circuit (high impedance) through the entire cycle.
9. Operation within the  $t_{RCD}(\text{max.})$  limit insures that  $t_{RAC}(\text{max.})$  can be met.  $t_{RCD}(\text{max.})$  is specified as a reference point only. If  $t_{RCD}$  is greater than the specified  $t_{RCD}(\text{max.})$  limit, then access time is controlled by  $t_{CAC}$ .
10. Operation within the  $t_{RAD}(\text{max.})$  limit insures that  $t_{RAC}(\text{max.})$  can be met.  $t_{RAD}(\text{max.})$  is specified as a reference point only. If  $t_{RAD}$  is greater than the specified  $t_{RAD}(\text{max.})$  limit, then access time is controlled by  $t_{AAC}$ .
11. Measured with the specified current load and 100pF.
12.  $t_{PDOFF}(\text{max.})$  is determined by the pull-up resistor value. Care must be taken to ensure adequate recovery time prior to reading valid up-level on subsequent SIMM position.
13. A + 2ns timing skew from the DRAM to the DIMM resulted from the addition of buffers (DRAM loading may add to skew).
14. A -2ns timing skew from the DRAM to the DIMM resulted from the addition of buffers (DRAM loading may add to skew).
15. A + 5ns ( $\overline{CAS}, \overline{WE}, \overline{OE}$ ) or + 6ns (address) timing skew from the DRAM to the DIMM resulted from the addition of buffers. (DRAM loading may add skew).
16. A -2ns min and a -5ns ( $\overline{CAS}, \overline{WE}, \overline{OE}$ ) or -6ns (address) max timing skew from the DRAM to the DIMM resulted from the addition of buffers. (DRAM loading may add to skew).
17. A + 2ns min and a + 5ns ( $\overline{CAS}, \overline{WE}, \overline{OE}$ ) or + 6ns (address) max timing skew from the DRAM to the DIMM resulted from the addition of buffers. (DRAM loading may add to skew).
18. A burst of 4096  $\overline{CAS}$ -before- $\overline{RAS}$  refresh cycles must be executed within 64ms after exiting self refresh (for SL-part).
19. If  $t_{CWD} \geq t_{WCS}(\text{MIN.})$ ,  $t_{RWD} \geq t_{RWD}(\text{MIN.})$ ,  $t_{AWD} \geq t_{AWD}(\text{MIN.})$  and  $t_{CPWD} \geq t_{CPWD}(\text{MIN.})$ , the cycle is a read modify write cycle and the data output will contain data read from the selected cell. If neither of the above conditions are met, the condition of the data out (at access time and until  $\overline{CAS}$  goes back to  $V_{IH}$ ) is indeterminated.
20. In  $\overline{CAS}$  before  $\overline{RAS}$  self refresh mode.  
 In case of using distributed  $\overline{CAS}$  before  $\overline{RAS}$  refresh, refresh 4096 times during a 256ms after reset  
 In case of using burst  $\overline{CAS}$  before  $\overline{RAS}$  refresh, refresh 4096 times during a 64ms after reset  
 In case of using  $\overline{RAS}$  only refresh, refresh against all refresh address during 64ms after reset
21. If  $\overline{RAS}$  goes to high before  $\overline{CAS}$  high going, the open circuit condition of the output is achieved by  $\overline{CAS}$  high going. If  $\overline{CAS}$  goes to high before  $\overline{RAS}$  high going, the open circuit condition of the output is achieved by  $\overline{RAS}$  high going.

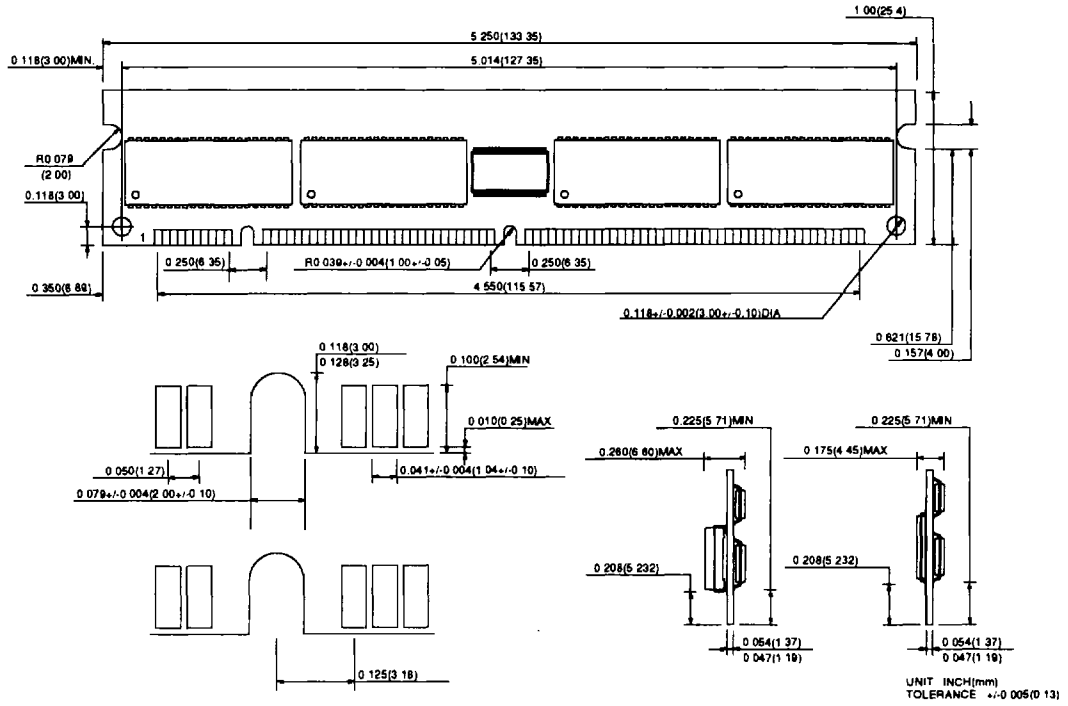
**CAPACITANCE**

( $T_A = 25^\circ\text{C}$ ,  $V_{CC} = 3.3V \pm 10\%$ ,  $V_{SS} = 0V$ ,  $f = 1\text{MHz}$ , unless otherwise noted.)

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
CIN1	Input Capacitance (A0-A11,B0)	-	13	pF
CIN2	Input Capacitance ( $\overline{RAS0}, \overline{RAS2}$ )	-	25	pF
CIN3	Input Capacitance ( $\overline{CAS0} - \overline{CAS7}, \overline{WE0}, \overline{WE2}, \overline{OE0}, \overline{OE2}$ )	-	13	pF
CDQ	Data Input/Output Capacitance (DQ0-DQ63)	-	15	pF

**PACKAGE INFORMATION**

**168 pin Dual In-line Memory Module (XG ; Gold plated)**



**ORDERING INFORMATION**

PART NUMBER	SPEED	POWER	PACKAGE	PLATING
HYM5V64104AXG	60/70/80		DIMM	Gold
HYM5V64104ASLXG	60/70/80	SL-part	DIMM	Gold
HYM5V64104ATXG	60/70/80		DIMM	Gold
HYM5V64104ASLTXG	60/70/80	SL-part	DIMM	Gold