SONY

5 Laser Diode Driver for Laser Projector

CXA4007ER

Description

The CXA4007ER is a laser diode driver IC for Laser Beam Scanning type Laser projector

Features

◆ LD Driver
- ◆ 5ch Laser Driver
  - Red-2ch, Green-2ch and Blue LDs are available
- ◆ Maximum driving current
  - Red outputs : Total = 575 mA (each channel: BASE current = 75 mA, VIDEO current = 500 mA)
  - Blue output : Total = 238 mA (each channel: BASE current = 38 mA, VIDEO current = 200 mA)
  - Green outputs : Total = 375 mA (each channel: BASE current = 75 mA, VIDEO current = 300 mA)
- ◆ Programmable snubber waveform compensation
- ◆ Programmable HFM frequency
  - Frequency: 100 MHz ～ 500 MHz
- ◆ Programmable HFM spread spectrum function
- ◆ Built-in HFM frequency counter

◆ VIDEO Data
- ◆ Single transmission
  - Built-in SSTL receiver, which can receive LVCMOS 1.8 V

◆ Laser Power Control
- ◆ 10bits – VIDEO DAC (VDAC)
  - Maximum operating pixel frequency : 200MHz
- ◆ Programmable BASE current, VIDEO current
  - BASE current: BASEx (10bits), VIDEO current: FSx (10bits)

Package

56PIN VQFN (Plastic)

Structure

CMOS IC

Contents

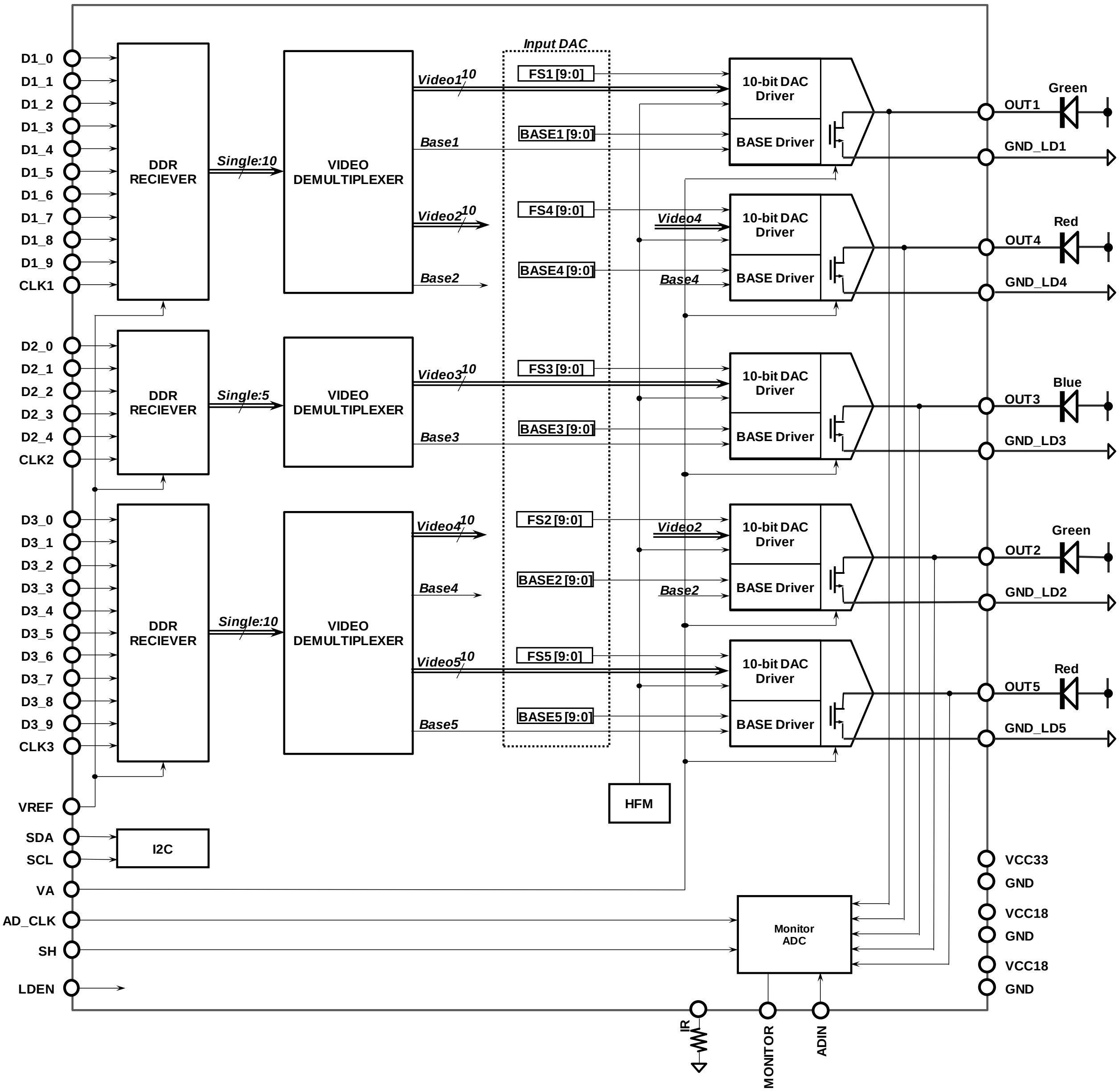
Absolute Maximum Ratings

Supply voltage	VCC18	2.5	V	
	VCC33	4.5	V	
Storage temperature	Tstg	-65 ～ +150	℃	
Junction temperature	Tjmax	150	℃	
OUT1 pin voltage	OUT1	< 8	V	(LD OFF)
OUT2 pin voltage	OUT2	< 8	V	(LD OFF)
OUT3 pin voltage	OUT3	< 8	V	(LD OFF)
OUT4 pin voltage	OUT4	< 8	V	(LD OFF)
OUT5 pin voltage	OUT5	< 8	V	(LD OFF)

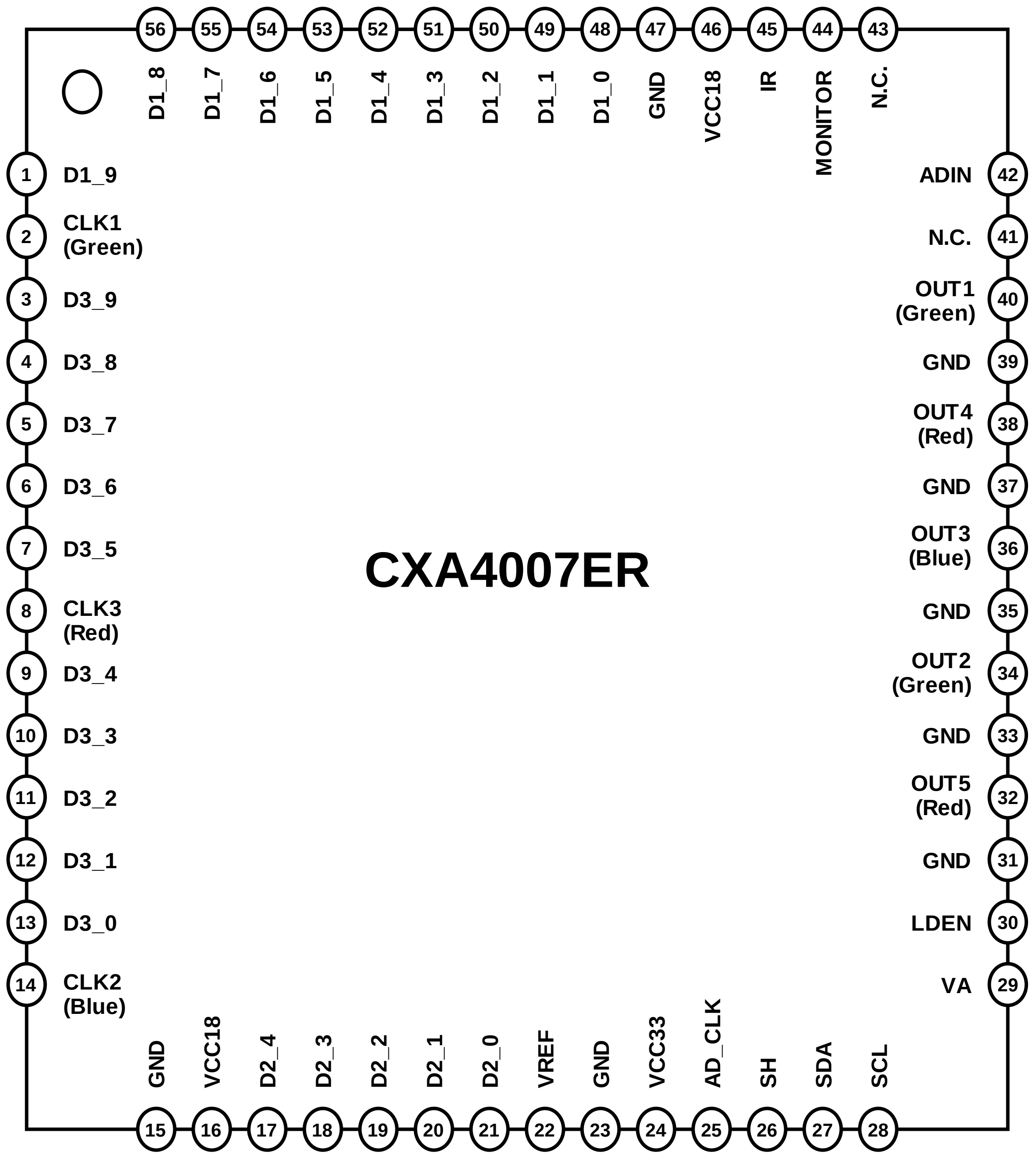
Recommended Operating Conditions

Supply voltage	VCC18	1.62 ～ 1.98	V
	VCC33	3.0 ～ 3.6	V
Operating temperature	Topr	–10 ～ 85	℃
OUT1 pin voltage	OUT1	< 7.5	V
OUT2 pin voltage	OUT2	< 7.5	V
OUT3 pin voltage	OUT3	< 7.5	V
OUT4 pin voltage	OUT4	< 7.5	V
OUT5 pin voltage	OUT5	< 7.5	V

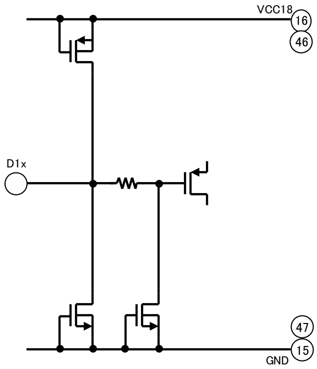
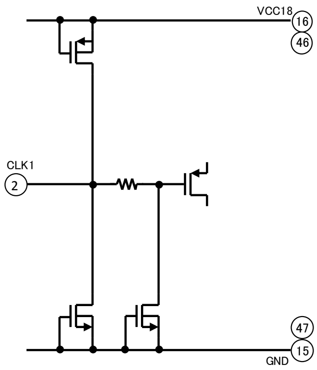
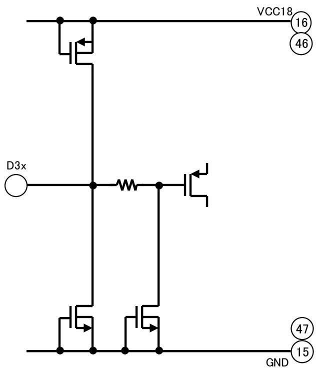
Block Diagram

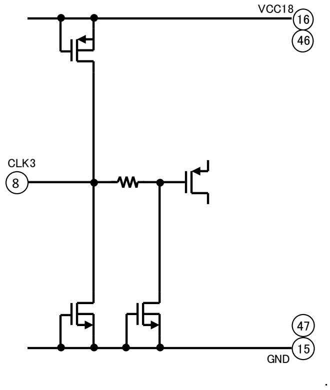
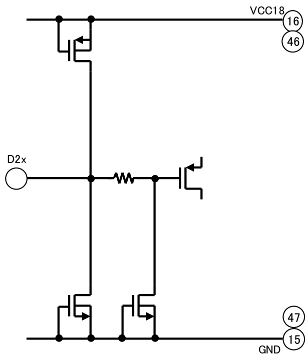
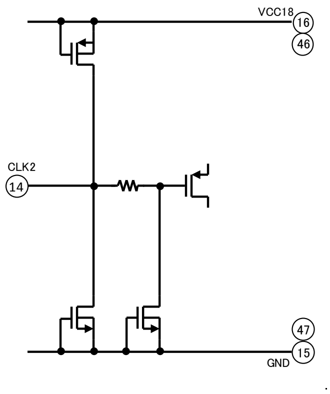
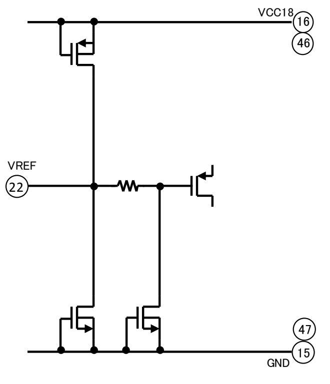


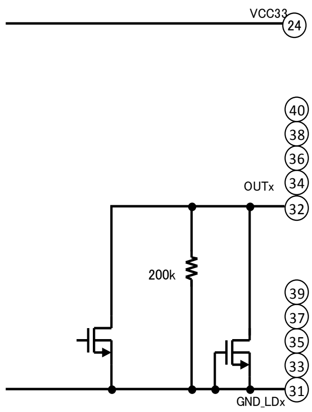
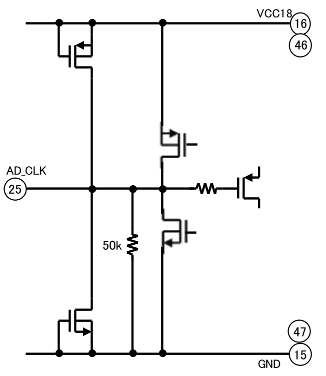
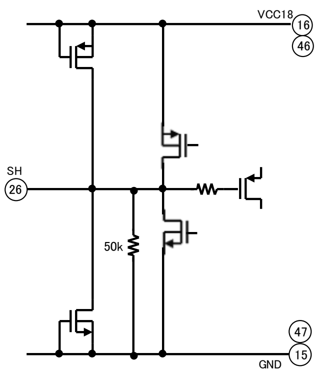
Pin Configuration

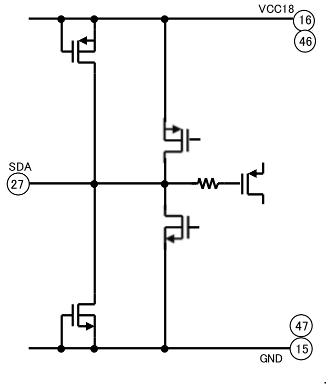
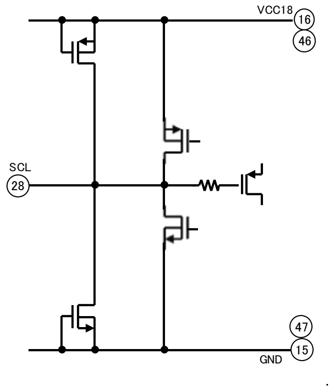
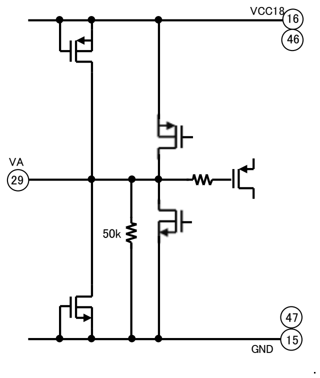
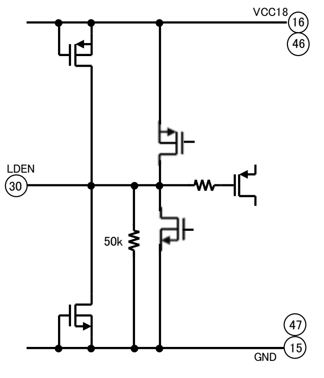


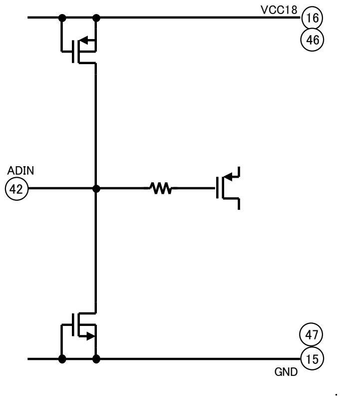
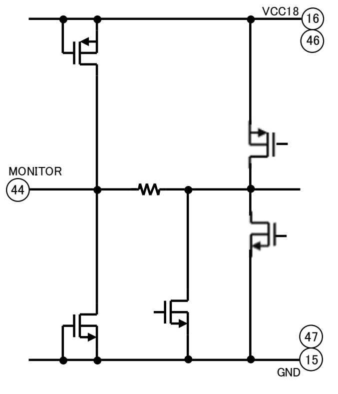
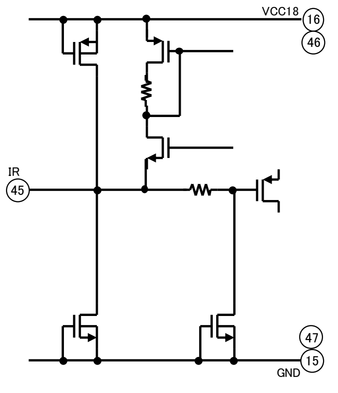
Pin Description

Pin No.	Symbol	I/O	Pin type	Equivalent circuit	Description
48	D1_0	I	Analog		Video Data input for OUT1 and OUT2 D1_0 is LSB、D1_9 is MSB CLK1 pos edge：Video data for OUT1 CLK1 neg edge：Video data for OUT2
49	D1_1				
50	D1_2				
51	D1_3				
52	D1_4				
53	D1_5				
54	D1_6				
55	D1_7				
56	D1_8				
1	D1_9				
2	CLK1	I	Analog		Video CLK input for D1[9:0]
3	D3_9	I	Analog		Video Data input for OUT4 and OUT5 D3_0 is LSB、D3_9 is MSB CLK3 pos edge：Video data for OUT4 CLK3 neg edge：Video data for OUT5
4	D3_8				
5	D3_7				
6	D3_6				
7	D3_5				
9	D3_4				
10	D3_3				
11	D3_2				
12	D3_1				
13	D3_0				

Pin No.	Symbol	I/O	Pin type	Equivalent circuit	Description
8	CLK3	I	Analog		Video CLK input for D3[9:0]
17	D2_4	I	Analog		Video Data input for OUT3 D2_0 is LSB、D2_4 is MSB CLK2 pos edge：D2[4:0] CLK2 neg edge：D2[9:5]
18	D2_3				
19	D2_2				
20	D2_1				
21	D2_0				
14	CLK2	I	Analog		Video CLK input for D2[9:0]
22	VREF	I	Analog		Reference voltage input for comparator

Pin No.	Symbol	I/O	Pin type	Equivalent circuit	Description
16	VCC18	-	Power		Power supply 1.8V
46					
24	VCC33	-	Power		Power supply 3.3V
15	GND	-	Ground		GND
23					
47					
39	GND_LD1	-	Ground		GND for OUT1 driver
37	GND_LD2				GND for OUT2 driver
35	GND_LD3				GND for OUT3 driver
33	GND_LD4				GND for OUT4 driver
31	GND_LD5				GND for OUT5 driver
40	OUT1	O	Analog		Current output1 for Laser diode
38	OUT2				Current output2 for Laser diode
36	OUT3				Current output3 for Laser diode
34	OUT4				Current output4 for Laser diode
32	OUT5				Current output5 for Laser diode
25	AD_CLK	I	LVTTL 1.8V		Clock input for ADC
26	SH	I	LVTTL 1.8V		Sample hold pulse input for ADC

Pin No.	Symbol	I/O	Pin type	Equivalent circuit	Description
27	SDA	I/O	LVTTL 1.8V		Serial data line for I2C
28	SCL	I	LVTTL 1.8V		Serial clock line for I2C
29	VA	I	LVTTL 1.8V		Video Area enable signal input High：Video Area output enable Low：Video Area output disable
30	LDEN	I	LVTTL 1.8V		LD enable signal input High：LD enable Low：LD disable

Pin No.	Symbol	I/O	Pin type	Equivalent circuit	Description
42	ADIN	I	Analog		ADC analog input
44	MONITOR	O	Analog		Monitor output
45	IR	-	Analog		Pin for reference current setting （connect to GND through 22KΩ）
41	N.C.	-	-		
43					

Electrical Characteristics

(VCC18 = 1.8V, VCC33 = 3.3V, Ta = 25℃)

No	Item	Symb	Conditions	Min.	Typ.	Max.	Unit
	Supply current 1 (Power save)	mA	OUT1-5_EN = 0d	0.01	0.1	0.2	mA
	Supply current 2 (Stanby)	mA	OUT1-5_EN = 1d LDEN = High, VA = Low VA1-5[1:0] = 1d	9	15	22	mA
	Supply current 3	mA	OUT1-5_EN = 1d VA1-5[1:0] = 1d LDEN = High, VA = High OUT1 = 90 mA (DACHFM-OFF, DC current) OUT2 = 90 mA (DACHFM-OFF, DC current) OUT3 = 40 mA (DACHFM-OFF, DC current) OUT4 = 120 mA (DACHFM-ON, Peak current) OUT5 = 120 mA (DACHFM-ON, Peak current)	30	42.6	55	mA

CMOS Logic Input Specifications

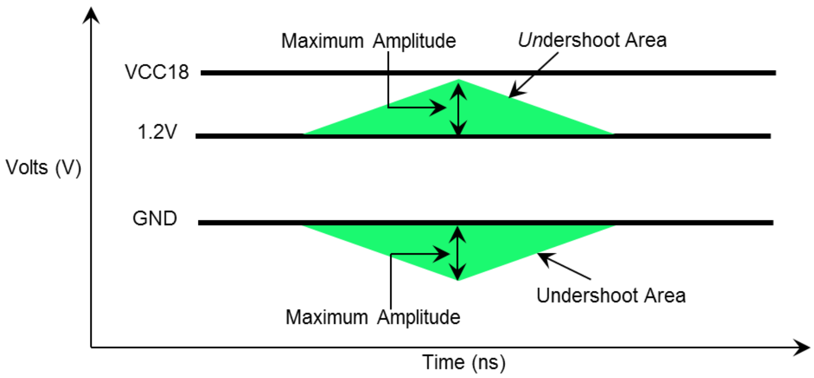
No	Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
	Input voltage High level	VSH	LDEN, VA, AD_CLK, SH, SDA, SCL	Vcc18 *0.7	-	Vcc18	V
	Input voltage Low level	VSL		0	-	Vcc18 *0.3	V
	Input current High level1	ISH1	LDEN, VA, AD_CLK, SH (VSH = 1.8 V)	20	39	60	uA
	Input current High level2	ISH2	SDA, SCL(VSH = 1.8 V)	-10	0	10	uA
	Input current Low level	ISL	LDEN, VA, AD_CLK, SH, SDA, SCL (VSH = 0 V)	-10	0	10	uA

CMOS Logic Output Specifications

No	Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
	Output voltage Low level	VOSL	SDA (IOL = 2 mA)	0	-	0.2	V

VIDEO DATA input specifications

No	Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
	Operating frequency	FCLK		-	-	200	MHz
	Clock Duty Cycle	CYCLE		45	-	55	%
	Setup time	TDS		0.64	-	-	ns
	Hold time	TDH		0.64	-	-	ns
	Input rise / fall time	TRTF	10% - 90%	-	1.5	-	ns
	Input voltage range	VINR		0	-	1.2	V
	Maximum peak amplitude allowed for Overshoot area	OVSA	VINR = 0-1.2V	-	0.42	-	V
	Maximum peak amplitude allowed for Undershoot area	UNSA	VINR = 0-1.2V	-	0.4	-	V
	Maximum Undershoot area below GND	UNSAREA		-	0.2	-	V-ns
	VREF input voltage range	VREF		0.54	-	0.66	V
	VREF input current	IREF	Vref = 0.6V	-10	0	10	uA
	DATA input capacitance	CDIN		-	1	-	pF



LD Driver DC Characteristics (OUTx)

No	Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
	VDAC - DNL	DNL	VIDEO full scale = 200 mA OUTx = 1.5 V	-3	-	3	LSB
	VDAC - INL	INL	VIDEO full scale = 200 mA OUTx = 1.5 V	-9	-	3	LSB

BASE DAC DC Characteristics

No	Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
	BASE DAC (Red / Green) maximum driving current	IMAX_BDAC_RG	BASEx[9:0] = 1023d BASEx_MODE=0d, OUTx = 1.5 V	75	100	-	mA
	BASE DAC (Blue) maximum driving current	IMAX_BDAC_B	BASE3[9:0] = 1023d BASE3_MODE=0d, OUT3 = 1.5 V	38	50	-	mA
	BASE DAC minimum driving current	IMIN_BDAC	BASEx[9:0] = 0d BASEx_MODE=0d, OUTx = 1.5 V	-	-	1	mA

VIDEO Full Scale DAC DC Characteristics

No	Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
	FS DAC (Red) maximum driving current	IMAX_FSDAC_R	FSx[9:0] = 1023d, VDACx[9:0] = FSx_MODE=0d, FSx_GAIN=3d OUTx = 1.5 V	500	550	-	mA
	FS DAC (Blue) maximum driving current	IMAX_FSDAC_B	FS3[9:0] = 1023d, VDAC3[9:0] = FS3_MODE=0d, FS3_GAIN=3d OUT3 = 1.5 V	200	240		mA
	FS DAC (Green) maximum driving current	IMAX_FSDAC_G	FSx[9:0] = 1023d, VDACx[9:0] = FSx_MODE=0d, FSx_GAIN=3d OUTx = 1.5 V	300	360		mA
	FS DAC minimum driving current 1	IMIN_FSDAC	FSx[9:0] = 1023d, VDACx[9:0] = 0d FSx_MODE=0d, FSx_GAIN=3d OUTx = 1.5 V	-	-	1	mA
	FS DAC minimum driving current 2	IMIN_FSDAC2	FSx[9:0] = 0d, VDACx[9:0] = 1023d FSx_MODE=0d, FSx_GAIN=3d OUTx = 1.5 V	-	-	1	mA

LD Driver AV Characteristics (OUTx)

No	Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
	Rise time (OUTx)	Tr	50 mA～120 mA, Pulse settling 10%～90%, Load = 13 Ω SNBRx[1:0] = TBD d, SNBCx[2:0] = TBD VIDEO Data = 256d	-	1	-	ns
	Fall time（OUTx)	Tf		-	1	-	ns
	Propagation delay1	DELAY1	OUT1,4 output ON response time from the head of video data for pixel	-	3CLK +5.5	-	ns
	Propagation delay2	DELAY2	OUT2,3,5 output ON response time from the head of video data for pixel	-	2.5CLK +5.5	-	ns

I/O Characteristics **Red/Green**

No	Item	Symbol	Conditions	Min.	Typ	Max	Unit
	I/O gain BASE_1 (Red/Green)	GAIN_B_1RG	Gain from BASEx[9:0] setting[dec] to OUTx BASEx_MODE = 1d, BASEx_GAIN = 0d BASEx[9:0] = 240d～480d, OUTx = 2.5 V	10	13	16	uA/dec
	I/O gain BASE_2 (Red/Green)	GAIN_B_2RG	Gain from BASEx[9:0] setting[dec] to OUTx BASEx_MODE = 1d, BASEx_GAIN = 1d BASEx[9:0] = 240d～480d, OUTx = 2.5 V	20	26	32	uA/dec
	I/O gain BASE_3 (Red/Green)	GAIN_B_3RG	Gain from BASEx[9:0] setting[dec] to OUTx BASEx_MODE = 1d, BASEx_GAIN = 2d BASEx[9:0] = 240d～480d, OUTx = 2.5 V	31	39	47	uA/dec
	I/O gain BASE_4 (Red/Green)	GAIN_B_4RG	Gain from BASEx[9:0] setting[dec] to OUTx BASEx_MODE = 1d, BASEx_GAIN = 3d BASEx[9:0] = 240d～480d, OUTx = 2.5 V	41	52	63	uA/dec
	I/O gain BASE_5 (Red/Green)	GAIN_B_5RG	Gain from BASEx[9:0] setting[dec] to OUTx BASEx_MODE = 0d, BASEx_GAIN = 0d BASEx[9:0] = 240d～480d, OUTx = 2.5 V	56	70	84	uA/dec
	I/O gain BASE_6 (Red/Green)	GAIN_B_6RG	Gain from BASEx[9:0] setting[dec] to OUTx BASEx_MODE = 0d, BASEx_GAIN = 1d BASEx[9:0] = 240d～480d, OUTx = 2.5 V	65	82	99	uA/dec
	I/O gain BASE_7 (Red/Green)	GAIN_B_7RG	Gain from BASEx[9:0] setting[dec] to OUTx BASEx_MODE = 0d, BASEx_GAIN = 2d BASEx[9:0] = 240d～480d, OUTx = 2.5 V	76	95	114	uA/dec
	I/O gain BASE_8 (Red/Green)	GAIN_B_8RG	Gain from BASEx[9:0] setting[dec] to OUTx BASEx_MODE = 0d, BASEx_GAIN = 3d BASEx[9:0] = 240d～480d, OUTx = 2.5 V	86	108	130	uA/dec

I/O Characteristics **Blue**

No	Item	Symbol	Conditions	Min.	Typ	Max	Unit
	I/O gain BASE_1 (Blue)	GAIN_B_1B	Gain from BASEx[9:0] setting[dec] to OUTx BASEx_MODE = 1d, BASEx_GAIN = 0d BASEx[9:0] = 240d～480d, OUTx = 2.5 V	5.5	7	8.5	uA/dec
	I/O gain BASE_2 (Blue)	GAIN_B_2B	Gain from BASEx[9:0] setting[dec] to OUTx BASEx_MODE = 1d, BASEx_GAIN = 1d BASEx[9:0] = 240d～480d, OUTx = 2.5 V	10	13	16	uA/dec
	I/O gain BASE_3 (Blue)	GAIN_B_3B	Gain from BASEx[9:0] setting[dec] to OUTx BASEx_MODE = 1d, BASEx_GAIN = 2d BASEx[9:0] = 240d～480d, OUTx = 2.5 V	16	20	24	uA/dec
	I/O gain BASE_4 (Blue)	GAIN_B_4B	Gain from BASEx[9:0] setting[dec] to OUTx BASEx_MODE = 1d, BASEx_GAIN = 3d BASEx[9:0] = 240d～480d, OUTx = 2.5 V	20.5	26	31.5	uA/dec
	I/O gain BASE_5 (Blue)	GAIN_B_5B	Gain from BASEx[9:0] setting[dec] to OUTx BASEx_MODE = 0d, BASEx_GAIN = 0d BASEx[9:0] = 240d～480d, OUTx = 2.5 V	28	35	42	uA/dec
	I/O gain BASE_6 (Blue)	GAIN_B_6B	Gain from BASEx[9:0] setting[dec] to OUTx BASEx_MODE = 0d, BASEx_GAIN = 1d BASEx[9:0] = 240d～480d, OUTx = 2.5 V	32	41	50	uA/dec
	I/O gain BASE_7 (Blue)	GAIN_B_7B	Gain from BASEx[9:0] setting[dec] to OUTx BASEx_MODE = 0d, BASEx_GAIN = 2d BASEx[9:0] = 240d～480d, OUTx = 2.5 V	38	48	58	uA/dec
	I/O gain BASE_8 (Blue)	GAIN_B_8B	Gain from BASEx[9:0] setting[dec] to OUTx BASEx_MODE = 0d, BASEx_GAIN = 3d BASEx[9:0] = 240d～480d, OUTx = 2.5 V	43	54	65	uA/dec

I/O Characteristics **Red**

No	Item	Symbol	Conditions	Min.	Typ.	Max	Unit
	I/O gain FS_1 (Red)	GAIN_FS_1R	Gain from FSx[9:0] setting [dec] to OUTx FSx_MODE = 1d, FSx_GAIN = 0d VDAC[9:0] = 1023d, FSx[9:0] = 60d～120d BASE current = 50 mA, OUTx = 2.5 V	44	63	82	uA/dec
	I/O gain FS_2 (Red)	GAIN_FS_2R	Gain from FSx[9:0] setting [dec] to OUTx FSx_MODE = 1d, FSx_GAIN = 1d VDAC[9:0] = 1023d, FSx[9:0] = 60d～120d BASE current = 50 mA, OUTx = 2.5 V	89	127	165	uA/dec
	I/O gain FS_3 (Red)	GAIN_FS_3R	Gain from FSx[9:0] setting [dec] to OUTx FSx_MODE = 1d, FSx_GAIN = 2d VDAC[9:0] = 1023d, FSx[9:0] = 60d～120d BASE current = 50 mA, OUTx = 2.5 V	134	192	250	uA/dec
	I/O gain FS_4 (Red)	GAIN_FS_4R	Gain from FSx[9:0] setting [dec] to OUTx FSx_MODE = 1d, FSx_GAIN = 3d VDAC[9:0] = 1023d, FSx[9:0] = 60d～120d BASE current = 50 mA, OUTx = 2.5 V	180	258	336	uA/dec
	I/O gain FS_5 (Red)	GAIN_FS_5R	Gain from FSx[9:0] setting [dec] to OUTx FSx_MODE = 0d, FSx_GAIN = 0d VDAC[9:0] = 1023d, FSx[9:0] = 60d～120d BASE current = 50 mA, OUTx = 2.5 V	276	345	432	uA/dec
	I/O gain FS_6 (Red)	GAIN_FS_6R	Gain from FSx[9:0] setting [dec] to OUTx FSx_MODE = 0d, FSx_GAIN = 1d VDAC[9:0] = 1023d, FSx[9:0] = 60d～120d BASE current = 50 mA, OUTx = 2.5 V	328	411	514	uA/dec
	I/O gain FS_7 (Red)	GAIN_FS_7R	Gain from FSx[9:0] setting [dec] to OUTx FSx_MODE = 0d, FSx_GAIN = 2d VDAC[9:0] = 1023d, FSx[9:0] = 60d～120d BASE current = 50 mA, OUTx = 2.5 V	381	477	597	uA/dec
	I/O gain FS_8 (Red)	GAIN_FS_8R	Gain from FSx[9:0] setting [dec] to OUTx FSx_MODE = 0d, FSx_GAIN = 3d VDAC[9:0] = 1023d, FSx[9:0] = 60d～120d BASE current = 50 mA, OUTx = 2.5 V	435	544	680	uA/dec

I/O Characteristics **Blue**

No	Item	Symbol	Conditions	Min.	Typ.	Max	Unit
	I/O gain FS_1 (Blue)	GAIN_FS_1B	Gain from FS3[9:0] setting [dec] to OUT3 FS3_MODE = 1d, FS3_GAIN = 0d VDAC[9:0] = 1023d, FS3[9:0] = 60d～120d BASE current = 50 mA, OUT3 = 2.5 V	19	28	37	uA/dec
	I/O gain FS_2 (Blue)	GAIN_FS_2B	Gain from FS3[9:0] setting [dec] to OUT3 FS3_MODE = 1d, FS3_GAIN = 1d VDAC[9:0] = 1023d, FS3[9:0] = 60d～120d BASE current = 50 mA, OUT3 = 2.5 V	38	55	72	uA/dec
	I/O gain FS_3 (Blue)	GAIN_FS_3B	Gain from FS3[9:0] setting [dec] to OUT3 FS3_MODE = 1d, FS3_GAIN = 2d VDAC[9:0] = 1023d, FS3[9:0] = 60d～120d BASE current = 50 mA, OUT3 = 2.5 V	59	84	109	uA/dec
	I/O gain FS_4 (Blue)	GAIN_FS_4B	Gain from FS3[9:0] setting [dec] to OUT3 FS3_MODE = 1d, FS3_GAIN = 3d VDAC[9:0] = 1023d, FS3[9:0] = 60d～120d BASE current = 50 mA, OUT3 = 2.5 V	78	112	146	uA/dec
	I/O gain FS_5 (Blue)	GAIN_FS_5B	Gain from FS3[9:0] setting [dec] to OUT3 FS3_MODE = 0d, FS3_GAIN = 0d VDAC[9:0] = 1023d, FS3[9:0] = 60d～120d BASE current = 50 mA, OUT3 = 2.5 V	120	150	188	uA/dec
	I/O gain FS_6 (Blue)	GAIN_FS_6B	Gain from FS3[9:0] setting [dec] to OUT3 FS3_MODE = 0d, FS3_GAIN = 1d VDAC[9:0] = 1023d, FS3[9:0] = 60d～120d BASE current = 50 mA, OUT3 = 2.5 V	143	179	224	uA/dec
	I/O gain FS_7 (Blue)	GAIN_FS_7B	Gain from FS3[9:0] setting [dec] to OUT3 FS3_MODE = 0d, FS3_GAIN = 2d VDAC[9:0] = 1023d, FS3[9:0] = 60d～120d BASE current = 50 mA, OUT3 = 2.5 V	166	208	260	uA/dec
	I/O gain FS_8 (Blue)	GAIN_FS_8B	Gain from FS3[9:0] setting [dec] to OUT3 FS3_MODE = 0d, FS3_GAIN = 3d VDAC[9:0] = 1023d, FS3[9:0] = 60d～120d BASE current = 50 mA, OUT3 = 2.5 V	189	237	297	uA/dec

I/O Characteristics **Green**

No	Item	Symbol	Conditions	Min.	Typ.	Max	Unit
	I/O gain FS_1 (Green)	GAIN_FS_1G	Gain from FSx[9:0] setting [dec] to OUTx FSx_MODE = 1d, FSx_GAIN = 0d VDAC[9:0] = 1023d, FSx[9:0] = 60d～120d BASE current = 50 mA, OUTx = 2.5 V	28	41	54	uA/dec
	I/O gain FS_2 (Green)	GAIN_FS_2G	Gain from FSx[9:0] setting [dec] to OUTx FSx_MODE = 1d, FSx_GAIN = 1d VDAC[9:0] = 1023d, FSx[9:0] = 60d～120d BASE current = 50 mA, OUTx = 2.5 V	58	83	108	uA/dec
	I/O gain FS_3 (Green)	GAIN_FS_3G	Gain from FSx[9:0] setting [dec] to OUTx FSx_MODE = 1d, FSx_GAIN = 2d VDAC[9:0] = 1023d, FSx[9:0] = 60d～120d BASE current = 50 mA, OUTx = 2.5 V	87	125	163	uA/dec
	I/O gain FS_4 (Green)	GAIN_FS_4G	Gain from FSx[9:0] setting [dec] to OUTx FSx_MODE = 1d, FSx_GAIN = 3d VDAC[9:0] = 1023d, FSx[9:0] = 60d～120d BASE current = 50 mA, OUTx = 2.5 V	117	168	219	uA/dec
	I/O gain FS_5 (Green)	GAIN_FS_5G	Gain from FSx[9:0] setting [dec] to OUTx FSx_MODE = 0d, FSx_GAIN = 0d VDAC[9:0] = 1023d, FSx[9:0] = 60d～120d BASE current = 50 mA, OUTx = 2.5 V	180	225	282	uA/dec
	I/O gain FS_6 (Green)	GAIN_FS_6G	Gain from FSx[9:0] setting [dec] to OUTx FSx_MODE = 0d, FSx_GAIN = 1d VDAC[9:0] = 1023d, FSx[9:0] = 60d～120d BASE current = 50 mA, OUTx = 2.5 V	214	268	335	uA/dec
	I/O gain FS_7 (Green)	GAIN_FS_7G	Gain from FSx[9:0] setting [dec] to OUTx FSx_MODE = 0d, FSx_GAIN = 2d VDAC[9:0] = 1023d, FSx[9:0] = 60d～120d BASE current = 50 mA, OUTx = 2.5 V	248	311	389	uA/dec
	I/O gain FS_8 (Green)	GAIN_FS_8G	Gain from FSx[9:0] setting [dec] to OUTx FSx_MODE = 0d, FSx_GAIN = 3d VDAC[9:0] = 1023d, FSx[9:0] = 60d～120d BASE current = 50 mA, OUTx = 2.5 V	284	355	444	uA/dec

High-frequency Modulation (HFM)

No	Item	Symbol	Conditions	Min.	Typ.	Max	Unit
	Frequency variable range	VARIF_L	HFMFx = 0d	-	-	100	MHz
	Frequency variable range	VARIF_H	HFMFx = 255d	500	-	-	MHz
	Frequency variability	FREQ	HFMFx = 34 d Frequency = 220 MHz	-25	-	25	%
	Frequency temperature coefficient	TFREQ	HFMFx = 34 d Frequency = 220 MHz	-	0.006	-	%/°C

LDON/OFF response

No	Item	Symbol	Conditions	Min.	Typ.	Max	Unit
	LDON response time 1	LDONRES1	Time for the output current to rise to 90% when LDEN is changed from Low to High	-	450	900	us
	LDON response time 2	LDONRES2	Time for the output current to rise to 90% when VA is changed from Low to High	-	5	30	ns
	LDOFF response time 1	LDOFFRES1	Time for the output current to fall to 10% when LDEN is changed from High to Low	-	3	10	ns
	LDOFF response time 2	LDOFFRES2	Time for the output current to fall to 10% when VA is changed from High to Low	-	5	30	ns

AD Characteristic

No	Item	Symbol	Conditions	Min.	Typ.	Max	Unit
	ADDAC - DNL	AD_DNL	ADIN = 0.4 V ～ 1.5 V	-	0	-	LSB
	ADDAC - INL	AD_INL	ADIN = 0.4 V ～ 1.5 V	-	-0.5	-	LSB
	Gain offset	AD_GAIN	Gain from OUTx to ADIN OUTx = 2 V ～ 7.5 V	-2.4	-	2.4	%
	DC offset	ADOFFSET	AD input voltage when ADIN = 1 V	-20	-	20	mV
	Input frequency range	ADCLK	ADCLK = 8.3125MHz	-5	-	5	%

Power Supply Monitor Characteristics

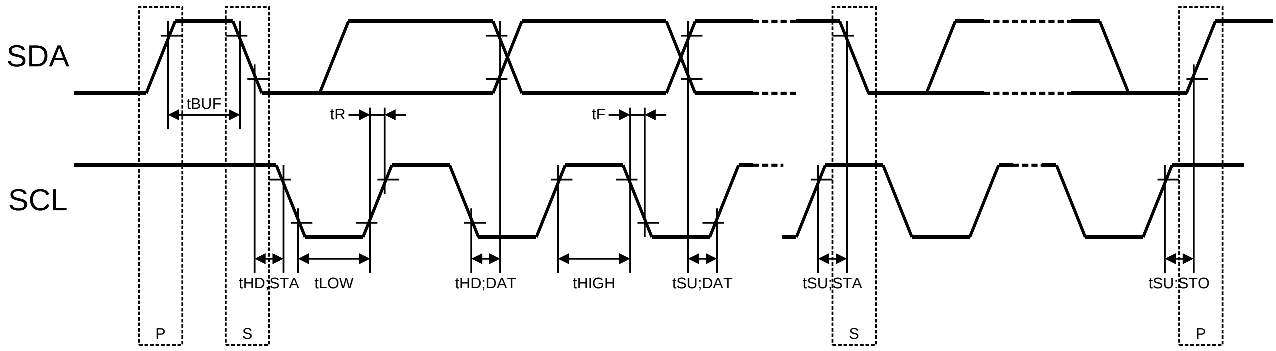
No	Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
	Power supply (3.3V) (LDOFF)	EM33OFF	VCC33 voltage at which LDOFF results	2.25	2.5	2.75	V
	Power supply (3.3V) (LDON)	EM33ON	VCC33 voltage at which LDOFF is canceled	2.4	2.65	2.9	V
	Power supply (1.8V) (LDOFF)	EM18OFF	VCC18 voltage at which LDOFF results	1.2	1.3	1.4	V
	Power supply (1.8V) (LDON)	EM18ON	VCC18 voltage at which LDOFF is canceled	1.3	1.4	1.5	V
	Register reset voltage	REGRESET	The voltage of VCC18 by which registers are reset	-	1.0	1.1	V

Monitor Characteristics

No	Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
	VOP monitor (5 V)	VmoDC_H	MONITOR voltage when 5 V is to OUTx	0.95	1	1.05	V
	VOP monitor (2 V)	VmoDC_M	MONITOR voltage when 2 V is to OUTx	0.35	0.4	0.45	V
	VOP monitor lower limit	VmoMin	MONITOR voltage when 0 V is to OUTx	0	-	0.1	V
	Temperature monitor output voltage	TmoVout	Tj = 70 ℃	-	0.79	-	V
	Temperature monitor temperature coefficient	TmoTemp		-	2.23	-	mV/℃

I2C Timing

No	Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
	Clock frequency	fSCL		-	-	400	kHz
	Data charge	tBUF		1.3	-	-	us
	Data transfer	tHD.STA		0.6	-	-	us
	Low level clock pulse width	tLOW		1.3	-	-	us
	High level clock pulse width	tHIGH		0.6	-	-	us
	Start setup waiting time	tSU,STA		0.6	-	-	us
	Data hold time	tHD.DAT		0	-	-	us
	Data setup time	tSU.DAT		100	-	-	ns
	Rise time	tR		-	-	300	ns
	Fall time	tF		-	-	300	ns
	Stop setup wating time	tSU.STO		0.6	-	-	us



I2C mode

The CXA4007ER performs IC control via the I2C interface. The I2C interface specifications are shown below.

Slave Address is 1001_110x. x = 1 read, x = 0 write access.

◆Write Cycle1

S	Slave Address	W	A	Start Sub Address	A	Write Data 1	A	P

◆Read Cycle1

S	Slave Address	W	A	Start Sub Address	A	Sr	Slave Address	R	A	Read Data 1	A	Read Data 2	A	Read Data 3	A	P

S = Start Condition P = Stop Condition A = Acknowlege W = Write Register (0) R = Read Register (1)

(shaded box) = from Master to Slave (white box) = from Slave to Master

Address Map

After Power-ON reset, all registers excluding are set to “0”.

In Address Map, even blank fields “-“ have physical register. Please set “0” to these bits.

In undefined addresses, there are no physical registers.

	Register							
Adr.	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x00	RST_DIS	–	–	OUT5_EN	OUT4_EN	OUT3_EN	OUT2_EN	OUT1_EN
0x01	RST							
0x02	VA4 [1:0]		VA3 [1:0]		VA2 [1:0]		VA1 [1:0]	
0x03	–		VA_PSMODE [1:0]		VA_DIRECT	VA_REG	VA5 [1:0]	
0x04	SH_REG	SH_CONT			EMVCC_MON	EMVCC_TRG	–	EMVCC_EN
0x05	VERREG [3:0]				–			EMVCC_RB
0x06	–	MON_OUTSEL [2:0]			VIMON [3:0]			
0x07	ADSEL [2:0]			FS5_MODE	FS4_MODE	FS3_MODE	FS2_MODE	FS1_MODE
0x08	ADEN	–		BASE5_MODE	BASE4_MODE	BASE3_MODE	BASE2_MODE	BASE1_MODE
0x09	FS1_LPF [1:0]		BASE1_LPF [1:0]		FS1_GAIN [1:0]		BASE1_GAIN [1:0]	
0x0A	FS2_LPF [1:0]		BASE2_LPF [1:0]		FS2_GAIN [1:0]		BASE2_GAIN [1:0]	
0x0B	FS3_LPF [1:0]		BASE3_LPF [1:0]		FS3_GAIN [1:0]		BASE3_GAIN [1:0]	
0x0C	FS4_LPF [1:0]		BASE4_LPF [1:0]		FS4_GAIN [1:0]		BASE4_GAIN [1:0]	
0x0D	FS5_LPF [1:0]		BASE5_LPF [1:0]		FS5_GAIN [1:0]		BASE5_GAIN [1:0]	
0x0E	FS5 [9:8]		FS3 [9:8]		FS2 [9:8]		FS1 [9:8]	
0x0F	–						FS5 [9:8]	
0x10	FS1 [7:0]							
0x11	FS2 [7:0]							
0x12	FS3 [7:0]							
0x13	FS4 [7:0]							
0x14	FS5 [7:0]							
0x15	BASE4 [9:8]		BASE3 [9:8]		BASE2 [9:8]		BASE1 [9:8]	
0x16	–						BASE5 [9:8]	
0x17	BASE1 [7:0]							
0x18	BASE2 [7:0]							
0x19	BASE3 [7:0]							
0x1A	BASE4 [7:0]							
0x1B	BASE5 [7:0]							
0x1C	–		SNBR1 [1:0]		–	SNBC1 [2:0]		
0x1D	–		SNBR2 [1:0]		–	SNBC2 [2:0]		
0x1E	–		SNBR3 [1:0]		–	SNBC3 [2:0]		
0x1F	–		SNBR4 [1:0]		–	SNBC4 [2:0]		
0x20	–		SNBR5 [1:0]		–	SNBC5 [2:0]		
0x21	–			HFM5_EN	HFM4_EN	HFM3_EN	HFM2_EN	HFM1_EN
0x22	HFMCNT_EN	–		HFMCNT_INT	–		OSC_SEL [1:0]	
0x23	HFMCNT_RB[7:0]							
0x24	HFMF1 [7:0]							
0x25	HFMF2 [7:0]							
0x26	–			EMIS3_1	EMIS1 [1:0]		EMIP1 [1:0]	
0x27	–			EMIS3_2	EMIS2 [1:0]		EMIP2 [1:0]	
0x28	–			–	HFM_SYNC_PW [1:0]		HFM_SYNC_LV	HFM_SYNC
0x29	HFM2_DUTY_MODE	HFM2_DUTY_POL	HFM2_DUTY [1:0]		HFM1_DUTY_MODE	HFM1_DUTY_POL	HFM1_DUTY [1:0]	
0x2A	AD_ALM	–			AD2_RB [9:8]		AD1_RB [9:8]	
0x2B	AD1_RB [7:0]							
0x2C	AD2_RB [7:0]							
0x2D	–							
0x2E	–							
0x2F	VDAC_MODE	–	VDAC45 [9:8]		VDAC3 [9:8]		VDAC12 [9:8]	
0x30	VDAC12 [7:0]							
0x31	VDAC3 [7:0]							
0x32	VDAC45 [7:0]							
0x33	WCL1_MODE	WCL1<6:0>						
0x34	WCL2_MODE	WCL2<6:0>						
0x35	WCL3_MODE	WCL3<6:0>						
0x36	WCL4_MODE	WCL4<6:0>						
0x37	WCL5_MODE	WCL5<6:0>						

Operation of FSx[9:0] and BASEx[9:0]

When setting lower 8 bits [7:0], all 10 bits [9:8] and [7:0] are reflected simultaneously to internal circuit.

Description of Register

Address 0x00

Bit	Name	Bit definition
7	RST_DIS	Global reset (RST) control selection by serial interface. 0: Enable 1: Disable
6-5	–	Not used. Please set this bit "0".
4	OUT5_EN	OUT5 output selection 0: Disable 1: Enable
3	OUT4_EN	OUT4 output selection 0: Disable 1: Enable
2	OUT3_EN	OUT3 output selection 0: Disable 1: Enable
1	OUT2_EN	OUT2 output selection 0: Disable 1: Enable
0	OUT1_EN	OUT1 output selection 0: Disable 1: Enable

Address 0x01

Bit	Name	Bit definition
7-0	RST	All registers are reset when this address is accessed by serial interface in write

Address 0x02

Bit	Name	Bit definition
7-6	VA4[1:0]	OUT4 output control when VA pin = "H" 00: Disable 01: VDAC Driver 10: VDAC Driver + BASE Driver 11: VDAC Driver + BASE Driver video data ≠ 0: Base driver outputs current in synchronization with video video data = 0: Base driver stops current in synchronization with video data.
5-4	VA3[1:0]	OUT3 output control when VA pin = "H" 00: Disable 01: VDAC Driver 10: VDAC Driver + BASE Driver 11: VDAC Driver + BASE Driver video data ≠ 0: Base driver outputs current in synchronization with video video data = 0: Base driver stops current in synchronization with video data.
3-2	VA2[1:0]	OUT2 output control when VA pin = "H" 00: Disable 01: VDAC Driver 10: VDAC Driver + BASE Driver 11: VDAC Driver + BASE Driver video data ≠ 0: Base driver outputs current in synchronization with video video data = 0: Base driver stops current in synchronization with video data.
1-0	VA1[1:0]	OUT1 output control when VA pin = "H" 00: Disable 01: VDAC Driver 10: VDAC Driver + BASE Driver 11: VDAC Driver + BASE Driver video data ≠ 0: Base driver outputs current in synchronization with video video data = 0: Base driver stops current in synchronization with video data.

Address 0x03

Bit	Name	Bit definition
7-6	—	Not used. Please set this bit "0".
5-4	VA_PSMODE	Circuit of power save mode selection by VA pin 00: Normal 01: Horizontal & Vertical Blanking 10: Vertical Blanking 11: Not used
4	VA_DIRECT	Output current control mode selection 2 by VA pin (VA_REG=1 at usefully) 0: Polarity of VA pin is reflected to output current in synchronization with video data input. 1: Polarity of VA pin is reflected to output current immediately.
3	VA_REG	Output current control mode selection 1 by VA pin 0: normal mode 1: The mode fixing that the polarity of VA pin is reflected to output current immediately.
1-0	VA5[1:0]	OUT5 output control when VA pin = "H" 00: Disable 01: VDAC Driver 10: VDAC Driver + BASE Driver 11: VDAC Driver + BASE Driver video data $\neq$ 0: Base driver outputs current in synchronization with video data. video data $=$ 0: Base driver stops current in synchronization with video data.

Address 0x04

Bit	Name	Bit definition
7	SH_REG	SH level control (SH_CONT=1 at usefully) 0: SH Low level 1: SH High level
6	SH_CONT	SH control mode selection 0: Pin control mode 1: Register control mode
5-4	—	Not used. Please set this bit "0".
3	EMVCC_MON	Monitor output of Vcc18 / Vcc33 supply voltage error detection result from MONITOR pin 0: Disable 1: Enable
2	EMVCC_TRG	Vcc18 / Vcc33 supply voltage error detection mode selection 0: Latch result 1: Follow real-time result
1	—	Not used. Please set this bit "0".
0	EMVCC_EN	LDOFF function when Vcc18 / Vcc33 supply voltage error is detected 0: Disable 1: Enable

Address 0x05

Bit	Name	Bit definition
7-4	VERREG[3:0]	IC version register (Read Only) 0100: CXA4007ER 0011: S6137 TS1 0010: S6137 TS2
3-1	—	Not used. Please set this bit "0".
0	EMVCC_RB	Vcc18, Vcc33 supply voltage error detection result (Read Only) 0: Normal operation 1: Supply voltage error is detected If an error is detected, error is latched to this register. An error detection result is cleared by a dummy write to this address.

Address 0x06

Bit	Name	Bit definition
7	—	Not used. Please set this bit "0".
6-4	MON_OUTSEL[2:0]	Monitoring circuit selection when marked (*) signals are selected in VIMON[3:0]. When VIMON[3:0] = 0000, MON_OUTSEL[2:0] selects HFM frequency count circuit. 000: OUT1 001: OUT2 010: OUT3 011: OUT4 100: OUT5 101: Not used 110: Not used 111: Not used
3-0	VIMON [3:0]	Monitoring signal selection. Marked (*) signals come from each output path. Please select a path in MON_OUTSEL[2:0]. 0000: OFF 0001: VOP monitor (*) 0010: Temperature sensor monitor 0011 – 1111: Not used.

Address 0x07

Bit	Name	Bit definition
7-5	ADSEL[2:0]	ADC mode selection when VOP monitor is selected by VIMON[3:0] 000: VHR for OUT1 is converted by ADC1, VHR for OUT2 is converted by ADC2 001: VHR for OUT3 is converted by ADC1 010: VHR for OUT4 is converted by ADC1, VHR for OUT5 is converted by ADC2 011: ADIN is converted by ADC1 1xx: Not used
4	FS5_MODE	OUT5 VDAC Driver Full-scale current mode selection 0: Normal mode 1: Low-GAIN mode
3	FS4_MODE	OUT4 VDAC Driver Full-scale current mode selection 0: Normal mode 1: Low-GAIN mode
2	FS3_MODE	OUT3 VDAC Driver current mode selection 0: Normal mode 1: Low-GAIN mode
1	FS2_MODE	OUT2 VDAC Driver current mode selection 0: Normal mode 1: Low-GAIN mode
0	FS1_MODE	OUT1 VDAC Driver current mode selection 0: Normal mode 1: Low-GAIN mode

Address 0x08

Bit	Name	Bit definition
7	ADEN	ADC1/2 mode selection 0: Disable 1: Enable
6-5	－	Not used. Please set this bit "0".
4	BASE5_MODE	OUT5 BASE Driver current mode selection 0: Normal mode 1: Low-GAIN mode
3	BASE4_MODE	OUT4 BASE Driver current mode selection 0: Normal mode 1: Low-GAIN mode
2	BASE3_MODE	OUT3 BASE Driver current mode selection 0: Normal mode 1: Low-GAIN mode
1	BASE2_MODE	OUT2 BASE Driver current mode selection 0: Normal mode 1: Low-GAIN mode
0	BASE1_MODE	OUT1 BASE Driver current mode selection 0: Normal mode 1: Low-GAIN mode

Address 0x09

Bit	Name	Bit definition	
7-6	FS1_LPF[1:0]	FS1 Bandwidth selection 00: No limit 01: 100 kHz 10: 50 kHz 11: 25 kHz	
5-4	BASE1_LPF[1:0]	BASE1 Bandwidth selection 00: No limit 01: 80 kHz 10: 25 kHz 11: 10 kHz	
3-2	FS1_GAIN[1:0]	FS1 GAIN selection	
		(FS1_MODE = 0) 00: GAIN=64% 01: GAIN=76% 10: GAIN=88% 11: GAIN=100%	(FS1_MODE = 1) 00: GAIN=12 % 01: GAIN=24% 10: GAIN=36% 11: GAIN=48%
1-0	BASE1_GAIN[1:0]	BASE1 GAIN selection	
		(BASE1_MODE = 0) 00: GAIN=64% 01: GAIN=76% 10: GAIN=88% 11: GAIN=100%	(BASE1_MODE = 1) 00: GAIN=12 % 01: GAIN=24% 10: GAIN=36% 11: GAIN=48%

Address 0x0A

Bit	Name	Bit definition	
7-6	FS2_LPF[1:0]	FS2 Bandwidth selection 00: No limit 01: 100 kHz 10: 50 kHz 11: 25 kHz	
5-4	BASE2_LPF[1:0]	BASE2 Bandwidth selection 00: No limit 01: 80 kHz 10: 25 kHz 11: 10 kHz	
3-2	FS2_GAIN[1:0]	FS2 GAIN selection	
		(FS2_MODE = 0) 00: GAIN=64% 01: GAIN=76% 10: GAIN=88% 11: GAIN=100%	(FS2_MODE = 1) 00: GAIN=12 % 01: GAIN=24% 10: GAIN=36% 11: GAIN=48%
1-0	BASE2_GAIN[1:0]	BASE2 GAIN selection	
		(BASE2_MODE = 0) 00: GAIN=64% 01: GAIN=76% 10: GAIN=88% 11: GAIN=100%	(BASE2_MODE = 1) 00: GAIN=12 % 01: GAIN=24% 10: GAIN=36% 11: GAIN=48%

Address 0x0B

Bit	Name	Bit definition	
7-6	FS3_LPF[1:0]	FS3 Bandwidth selection 00: No limit 01: 100 kHz 10: 50 kHz 11: 25 kHz	
5-4	BASE3_LPF[1:0]	BASE3 Bandwidth selection 00: No limit 01: 80 kHz 10: 25 kHz 11: 10 kHz	
3-2	FS3_GAIN[1:0]	FS3 GAIN selection	
		(FS3_MODE = 0) 00: GAIN=64% 01: GAIN=76% 10: GAIN=88% 11: GAIN=100%	(FS3_MODE = 1) 00: GAIN=12 % 01: GAIN=24% 10: GAIN=36% 11: GAIN=48%
1-0	BASE3_GAIN[1:0]	BASE3 GAIN selection	
		(BASE3_MODE = 0) 00: GAIN=64% 01: GAIN=76% 10: GAIN=88% 11: GAIN=100%	(BASE3_MODE = 1) 00: GAIN=12 % 01: GAIN=24% 10: GAIN=36% 11: GAIN=48%

Address 0x0C

Bit	Name	Bit definition	
7-6	FS4_LPF[1:0]	FS4 Bandwidth selection 00: No limit 01: 100 kHz 10: 50 kHz 11: 25 kHz	
5-4	BASE4_LPF[1:0]	BASE4 Bandwidth selection 00: No limit 01: 80 kHz 10: 25 kHz 11: 10 kHz	
3-2	FS4_GAIN[1:0]	FS4 GAIN selection	
		(FS4 MODE = 0) 00: GAIN=64% 01: GAIN=76% 10: GAIN=88% 11: GAIN=100%	(FS4 MODE = 1) 00: GAIN=12 % 01: GAIN=24% 10: GAIN=36% 11: GAIN=48%
1-0	BASE4_GAIN[1:0]	BASE4 GAIN selection	
		(BASE4 MODE = 0) 00: GAIN=64% 01: GAIN=76% 10: GAIN=88% 11: GAIN=100%	(BASE4 MODE = 1) 00: GAIN=12 % 01: GAIN=24% 10: GAIN=36% 11: GAIN=48%

Address 0x0D

<table>
<tr><th>Bit</th><th>Name</th><th colspan="2">Bit definition</th></tr>
<tr><td>7-6</td><td>FS5_LPF[1:0]</td><td colspan="2">FS5 Bandwidth selection
00: No limit
01: 100 kHz
10: 50 kHz
11: 25 kHz</td></tr>
<tr><td>5-4</td><td>BASE5_LPF[1:0]</td><td colspan="2">BASE5 Bandwidth selection
00: No limit
01: 80 kHz
10: 25 kHz
11: 10 kHz</td></tr>
<tr><td rowspan="2">3-2</td><td rowspan="2">FS5_GAIN[1:0]</td><td colspan="2">FS5 GAIN selection</td></tr>
<tr><td>(FS5_MODE = 0)
00: GAIN=64%
01: GAIN=76%
10: GAIN=88%
11: GAIN=100%</td><td>(FS5_MODE = 1)
00: GAIN=12 %
01: GAIN=24%
10: GAIN=36%
11: GAIN=48%</td></tr>
<tr><td rowspan="2">1-0</td><td rowspan="2">BASE5_GAIN[1:0]</td><td colspan="2">BASE5 GAIN selection</td></tr>
<tr><td>(BASE5_MODE = 0)
00: GAIN=64%
01: GAIN=76%
10: GAIN=88%
11: GAIN=100%</td><td>(BASE5_MODE = 1)
00: GAIN=12 %
01: GAIN=24%
10: GAIN=36%
11: GAIN=48%</td></tr>
</table>

Address 0x0E, 0x10

Bit	Name	Bit definition
0x0E 1-0	FS1 [9:8]	VDAC Driver1 Full Scale current setting Resolution = [VDAC Driver1 maximum driving current] / 1023 0: 0 mA 1: [VDAC Driver1 maximum driving current] / 1023 to 3FF: [VDAC Driver1 maximum driving current]
0x10 7-0	FS1 [7:0]	

When setting FS1[7:0], FS1[9:8] and FS1[7:0] is reflected simultaneously to internal circuit.

Address 0x0E, 0x11

Bit	Name	Bit definition
0x0E 3-2	FS2 [9:8]	VDAC Driver2 Full Scale current setting Resolution = [VDAC Driver2 maximum driving current] / 1023 0: 0 mA 1: [VDAC Driver2 maximum driving current] / 1023 to 3FF: [VDAC Driver2 maximum driving current]
0x11 7-0	FS2 [7:0]	

When setting FS2[7:0], FS2[9:8] and FS2[7:0] is reflected simultaneously to internal circuit.

Address 0x0E, 0x12

Bit	Name	Bit definition
0x0E 5-4	FS3 [9:8]	VDAC Driver3 Full Scale current setting Resolution = [VDAC Driver3 maximum driving current] / 1023 0: 0 mA 1: [VDAC Driver3 maximum driving current] / 1023 to 3FF: [VDAC Driver3 maximum driving current]
0x12 7-0	FS3 [7:0]	

When setting FS3[7:0], FS3[9:8] and FS3[7:0] is reflected simultaneously to internal circuit.

Address 0x0E, 0x13

Bit	Name	Bit definition
0x0E 7-6	FS4 [9:8]	VDAC Driver4 Full Scale current setting Resolution = [VDAC Driver4 maximum driving current] / 1023 0: 0 mA 1: [VDAC Driver4 maximum driving current] / 1023 to 3FF: [VDAC Driver4 maximum driving current]
0x13 7-0	FS4 [7:0]	

When setting FS4[7:0], FS4[9:8] and FS4[7:0] is reflected simultaneously to internal circuit.

Address 0x0E, 0x14

Bit	Name	Bit definition
0x0F 1-0	FS5 [9:8]	VDAC Driver5 Full Scale current setting Resolution = [VDAC Driver5 maximum driving current] / 1023 0: 0 mA 1: [VDAC Driver5 maximum driving current] / 1023 to 3FF: [VDAC Driver5 maximum driving current]
0x14 7-0	FS5 [7:0]	

When setting FS5[7:0], FS5[9:8] and FS5[7:0] is reflected simultaneously to internal circuit.

Address 0x15, 0x17

Bit	Name	Bit definition
0x15 1-0	BASE1[9:8]	OUT1 BASE current setting Resolution = [BASE Driver1 maximum driving current] / 1023 0: 0 mA 1: [BASE Driver1 maximum driving current] / 1023 to 3FF: [BASE Driver1 maximum driving current]
0x17 7-0	BASE1[7:0]	

When setting BASE1[7:0], BASE1[9:8] and BASE1[7:0] is reflected simultaneously to internal circuit.

Address 0x15, 0x18

Bit	Name	Bit definition
0x15 3-2	BASE2[9:8]	OUT2 BASE current setting Resolution = [BASE Driver2 maximum driving current] / 1023 0: 0 mA 1: [BASE Driver2 maximum driving current] / 1023 to 3FF: [BASE Driver2 maximum driving current]
0x18 7-0	BASE2[7:0]	

When setting BASE2[7:0], BASE2[9:8] and BASE2[7:0] is reflected simultaneously to internal circuit.

Address 0x15, 0x19

Bit	Name	Bit definition
0x15 5-4	BASE3[9:8]	OUT3 BASE current setting Resolution = [BASE Driver3 maximum driving current] / 1023 0: 0 mA 1: [BASE Driver3 maximum driving current] / 1023 to 3FF: [BASE Driver3 maximum driving current]
0x19 7-0	BASE3[7:0]	

When setting BASE3[7:0], BASE3[9:8] and BASE3[7:0] is reflected simultaneously to internal circuit.

Address 0x15, 0x1A

Bit	Name	Bit definition
0x15 7-6	BASE4[9:8]	OUT4 BASE current setting Resolution = [BASE Driver4 maximum driving current] / 1023 0: 0 mA 1: [BASE Driver4 maximum driving current] / 1023 to 3FF: [BASE Driver4 maximum driving current]
0x19 7-0	BASE4[7:0]	

When setting BASE4[7:0], BASE4[9:8] and BASE4[7:0] is reflected simultaneously to internal circuit.

Address 0x16, 0x1B

Bit	Name	Bit definition
0x16 1-0	BASE5[9:8]	OUT5 BASE current setting Resolution = [BASE Driver5 maximum driving current] / 1023 0: 0 mA 1: [BASE Driver5 maximum driving current] / 1023 to 3FF: [BASE Driver5 maximum driving current]
0x1B 7-0	BASE5[7:0]	

When setting BASE5[7:0], BASE5[9:8] and BASE5[7:0] is reflected simultaneously to internal circuit.

Address 0x1C

Bit	Name	Bit definition
7-6	—	Not used. Please set this bit "0".
5-4	SNBR1 [1:0]	OUT1 Snubber resistor selection 00: Fast waveform 01: ↓ 10: ↓ 11: Slow waveform
3	—	Not used. Please set this bit "0".
2-0	SNBC1 [2:0]	OUT1 Snubber capacitor selection 000: Fast waveform 001: ↓ 010: ↓ 011: ↓ 100: ↓ 101: ↓ 110: ↓ 111: Slow waveform

Address 0x1D

Bit	Name	Bit definition
7-6	—	Not used. Please set this bit "0".
5-4	SNBR2 [1:0]	OUT2 Snubber resistor selection 00: Fast waveform 01: ↓ 10: ↓ 11: Slow waveform
3	—	Not used. Please set this bit "0".
2-0	SNBC2 [2:0]	OUT2 Snubber capacitor selection 000: Fast waveform 001: ↓ 010: ↓ 011: ↓ 100: ↓ 101: ↓ 110: ↓ 111: Slow waveform

Address 0x1E

Bit	Name	Bit definition
7-6	—	Not used. Please set this bit "0".
5-4	SNBR3 [1:0]	OUT3 Snubber resistor selection 00: Fast waveform 01: ↓ 10: ↓ 11: Slow waveform
3	—	Not used. Please set this bit "0".
2-0	SNBC3 [2:0]	OUT3 Snubber capacitor selection 000: Fast waveform 001: ↓ 010: ↓ 011: ↓ 100: ↓ 101: ↓ 110: ↓ 111: Slow waveform

Address 0x1F

Bit	Name	Bit definition
7-6	—	Not used. Please set this bit "0".
5-4	SNBR4 [1:0]	OUT4 Snubber resistor selection 00: Fast waveform 01: ↓ 10: ↓ 11: Slow waveform
3	—	Not used. Please set this bit "0".
2-0	SNBC4 [2:0]	OUT4 Snubber capacitor selection 000: Fast waveform 001: ↓ 010: ↓ 011: ↓ 100: ↓ 101: ↓ 110: ↓ 111: Slow waveform

Address 0x20

Bit	Name	Bit definition
7-6	—	Not used. Please set this bit "0".
5-4	SNBR5 [1:0]	OUT5 Snubber resistor selection 00: Fast waveform 01: ↓ 10: ↓ 11: Slow waveform
3	—	Not used. Please set this bit "0".
2-0	SNBC5 [2:0]	OUT5 Snubber capacitor selection 000: Fast waveform 001: ↓ 010: ↓ 011: ↓ 100: ↓ 101: ↓ 110: ↓ 111: Slow waveform

Address 0x21

Bit	Name	Bit definition
7-5	—	Not used. Please set this bit "0".
4	HFM5_EN	OUT5 HFM output selection 0: Disable 1: Enable
3	HFM4_EN	OUT4 HFM output selection 0: Disable 1: Enable
2	HFM3_EN	OUT3 HFM output selection 0: Disable 1: Enable
1	HFM2_EN	OUT2 HFM output selection 0: Disable 1: Enable
0	HFM1_EN	OUT1 HFM output selection 0: Disable 1: Enable

Address 0x22

Bit	Name	Bit definition
7	HFMCNT_EN	HFM frequency count function selection Please select count circuit in MON_OUTSEL[2:0]. 0: Disable 1: Enable
6-5	―	Not used. Please set this bit "0".
4	HFMCNT_INT	HFM frequency count period selection 0: AD_CLK 8T period 1: AD_CLK 16T period
3-2	―	Not used. Please set this bit "0".
1-0	OSC_SEL [1:0]	HFM circuit selection 00: OUT1,2/OUT3/OUT4,5 is driven by frequency of HFM1 01: OUT1,2/OUT4,5 is driven by frequency of HFM1/HFM2 respectively 10: OUT1,2/OUT3/OUT4,5 is driven by frequency of CLK3 11: OUT1,2/OUT3/OUT4,5 is driven by frequency of AD_CLK

Address 0x23

Bit	Name	Bit definition
7-0	HFMCNT_RB [7:0]	HFM frequency count result (Read only)

Address 0x24

Bit	Name	Bit definition
7-0	HFMF1 [7:0]	HFM1 frequency setting 0d: 65 MHz to 255d: 775 MHz

Address 0x25

Bit	Name	Bit definition
7-0	HFMF2 [7:0]	HFM2 frequency setting 0d: 65 MHz to 255d: 775 MHz

Address 0x26

Bit	Name	Bit definition	
7-5	—	Not used. Please set this bit "0".	
4	EMIS3_1	HFM1 Spread Spectrum mode selection 0: Spreading width = Normal 1: Spreading width = Wide	
3-2	EMIS1 [1:0]	HFM1 Spread Spectrum - spreading width	
		(EMIS3_1 = 0)	(EMIS3_1 = 1)
		(OSC_SEL = 00, 01) 00: OFF 01: 1.1% 10: 2.2% 11: 4.4%	 00: 1.65% 01: 3.3% 10: 6.6% 11: 13.2%
1-0	EMIP1 [1:0]	HFM1 Spread Spectrum - modulation frequency selection 00: 0.013% 01: 0.025% 10: 0.05% 11: 0.1%	

Address 0x27

Bit	Name	Bit definition	
7-5	—	Not used. Please set this bit "0".	
4	EMIS3_2	HFM2 Spread Spectrum mode selection 0: Spreading width = Normal 1: Spreading width = Wide	
3-2	EMIS2 [1:0]	HFM2 Spread Spectrum - spreading width	
		(EMIS3_2 = 0)	(EMIS3_2 = 1)
		(OSC_SEL = 00, 01) 00: OFF 01: 1.1% 10: 2.2% 11: 4.4%	 00: 1.65% 01: 3.3% 10: 6.6% 11: 13.2%
1-0	EMIP2 [1:0]	HFM1 Spread Spectrum - modulation frequency selection 00: 0.013% 01: 0.025% 10: 0.05% 11: 0.1%	

Address 0x28

Bit	Name	Bit definition
7-4	—	Not used. Please set this bit "0".
3-2	HFM_SYNC_PW [1:0]	Fine adjustment of current which decides HFM re-start period 00: 0.5ns 01: 1ns 10: 2ns 11: 4ns
1	HFM_SYNC_LV	Power level of HFM re-start period selection in HFM_SYNC = 1 0: HFM "L" level 1: HFM "H" level
0	HFM_SYNC	HFM timing selection. HFM starts in synchronization with C_SEP timing. 0: Phase synchronization Disable 1: Phase synchronization Enable

Address 0x29

<table>
<tr><th>Bit</th><th>Name</th><th colspan="2">Bit definition</th></tr>
<tr><td>7</td><td>HFM2_DUTY_MODE</td><td colspan="2">HFM2 Duty mode selection
0: Set by HFM Hi-Lo ratio
1: Set by constant delay from HFM Hi period = 67%</td></tr>
<tr><td>6</td><td>HFM2_DUTY_POL</td><td colspan="2">HFM2 constant delay polarity selection
0: Increase HFM Hi period width from 67% (+ adjustment)
1: Decrease HFM Hi period width from 67% (- adjustment)</td></tr>
<tr><td rowspan="2">5-4</td><td rowspan="2">HFM2_DUTY [1:0]</td><td colspan="2">HFM2 DUTY setting</td></tr>
<tr><td>(HFM2_DUTY_MODE = 0)
00: HFM Hi period = 50%
01: HFM Hi period = 67%
10: HFM Hi period = 83%
11: HFM Hi period = 50%</td><td>(HFM2_DUTY_MODE = 1,
polarity of constant delay is selected by HFM2_DUTY_POL)
00: HFM Hi period = 67% ± 0.1 ns
01: HFM Hi period = 67% ± 0.2 ns
10: HFM Hi period = 67% ± 0.3 ns
11: HFM Hi period = 67% ± 0.4 ns</td></tr>
<tr><td>3</td><td>HFM1_DUTY_MODE</td><td colspan="2">HFM1 Duty mode selection
0: Set by HFM Hi-Lo ratio
1: Set by constant delay from HFM Hi period = 67%</td></tr>
<tr><td>2</td><td>HFM1_DUTY_POL</td><td colspan="2">HFM1 constant delay polarity selection
0: Increase HFM Hi period width from 67% (+ adjustment)
1: Decrease HFM Hi period width from 67% (- adjustment)</td></tr>
<tr><td rowspan="2">1-0</td><td rowspan="2">HFM1_DUTY [1:0]</td><td colspan="2">HFM1 DUTY setting</td></tr>
<tr><td>(HFM1_DUTY_MODE = 0)
00: HFM Hi period = 50%
01: HFM Hi period = 67%
10: HFM Hi period = 83%
11: HFM Hi period = 50%</td><td>(HFM1_DUTY_MODE = 1
polarity of constant delay is selected by HFM1_DUTY_POL)
00: HFM Hi period = 67% ± 0.1 ns
01: HFM Hi period = 67% ± 0.2 ns
10: HFM Hi period = 67% ± 0.3 ns
11: HFM Hi period = 67% ± 0.4 ns</td></tr>
</table>

Address 0x2A

Bit	Name	Bit definition
7	AD_ALM	Data decision signal of ADC from output register (Read only) 0: Data decision signal 1: Operation alarm
6-4	—	Not used. Please set this bit "0".
3-2	AD2_RB [9:8]	Upper 2 bit of Data converted by ADC2 result (Read only)
1-0	AD1_RB [9:8]	Upper 2 bit of Data converted by ADC1 result (Read only)

Address 0x2B

Bit	Name	Bit definition
7-0	AD1_RB [7:0]	Lower 8 bit of Data converted by ADC1 result (Read only)

Address 0x2C

Bit	Name	Bit definition
7-0	AD2_RB [7:0]	Lower 8 bit of Data converted by ADC2 result (Read only)

Address 0x2D

Bit	Name	Bit definition
7-0	—	Not used. Please set this bit "0".

Address 0x2E

Bit	Name	Bit definition
7-0	—	Not used. Please set this bit "0".

Address 0x2F

Bit	Name	Bit definition
7	VDAC_MODE	VIDEO Data register control mode 0: Normal (Video Data Input) 1: Register control mode

Address 0x2F, 0x30

Bit	Name	Bit definition
0x2F 1-0	VDAC12[9:8]	VDAC Driver1 and VDAC Driver2 current setting. (VDAC_MODE=1 at usefully) Resolution = [maximum driving current] / 1023 0: 0 mA to 1: [maximum driving current] / 1023 3FF: [maximum driving current]
0x30 7-0	VDAC12[7:0]	

Address 0x2F, 0x31

Bit	Name	Bit definition
0x2F 3-2	VDAC3[9:8]	VDAC Driver3 current setting. (VDAC_MODE=1 at usefully) Resolution = [maximum driving current] / 1023 0: 0 mA to 1: [maximum driving current] / 1023 3FF: [maximum driving current]
0x31 7-0	VDAC3[7:0]	

Address 0x2F, 0x32

Bit	Name	Bit definition
0x2F 5-4	VDAC45[9:8]	VDAC Driver4 and VDAC Driver5 current setting. (VDAC_MODE=1 at usefully) Resolution = [maximum driving current] / 1023 0: 0 mA to 1: [maximum driving current] / 1023 3FF: [maximum driving current]
0x32 7-0	VDAC45[7:0]	

Address 0x33

Bit	Name	Bit definition
7	WCL1_MODE	Compensation function of VDAC Driver1 current mode setting 0: Set by WCL1[6:0] 1: Set by FS1[9:0]
6-0	WCL1[6:0]	Compensation function of VDAC Driver1 current setting

Address 0x34

Bit	Name	Bit definition
7	WCL2_MODE	Compensation function of VDAC Driver2 current mode setting 0: Set by WCL2[6:0] 1: Set by FS2[9:0]
6-0	WCL2[6:0]	Compensation function of VDAC Driver2 current setting

Address 0x35

Bit	Name	Bit definition
7	WCL3_MODE	Compensation function of VDAC Driver3 current mode setting 0: Set by WCL3[6:0] 1: Set by FS3[9:0]
6-0	WCL3[6:0]	Compensation function of VDAC Driver3 current setting

Address 0x36

Bit	Name	Bit definition
7	WCL4_MODE	Compensation function of VDAC Driver4 current mode setting 0: Set by WCL4[6:0] 1: Set by FS4[9:0]
6-0	WCL4[6:0]	Compensation function of VDAC Driver4 current setting

Address 0x37

Bit	Name	Bit definition
7	WCL5_MODE	Compensation function of VDAC Driver5 current mode setting 0: Set by WCL5[6:0] 1: Set by FS5[9:0]
6-0	WCL5[6:0]	Compensation function of VDAC Driver5 current setting

Address 0x38

Bit	Name	Bit definition
7-0	—	Not used. Please set this bit "0".

Description of Operation

Power saving

CXA4007ER becomes power-saving mode when register **OUT1_EN**, **OUT2_EN**, **OUT3_EN, OUT4_EN, OUT5_EN** are set to “0”.

Each output can be enabled individually by setting **OUTx_EN=”1”**. If **OUTx_EN = “0”**, the unselected output stage is power-saving mode.

VA Power Save Mode

When VA pin is set to "L", CXA4007ER transitions to power save mode (i.e. output currents from OUTx is zero and low power operation mode).

The circuits applied this mode are adopted by VA_PSMODE[1:0] setting.

Recovery time from power save mode to normal mode is also decided by VA_PSMODE[1:0] setting.

・VA_PSMODE[1:0]=0d

Turn off output current by setting VA to "L".

Recovery time is about 5nS.

・VA_PSMODE[1:0]=1d

Turn off output current and power down DDR receiver by setting VA to "L".

Recovery time is about 200ns.

・VA_PSMODE[1:0]=2d

Turn off output current and power down DDR receiver and HFM by setting VA to "L".

Recovery time is about 1000ns.

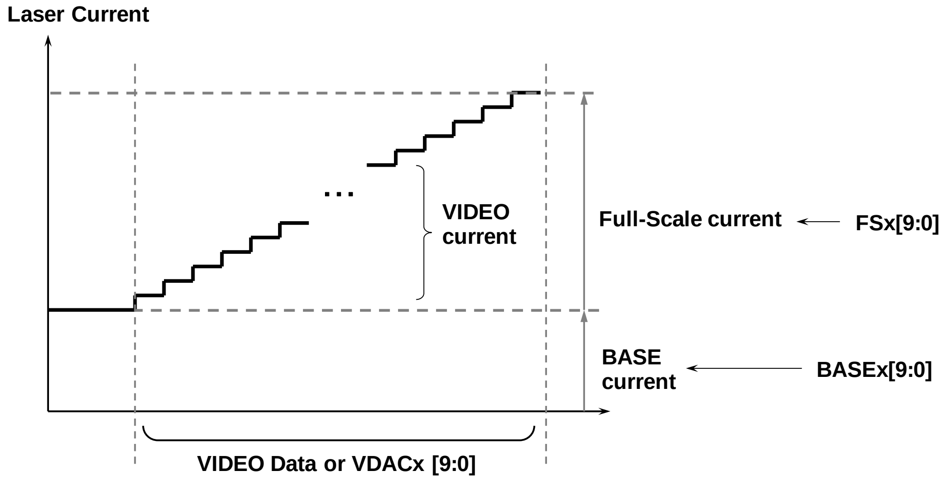
Laser control current

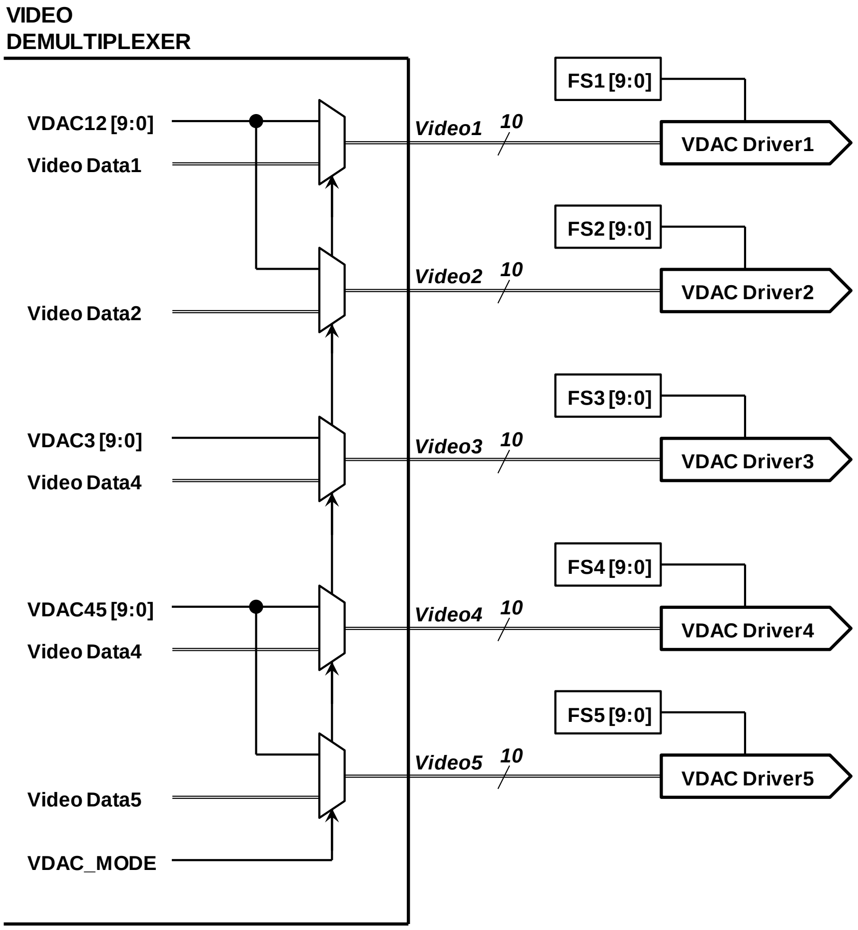
Laser current consists of BASE current and VIDEO current.

The BASE current controls each in register (BASE1[9:0], BASE2[9:0], BASE3[9:0], BASE4[9:0], BASE5[9:0]) for output OUT1, OUT2, OUT3, OUT4, OUT5.

The VIDEO current controls full scale current each in register (**FS1[9:0]**, **FS2[9:0]**, **FS3[9:0], FS4[9:0], FS5[9:0]**) for OUT1, OUT2, OUT3, OUT4, OUT5, and be set by VIDEO Data input. As option, the VIDEO Data input is controllable by register (**VDAC12[9:0], VDAC3[9:0], VDAC45[9:0]**) at the time of VDAC_MODE=1. In this case, VIDEO Data input is not used.

Set OUT1,OUT2 by VDAC12[9:0], and set OUT3 by VDAC3[9:0], and set OUT4,OUT5 by VDAC45[9:0]).

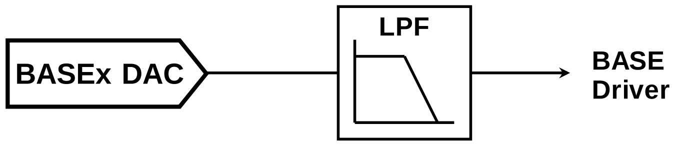




I/O Gain and Bandwidth

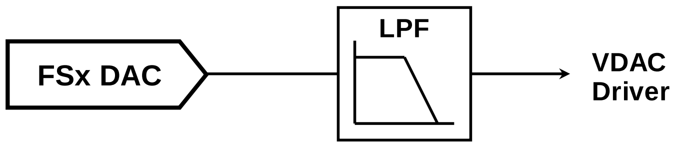
I/O gain of BASE current is decided by the combination of **BASEx_MODE** and **BASEx_GAIN[1:0]** and that of VIDEO current is decided by the combination of **FSx_MODE** and **FSx_GAIN[1:0]**.

Bandwidth of pass from BASEx DAC to OUTx is decided by **BASEx_LPF[1:0]** and that of pass from FSx DAC to OUTx is decided by **FSx_LPF[1:0]**.



BASEx_GAIN [1:0]	BASEx_MODE	
	0	1
00	64%	12%
01	76%	24%
10	88%	36%
11	100%	48%

BASEx_LPF [1:0]	LPF
00	No Limit
01	80kHz
10	25kHz
11	10kHz



FSx_GAIN [1:0]	FSx_MODE	
	0	1
00	64%	12%
01	76%	24%
10	88%	36%
11	100%	48%

FSx_LPF [1:0]	LPF
00	No Limit
01	100kHz
10	50kHz
11	25kHz

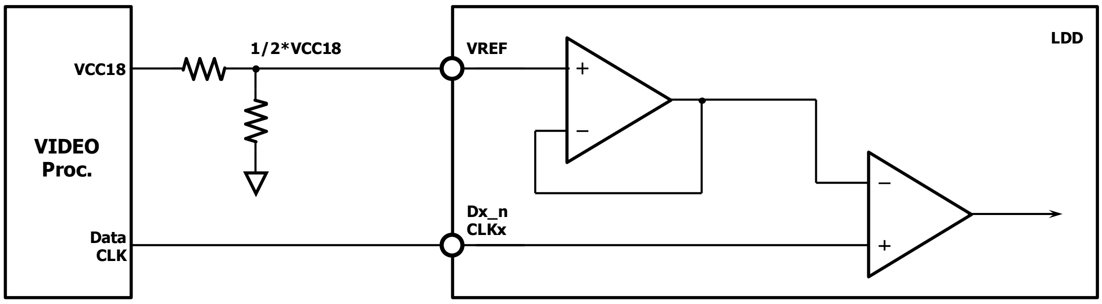
VIDEO Data interface

CXA4007ER has DDR compliant Single input circuit.

SSTL receiver which can receive LVCMOS1.8V is implemented.

VIDEO Data input D1_0 ～ D1_9, D2_0 ～ D2_4, D3_0 ～ D3_9, CLK1, CLK2 and CLK3 are quasi-differential input.

Each input signal is compared to VREF voltage.



VIDEO Data format

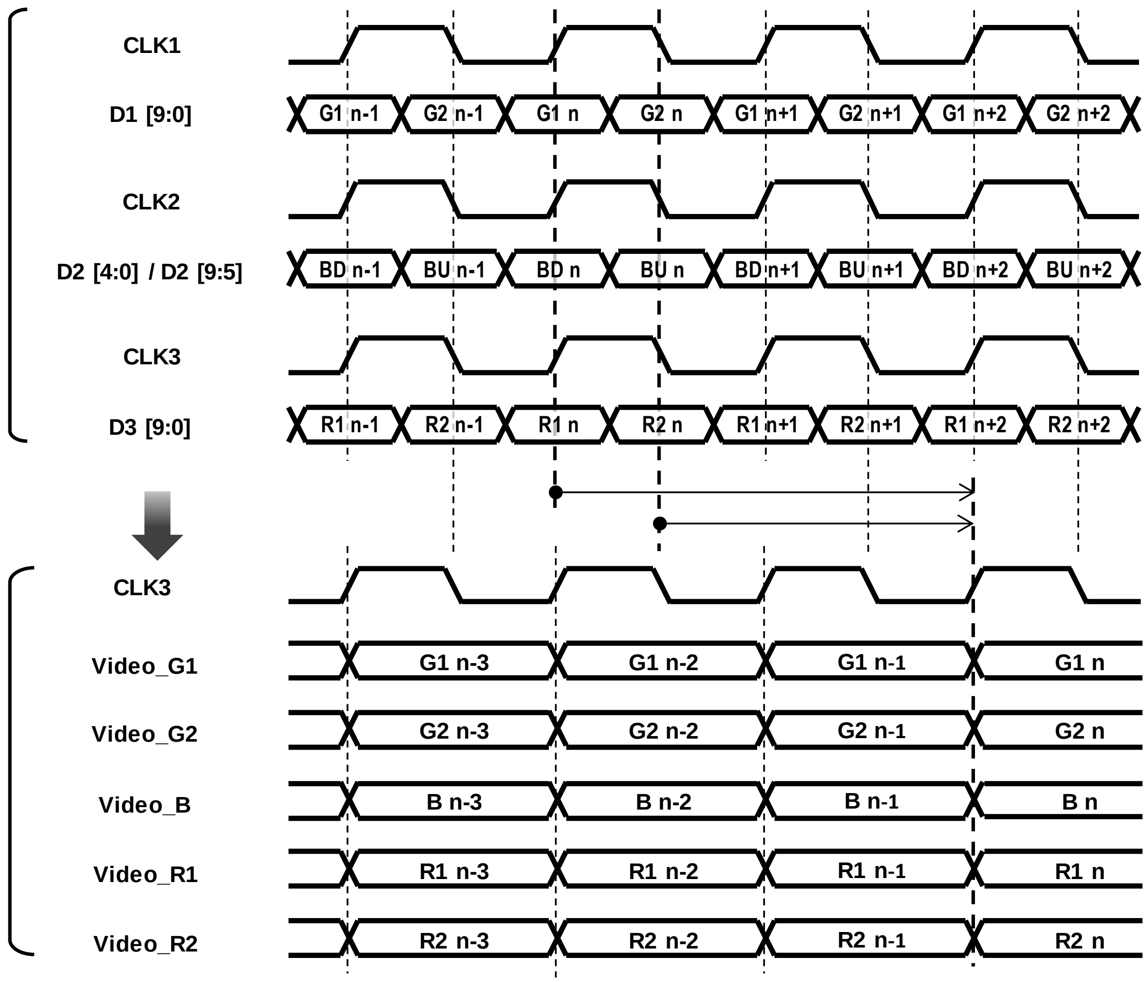
Input circuit conforms to DDR.

Video Data, Clock, Clock edge and output are assigned the following table.

DATA	CLOCK	Edge	OUTPUT
D1[9:0]	CLK1	Pos	OUT1
D1[9:0]	CLK1	Neg	OUT2
D2[4:0]	CLK2	Pos & Neg	OUT3
D3[9:0]	CLK3	Pos	OUT4
D3[9:0]	CLK3	Neg	OUT5

For example, if VIDEO Data and Clock are input as shown in below timing chart, VIDEO_R1 / VIDEO_R2 / VIDEO_B / VIDEO_G1 / VIDEO_G2 are sent to OUT1 / OUT2 / OUT3 / OUT4 / OUT5.

※Note : This timing chart is not taken into account the propagation delay.



Video Data for OUT2 is only 5 line. Therefore, it is necessary for D2[4:0] to be send data divided into two : first is lower 5 bit data, second is upper 5 bit data. Coordinated to each internal VIDEO Data in internal CLK3 timing. therefore, CLK3 input is necessary for each VIDEO Data.

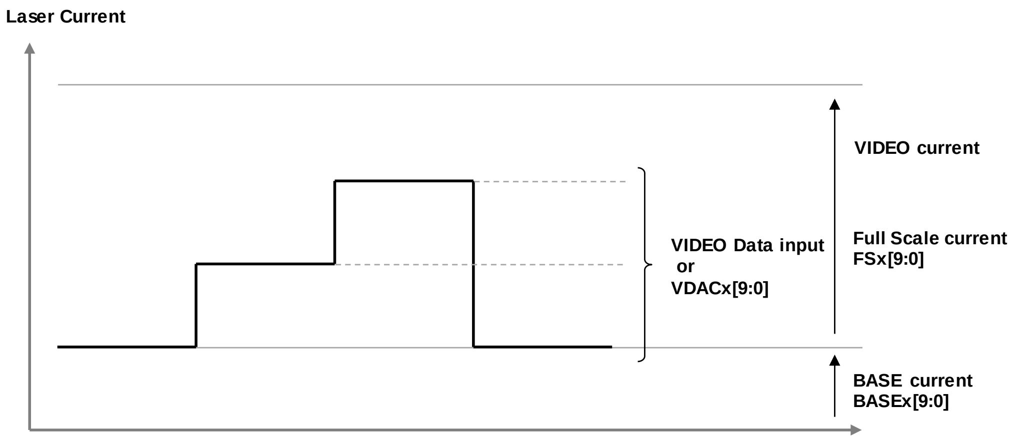
Output current control

Output current is controlled by **VAx[1:0]** setting when VA = “H”.

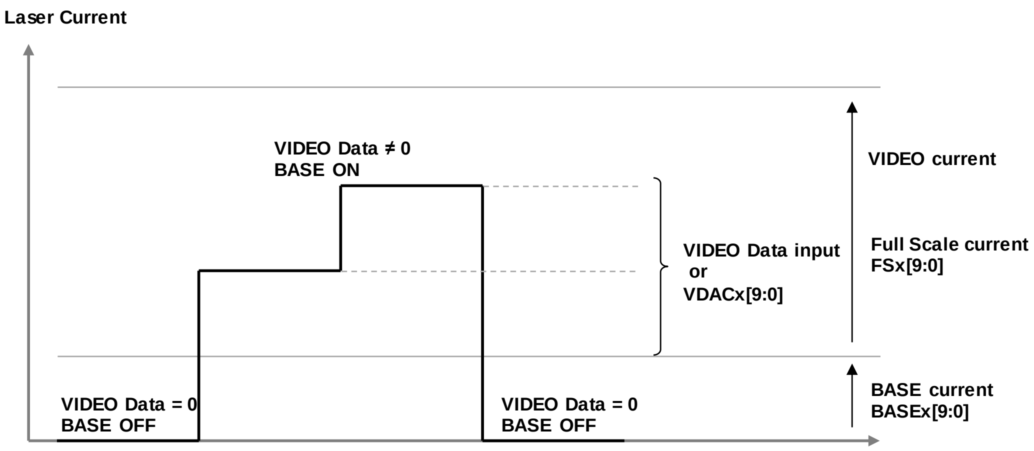
1. **VAx[1:0] = 0d**
   Output current is OFF even if VA = “H”.

2. **VAx[1:0] = 1d**
   VIDEO current is ON. VIDEO current is decided by **FSx[9:0]** setting and VIDEO Data.
   BASE current is OFF.

3. **VAx[1:0] = 2d**
   VIDEO current and BASE current are ON.
   VIDEO current is decided by **FSx[9:0]** setting and VIDEO Data.
   BASE current is decided by **BASE[9:0]** setting.



4. **VAx[1:0] = 3d**
   VIDEO current and BASE current are ON.
   VIDEO current is decided by **FSx[9:0]** setting and VIDEO Data.
   BASE current is decided by **BASE[9:0]** setting and VIDEO Data.
   video data ≠ 0: Base driver outputs current in synchronization with VIDEO Data.
   video data ＝ 0: Base driver stops current in synchronization with VIDEO Data.



Output waveform compensation

CXA4007ER has programmable snubber for each output.

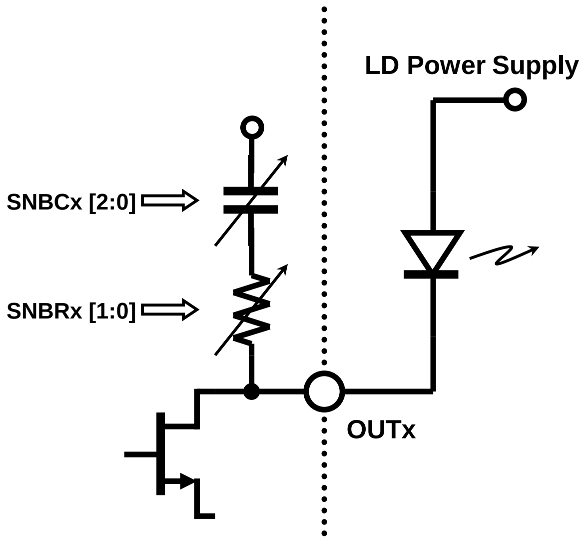
OUT1 waveform can be compensated by setting **SNBC1[2:0]** and **SNBR1[1:0]**.

OUT2 waveform can be compensated by setting **SNBC2[2:0]** and **SNBR2[1:0]**.

OUT3 waveform can be compensated by setting **SNBC3[2:0]** and **SNBR3[1:0]**.

OUT4 waveform can be compensated by setting **SNBC4[2:0]** and **SNBR4[1:0]**.

OUT5 waveform can be compensated by setting **SNBC5[2:0]** and **SNBR5[1:0]**.



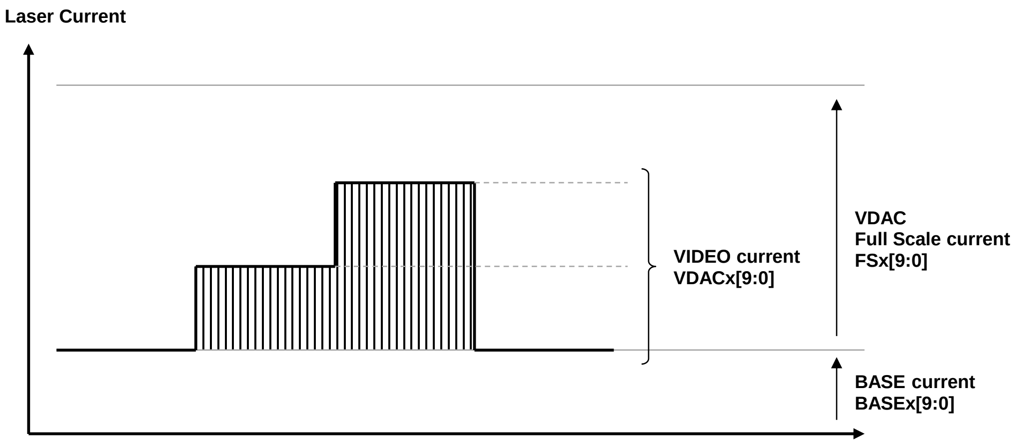
High Frequency Modulation (HFM)

HFM ON/OFF control is possible to each output by **OSCx_EN**.

1.HFM mode

In this mode, HFM amplitude depends on VIDEO Data setting.

HFM selected is possible to each output by **OSC_SEL[1:0].**



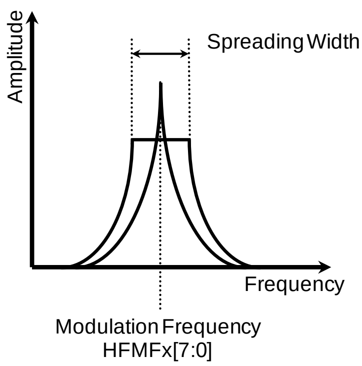
2.HFM frequency setting

HFM frequency is decided by setting **HFMFx[7:0]**.

Frequency Range : 100 MHz ～ 500 MHz

3.HFM Spread Spectrum Function

The HFM spread spectrum function is enabled by **EMIS [1:0] ≠ 0d and EMI3_x** and the spectrum is spread as shown in the figure below. The HFM spreading width becomes big in **EMIS3_x=1d.**



High Frequency Count Function

While **HFMCNT_EN = 1d**, HFM frequency can be counted by setting **HFMF1 [7:0] and HFMF2[7:0]**. HFM count can select target output pin by setting **MON_OUTSEL[2:0]**.The result is stored to **HFMCNT_RB [7:0]**, which can be read back by the serial interface.

Measurement period (8T, 16Cycle) can be set by **HFMCNT_INT**. HFM frequency can be calculated by using the count result and measurement period setting **HFMCNT_INT**. Though the counter overflowed, the count result don't keep value 0d or 255d and the counter continues counting operation.

This function is disabled when **HFMCNT_EN = 0**,

Calculating formula

HFM frequency f = (N × 256 + Count) × CLK/M

Where,

f = HFM frequency [MHz], CLK = AD_CLK [MHz], M = Measurement period [Cycle], Count = Count result,
N = Overflowed number of times.

MONITOR

CXA4007ER can monitor following signals from MONITOR pin. OUTx pin voltage (VOP monitor), Temperature sensor voltage.

VOP monitor can select target output pin by setting **MON_OUTSEL[2:0]**.

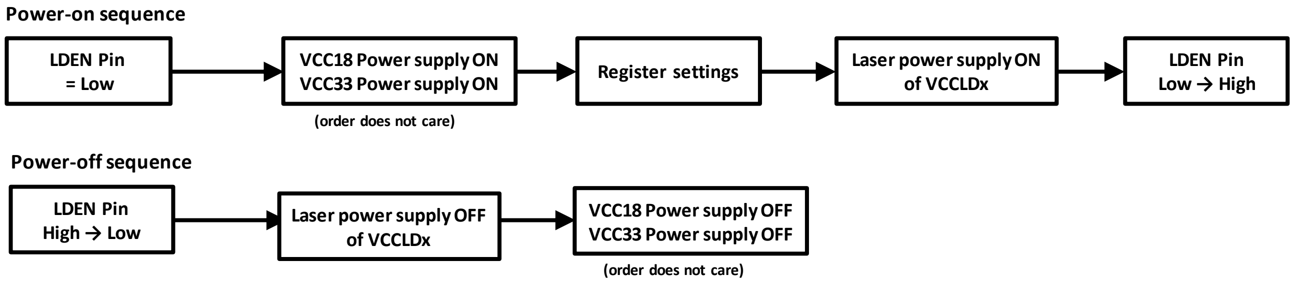
Emergency Detection function

CXA4007ER has power supply voltage monitoring circuit for safety LD emission. This function monitors 2 power supply voltage VCC33 and VCC18. Please refer to electrical characteristics for detecting threshold voltage. If emergency state is detected from VCC33 or VCC18, emergency detecting circuit outputs LDOFF signal. Then all output current is forced off when **EMVCC_EN = 1d**.

EMVCC_RB is a read only register. To clear error bit, please operate serial interface for dummy data write to **Address:0x05** after error condition recoverd.

Output signal of error detecting circuit can be monitored from MONITOR pin by setting **EMVCC_MON = 1d**.

Power-on and power-off sequences



Notes on Operation

IR pin

Use a high-accuracy resistor for an external resistor (22 kΩ) of (42) IR pin.
The resistance allowance of 22 kΩ affects the setting accuracy of modulation frequency.
In additional, the wiring to an external resistor should be as short as possible. It may affect characteristics including the output noise.

Allowable power dissipation

The allowable dissipation is defined to be the dissipation which the junction temperature does not exceed 150 ˚C.
From thermal resistance between junction and ambience, the allowable dissipation can be calculated by the equation below.

Allowable power dissipation (PD) = (150 ˚C - ambient temperature)/(θj-a)

The thermal resistance between junction and ambience (θj-a) is expressed by following equation.

(θj-a) = (θj-c) + (θc-a)

θj-c : Thermal resistance between junction and package = 2 ˚C /W

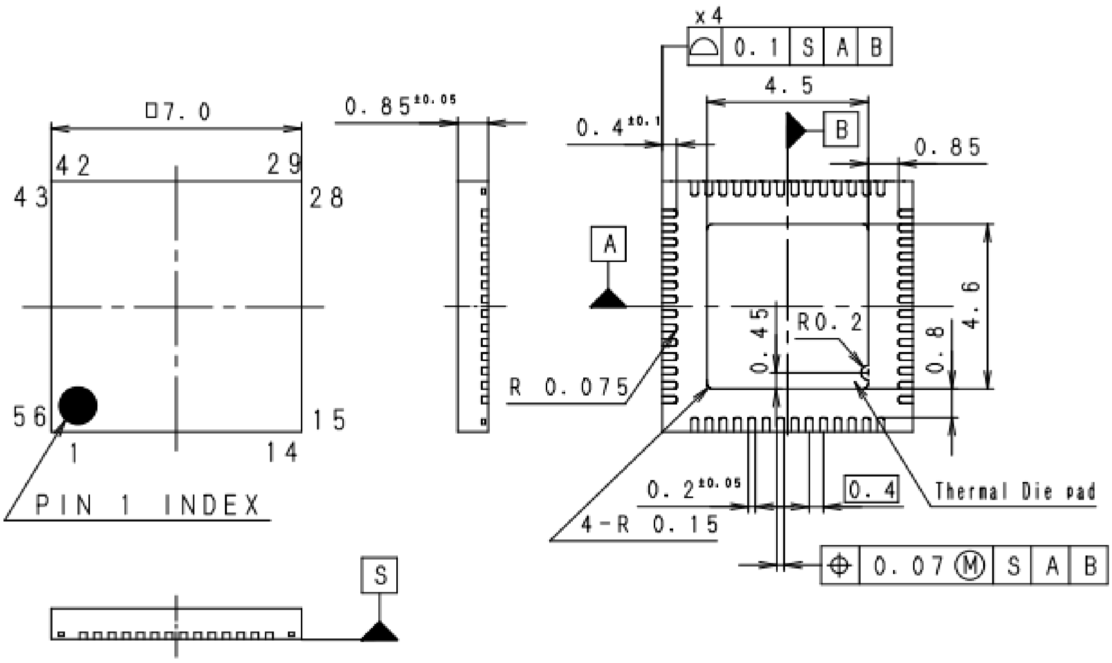
θc-a : Thermal resistance between package and ambience

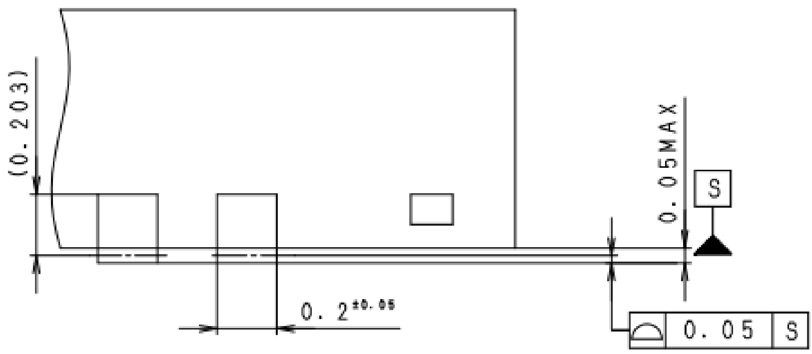
Find thermal resistance between package and ambience (θc-a) from power consumption and package surface temperature, at the condition that CXA4007ER is mounted on PWB. Then calculate the allowable power dissipation.

Package Outline

(Unit : mm)

56PIN VQFN (PLASTIC)





TERMINAL SECTION

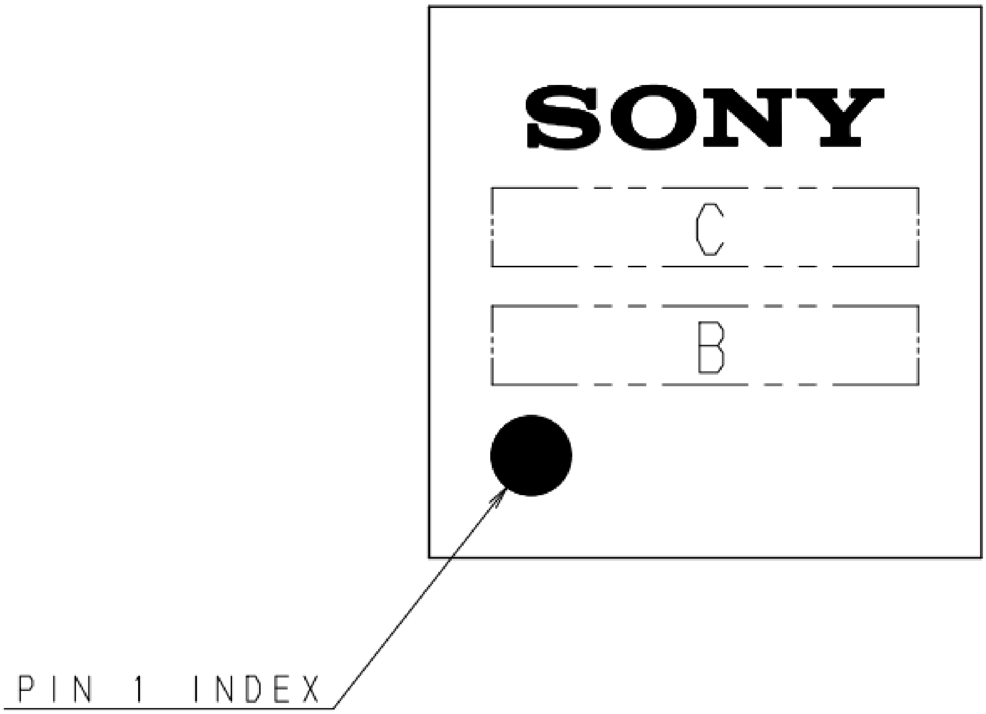
PACKAGE STRUCTURE

SONY CODE	VQFN-56P-311
JEITA CODE	P-VQFN56-7×7-0. 4
JEDEC CODE	———

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	Sn PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0. 12g

PART No. AP-2000-56QNAF1	Rev. 0
ISSUED 14. 01. 28	REVISED
PRODUCTION LINE	COMPILING DIV. SONY SEMICONDUCTOR.
REMARKS PKG CODE:ER-056-M	

Marking



MARKING C: A4007ER

注1） C部は製品名（Max7文字）を配置する。

（7文字を超える場合は製品名省略標示規定に従う。）

2） B部はロット番号（Max7文字）を配置する。

< INSTRUCTIONS >

1) TYPE NO. (MAX 7 CHARACTERS) IN SECTION C.

(FOR MORE THAN 7 CHARACTERS FOLLOW RULES FOR ABBREVIATIONS.)

2) LOT NO. (MAX 7 CHARACTERS) IN SECTION B.

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