MTC-20124

Integrated ADSL
CMOS Analog Front-end
Circuit

Data Sheet

Preliminary (Rev 1c Aug 1996)

Features

- **Fully integrated AFE**
- **Overall 12 bit resolution, 10k-768kHz signal bandwidth**
- **1.54 MS/s ΣΔ ADC**
- **1.54 MS/s ΣΔ DAC**
- **Single 5V operation**
- **THD: - 60dB @ full scale**
- **4 bit digital interface**
- **1V full scale input**
- **Differential analog I/O**
- **Accurate continuous-time channel filtering**
- **14th order, Chebyshev BP filter 1% trimmed**

Applications

- **Very high speed modems (fast internet access)**
- **Digital Subscriber Loop (xDSL) modem**
- **Video-On-Demand public network (Line Termination and Network Termination mode)**
- **Video telephony**
- **High rate, high resolution data conversion**
- **Wide band, low noise filtering**

General Description

Fig.1 shows the top level block schematic of the analog front-end circuit. The circuit is configured to operate in NT mode; the alternative configuration for operation at the LT side is indicated by the dotted connections. The best Signal/Noise ratio and filtering performance is obtained by first amplifying the receive signal with a low-noise variable gain preamplifier. As the amplifier output also contains the very high echo signal which would saturate the continuous-time bandpass

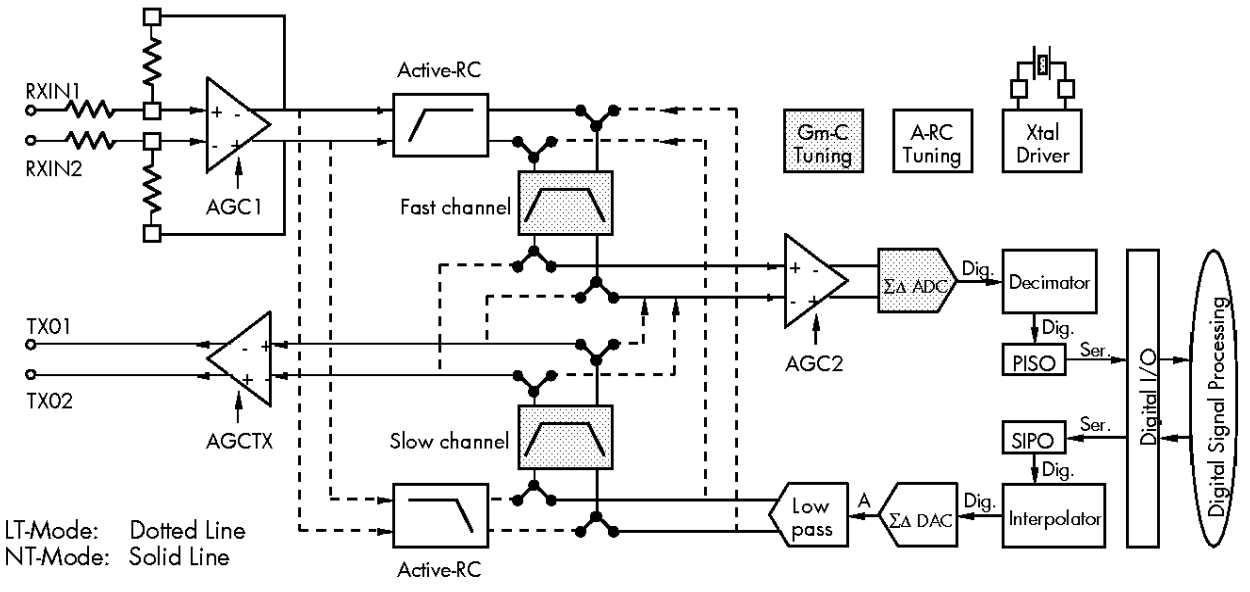

Fig.1: Block Diagram of MTC-20124

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filters, active-RC filters are used to first reduce the echo signal to an acceptable level. These active-RC filters use a tunable capacitor approach; as a result, the roll-off frequency variation is less than 5% over the process and temperature range. The bandpass filters eliminate echo and out-of-band interference. To achieve at least 12 bit resolution at 1.54 Msamples/s, a 4th order cascaded ΣΔ modulator (Fig.3) with a sampling frequency of 49.15 MHz is selected, corresponding to an oversampling ratio of 32. The decimation is performed by a 5th order digital comb filter.

In the transmit direction, the digital data is first up-sampled in a digital interpolation filter. A 6th order ΣΔ modulator is used to generate a 49.15 Mbit/s PDM signal (Fig.4). This is further converted into an analog signal by an SC-type LP filter followed by a 2nd order Sallen&Key filter. To further attenuate high frequency PDM noise and out-of-band noise, a second continuous-time bandpass filter is used. The transmit power is controlled by the transmit AGC amplifier.
A crystal oscillator driver is provided to generate the 49.15 MHz master clock with an external crystal. Amplitude regulation is employed to minimize the frequency pulling.

Main Blocks Description

Filtering Section

• OTA-C bandpass filter

Two bandpass filters are needed for accurate channel separation and out-of-band noise filtering. The selectivity requirements demand the use of 14th order Chebyshev filters with 1.5 dB in-band ripple. Since the fast channel bandpass filter operates in the MHz range, a Gm-C architecture is used because of its low power and high frequency capability. The same technique is used for the slow channel filter so that only one on-chip tuning circuit is needed.

To obtain linearity in excess of 60 dB, a highly linear integrator, based on source degeneration with linear resistors is used (Fig.2).

A super Gm input stage is used to realize the linear V- I conversion. The amount of the output integrating current is controlled by the three tuning transistors M1 - M2 - M3. As the tuning transistors experience only a small voltage swing, superior linearity results compared to the MOSFET-C filter where the tuning MOSFET experiences the full signal swing. It can be shown that as long as the voltage across M1 is differential, no distortion will be generated by the tuning transistors.

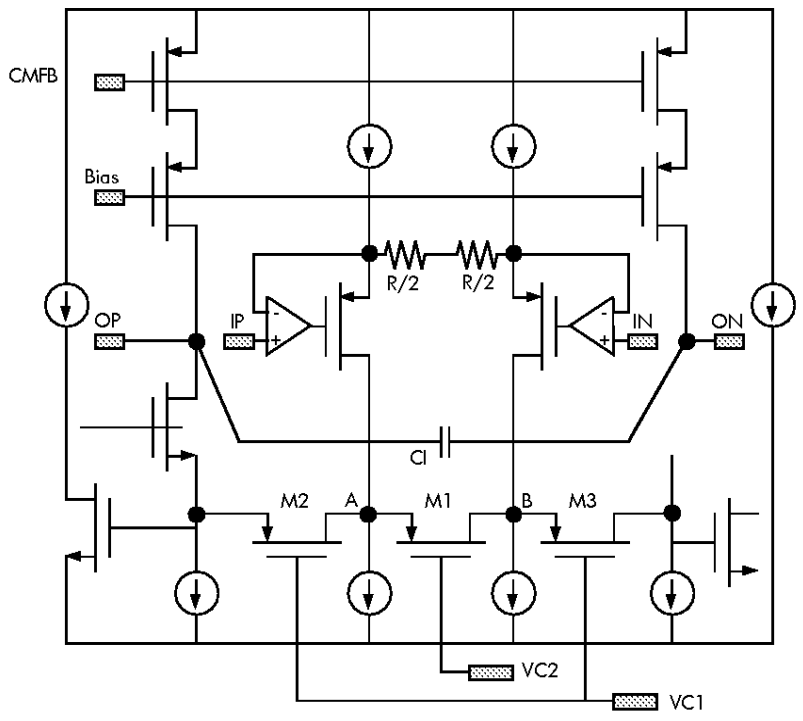

Fig.2: OTA-C Basic Structure

• Frequency tuning

Since the filter frequencies are determined by the Gm/C ratio, either Gm and C can be tuned. However, for linearity, high linear poly-diffusion capacitors must be used which cannot be tuned in a continuous way.
Therefore, the tuning must be realized by tuning the Gm value. The large signal transconductance Gm of the OTA in Fig.2 can be tuned by the voltages VC1 and VC2 at the gates of the three transistors.
Using this technique, the GM can be tuned from 28% to 72% of its maximal value with stable performance over the whole tuning range. The system clock is used as the reference frequency. No external capacitors are required for the tuning circuit.

Analog to Digital Converter

• ΣΔ ADC Modulator

The ADC is a 4th order ΣΔ modulator based on the cascaded approach as shown in Fig.3. This topology combines the stability of classical 1st and 2nd order ΣΔ modulators with the noise shaping characteristics of higher order modulators. This makes it possible to use a low oversampling ratio of only 32 to achieve 12 bit accuracy at 1.54 MHz Nyquist rate in a CMOS technology. The top level verification of the ADC are performed using dedicated behavioral simulation program. Based on top level simulations, the basic design requirements for the basic building blocks such as integrators and voltage reference buffers are defined.

• Noise cancellation and decimation

The three outputs of the ΣΔ modulator are combined digitally in order to cancel the quantisation noise.
The remaining quantisation noise, shaped to high frequency, is attenuated in a special digital filter: the decimator. This filter combines the undersampling (decimation) operation with a COMB structure that performs a 5th order low pass filtering.
A decimation to 2 times the Nyquist rate is performed by this filter.

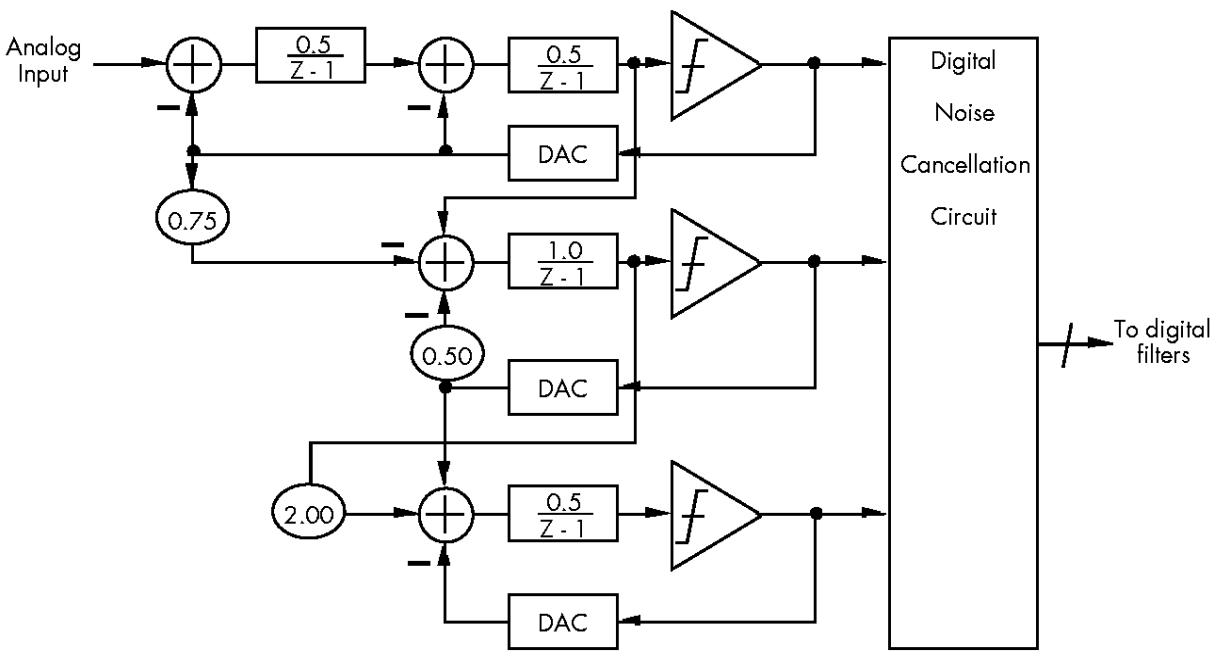

Fig.3: ΣΔ AD Modulator

Digital to Analog Converter

• The ΣΔ DAC modulator

The D/A conversion in the transmit path is done by a 6th order digital ΣΔ modulator using the multiple feedback technique with an oversampling ratio of 32 (Fig.4). Three transmission zeros are included in the Noise Transfer Function (NTF) to increase the peak S/N ratio. To guarantee the stability, the input signal is clipped in a preceding interpolation filter. Internal scaling is performed to maximize the dynamic range and to avoid internal overload.

• DA converter - low pass filter

The low pass filter is a combination of a switched-capacitor low pass 1st order combined with a 2nd order continuous-time low pass Sallen&Key filter. The ripple in the band is kept within 1.5 dB. Pole position has been minimized by using the overshoot characteristic of the 2nd order to compensate the attenuation near the corner frequency. The circuits are implemented using full differential design techniques.

The remaining quantisation noise is suppressed by the bandpass filter following this block in the transmission path.

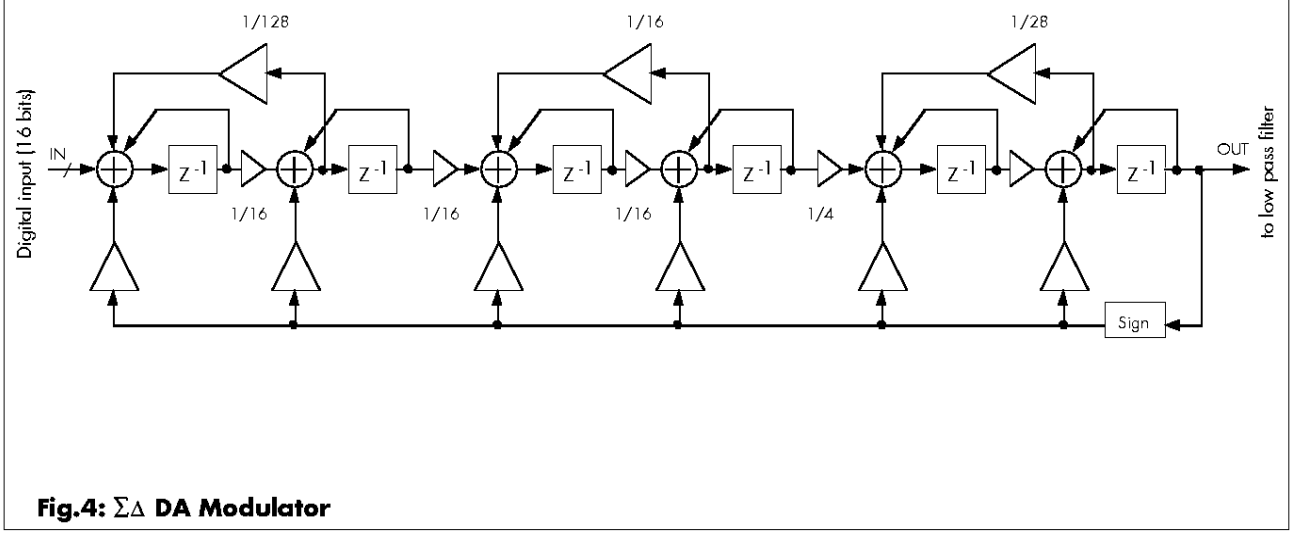

Fig.4: ΣΔ DA Modulator

Digital Interface

The interface of the digital data to the outside world is achieved by using parallel to serial multiplexers (PISO and SIPO in Fig.1).
The internal 16 bit wide digital words are multiplexed onto four serial words, each of 4 bit wide, to interface with the external environment.
The arrangement of the data on the serial lines are shown in Table 1.

The data on the parallel format are clocked with the CLWD signal (3.072 MHz), the serial data are latched out with the rising edge of the CLNB clock (12.284 MHz). This last clock has a rate four times higher than the first one. Both are synchronized onto the master clock (49.15 MHz).

To enter into the chip the serial data is at the falling edge of the CLNB clock.

PISO: Paralell In-Serial Out multiplexer
SIPO: Serial In-Parallel Out multiplexer

Table 1: Parallel to Serial Interface Data Arrangement

Parallel data	Serial data				
(MSB) B16	T0	T1	T2	T3	
. .	B01	B05	B09	B13	Rx1 /Tx1
. .	B02	B06	B10	B14	Rx2 /Tx2
. .	B03	B07	B11	B15	Rx3 /Tx3
(LSB) B01	B04	B08	B12	B16	Rx4 /Tx4

VCXO

A voltage control crystal oscillator driver is integrated in MTC-20124. Its nominal frequency is 49.152MHz. The quartz crystal is connected between the pins XTAL1 and XTAL2. The oscillator driver drives the third overtone of the quartz crystal. The quartz crystal must be manufactured so that its dynamic capacitance is larger than Cm>2.5fF and it oscillates at the nominal frequency with a load capacitance CL equals to 10pF.

The control voltage is derived from a return-to-zero PDM signal coming from the MTC-20125. The PDM is always zero when there is no clock. The PDM is taken by the MTC-20124 at the pin VXCIN and is converted to an analog signal in the MTC-20124. The analog signal is then sent to the external pin at VCXOUT where a large capacitor (i.e. 100nF) is used for low pass filtering. The analog control voltage at VCXOUT is further amplified by an external amplifier to generate the required control voltage (range: -12V to 1V) for the varicap.
The VCXO characteristics are given in Table.2

Table 2: VCXO characteristics

PARAMETERS	Min	Nominal	Max	Note
Absolute frequency accuracy	-15ppm	49.152Mhz	+15ppm	
Frequency tunning range		±30ppm		Cm=2.5fF

N.B: Frequency tuning range is proportional to the crystal dynamic capacitance Cm.(e.g. if Cm=1.5fF the tunung range will be ± 18 ppm).
The tuning must be monotonic with 8-bit resolution with the worst-case tuning steps of <2ppm/LSB (8-bit). The time constant of the tuning must be variable from 5s to 10s through an external capacitor Ct.

Digital Part Bypass

When pin BYPAS=1, the digital part of the A/D and D/A convertors are bypassed. This mode will not affect the analog functional blocks.

Following conditions are obtained :
- The three A/D PDM output signals are directly transmitted to outside via pins RXD<3:1>.
- The decimator is not active.
- The D/A PDM input signal is received from outside via pin TXDO.
- The interpolator and digital modular are not active.
- The PISO and SIPO multiplexers are not active.

Power Down

When pin PDOWN="O", the chip is set in power down mode. In this mode all analog functional blocks are deactivated except : preamplifier, activation detector, clock circuits for output clock CLKO. PDOWN will not affect the digital part of the chip. The chip is activated when PDOWN="1".

There are four different modes available. The selection of the operation mode is controlled by the 3 inputs Scantest (SCN), TRIM and TEST. The selection table is shown in table 3.

Input Signal Detection Circuit

The circuit detects the presence of an "activate" input signal on pins RXIN1 and RXIN2. It sets pin ACTI logic high if an activate input signal is detected. Otherwise, the pin ACTI is kept logic low.

Reset Function

The reset function is active when the RESET pin is at a low voltage input level. Under this condition, the reset function can be easily used for power up reset conditions.

Test

The test functions are implemented for component test only. However, some test functions can be used for extended system tests (table 3).

Table 3 : Test mode selection table

	SCN	TRIM	TEST
Normal mode	0	0	0
Scan test mode	1	0	X
Timming mode	0	1	X
Test mode	0	X	1

Performance

The complete analog front-end circuit is fabricated in the C07M-A 0.7 µ CMOS technology. The circuit is powered by a single 5V supply and typically consumes 1.2W power. 90% of the power is used by the ΣΔ AD and DA converters due to 49.15 MHz sampling frequency. Main characteristics are given in Table 4.The intermodulation distortion IM3 for a 4Vpp input signal is lower than -60dB. The complete DAC achieves 12 bit resolution limited by the kT/C noise in the SC-filter.

Table 4: Performance Characteristics (Nominal condition)

Parameter	Typical value
Gm-C BP Filters :	
IM3 for Vin=4Vpp @ 80 kHz	- 63 dB
@ 500 kHz	- 55 dB
Corner frequency: slow channel:	12 kHz - 96 kHz
fast channel:	138 kHz - 768 kHz
Center fc accuracy	< ± 1% error
fc tuning range: slow channel:	17 kHz - 49 kHz
fast channel:	171 kHz - 481 kHz
Equivalent noise: slow channel:	450 nV/√Hz
fast channel:	280 nV/√Hz
ADC/DAC :	
Reference voltage	± 1 V
Sampling frequency:	49.15 MHz
SNR: ADC (after 32 decimation)	69 dB
DAC (after 32 decimation)	73 dB
Power dissipation	1.2 W (Supply = 5 V)
Analog:	1.0 W
Digital:	0.2 W

Chip Package

The chip is noused in a 144 pin EQFP package.
The package provides a heat sink in order to dissipate the power necessary to handle high bandwidth performance. In order to reduce the disturbance generated by high speed digital switching, several pins have been allocated for power supply connection.
For the same reason, there are 4 pins on each side of chip allocated to ground connections.

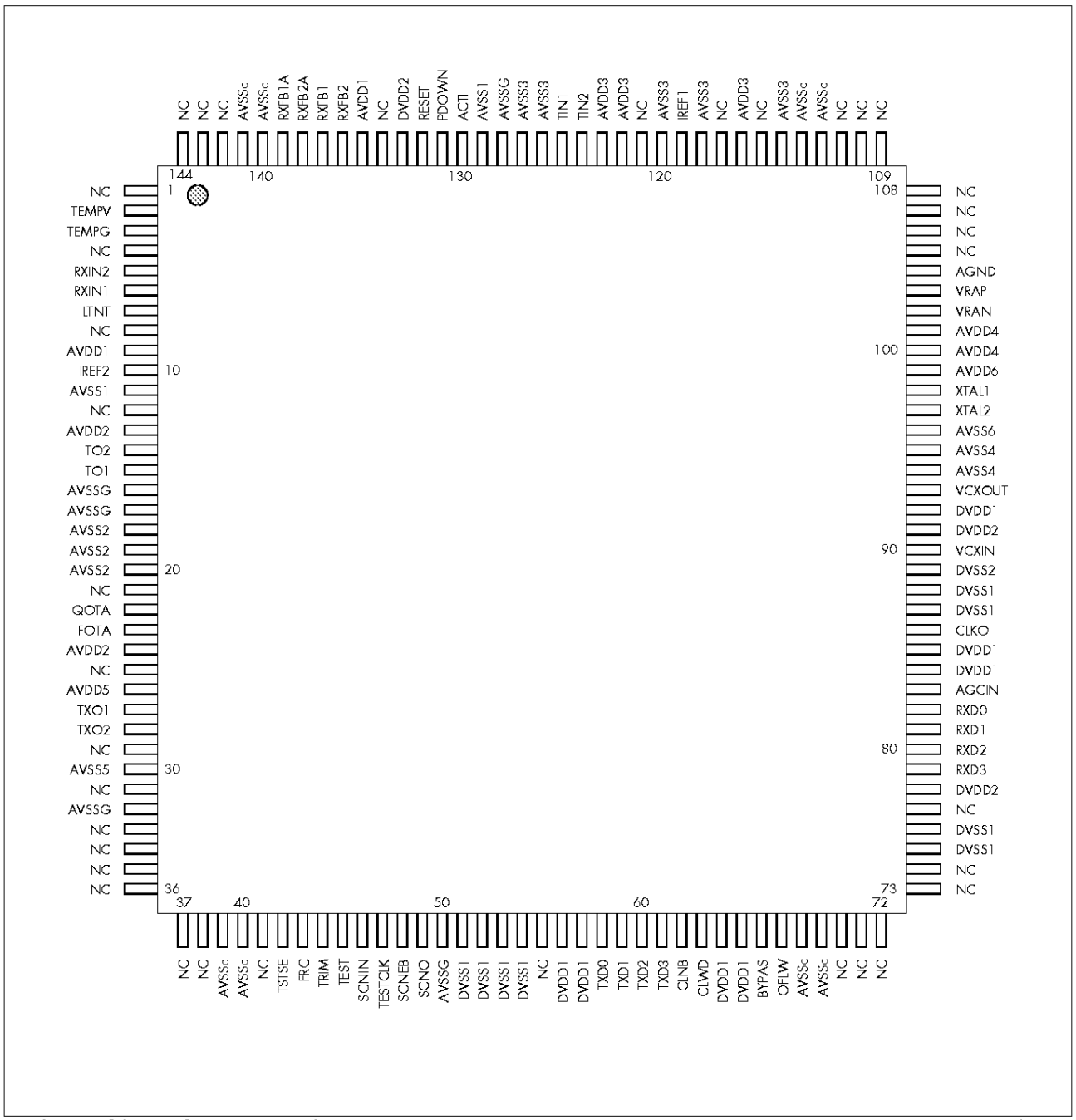

Fig.5: Chip Package: 144 pin EQFP NC = Not connected

Chip Package Electrical Ratings and Characteristics

Limiting capabilities

Limiting capabilities are those parameter limits above which damage to the integrated circuit may occur. It is not implied that more than one of these conditions can be applied simultaneously.

- During power on or power off surges, the device withstands 7 V on the VDD line for up to one second.
- During testing, output pins withstand being shorted to either VDD or VSS, for up to one second (min. 1 minute between events).
- AVDDX, DVDD1 will not differ over more than +/-0.5v.
- AVSSx and DVSSx are connected to external analog and digital ground plates.

Table 5 : Absolute Maximum ratings

Symbol	Parameter Description	Min	Max	Unit
VDD	Any VDD supply voltage, related to substrate	-0.3	7	V
VIN	Voltage at any input pin	-0.7	7	V
Tstg	Storage Temperature	-65	150	°C
TL	Lead Temperature (10 second soldering)		300	°C
ILU	Latch-up current @ 80°C	50		mA

Transient Energy Capability

ESD

ESD testing has to be performed according to ± 1000V for the Human Body Model (HBM) and ± 200V for the Charged Device Model (CDM).

Latch-up

Maximum current (sinking or sourcing) into/from any pin must be less then 100 mA to prevent latch-up.

Thermal Data

The junction to ambient thermal resistance RthA when mounted on a horizontal printed board in still air is less then 30° C/W.

Reliability

Device failure rate objective : 250 FIT (≠ failures/10^9 component.hours).

Operating conditions

Unless specified, the characteristic limits of 'Static characteristics' in this document apply over an operating temperature range of 0°C to 70°C and for VDD within the range : +4.75V to +5.25V ref. to substrate. (DVDD2 from 3V to 5.25V).

The ambient temperature when testing the device on ATE equipment shall be raised in function of the test time as to guarantee the same chip temperature as on board level at 70°C ambient.

Table 6 : Operating Conditions

Symbol	Parameter Description	Min	Max	Unit
AVDD	AVDD supply voltage, related to substrate	4.75	5.25	V
DVDD1	DVDD1 supply voltage, related to substrate	4.75	5.25	V
Vin, Vout	Voltage at any input and output pin	0	VDD	V
Pd	Power Dissipation (BYPASS=0:ADSLA mode)	1.0	1.4	W
Ta	Ambient Temperature	0	70	°C
DVDD2	Supply voltage for digital I/O's	3.0 4.75	3.6 5.25	V V

Static Characteristics

Power Supply

Table 7 : Static current consumption at 5V. VDD

Symbol	Parameter	Test Conditions		TYP	Max	Unit
IVDD	Supply total current VDD=5V	BYPAS=0	Power up	200	240	mA
IVDD			Power down	TBD	TBD	mA

Digital inputs
CMOS inputs : (TXDx, PDOWN, AGCIN, SCNIN, SCN, SCNCLK, TSTSE, FRC, TRIM, TEST, RESET, BYPAS)

Table 8 : Characteritics of digital inputs

Symbol	Parameter	Test Cond	Min	Max	Unit
VIL	Low level input voltage			0.3*DVDD2	V
VIH	High level input voltage		0.7*DVDD2		V
IIL	Low level input current	VDD=max VIL=0V		10	µA
IIh	High level input current	VDD=max VIH=5.25V		10	µA
C_{inp}	Input capacitance			7	pF

CMOS inputs on analog supply: (LT/NT)

Table 9 : Characteristics of digital inputs

Symbol	Parameter	Test Cond.	Min	Max	Unit
VIL	Low level input voltage			0.3*AVDD	V
VIH	High level input voltage		0.7*AVDD		V
IIL	Low level input current	VDD=max VIL=0V		10	µA
IIh	High level input current	VDD=max VIH=5.25V		10	µA
Cinp	Input capacitance			7	pF

Digital outputs

Hard driven outputs : (RXDx, CLKO, CLNIB, CLWD, ACTI, SCNO)

Table 10 : Characteristics of digital outputs

Symbol	Parameter	Test Cond.	Min	Max	Unit
VOL	Low level output voltage	IOUT=-4mA		0.15*DVDD2	V
VOH	High level output voltage	IOUT=-4mA	0.85*DVDD2		V
CLOAD	Load capacitance			30	pF

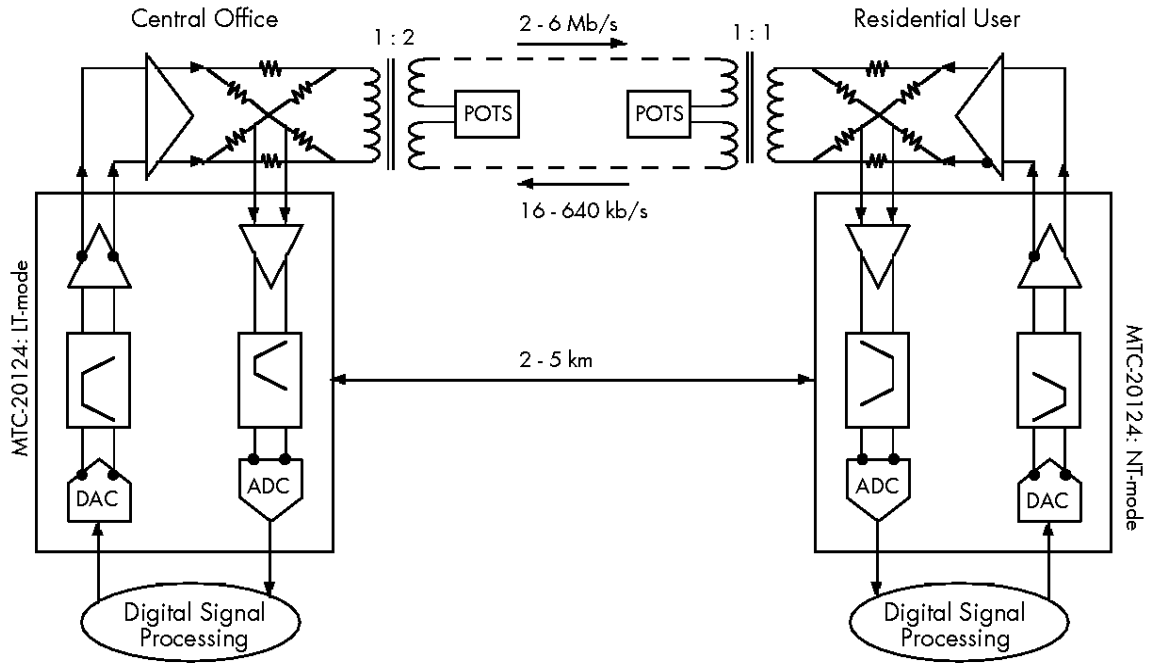

Fig.6: ADSL Front-end Application

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