FUJITSU SEMICONDUCTOR
DATA SHEET

DS04-31103-1E

ASSP for Graphics Control

Graphics Display Controller

MB86292

■ DESCRIPTION

The MB86292 is an evolved version of the Fujitsu MB86290A graphics controller designed for use in a car navigation system or amusement equipment. The MB86292 is a graphics display controller with an on-chip geometry processor and digital video capture facility. It can be connected to FCRAM.
Connecting the MB86292 to FCRAM which has lower latency upon a paging error speeds up the random access to memory, resulting in faster display and drawing. In addition, integrating the geometry processor reduces the CPU load, thereby improving the performance of the entire system.

■ FEATURES

- Operating frequency : 100 MHz (External clock of 14.32 MHz Max)
- Geometry processor : Capable of executing operations for geometric transformation and surface front/rear evaluation.
- Memory block : Capable of connecting SDRAM and FCRAM
- Video capture block : Embedded facility to capture digital video images, for example, from TV, capable of easily implementing “Picture in Picture” and video graphics superimposing.
- Host interface : Enables direct connection to various CPUs (Fujitsu SparcLite, Hitachi SH3/4 or NEC V83x) .

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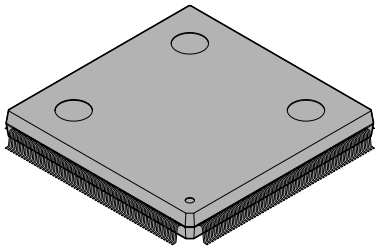
■ PACKAGE

256-pin plastic QFP



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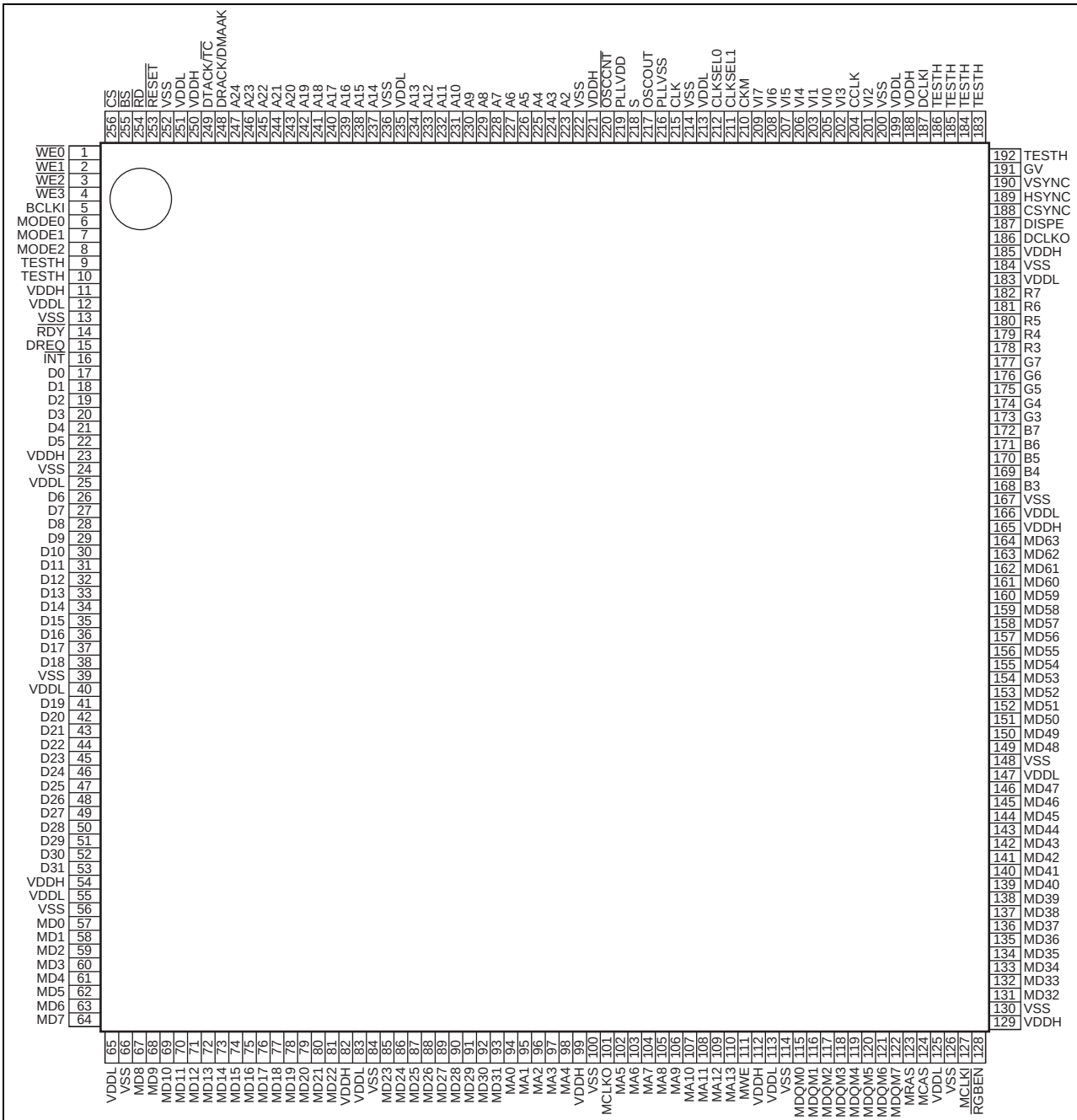
- Drawing features :
  - Drawing at a peak rate of 800 Mpixel/s (at an internal operating frequency of 100 MHz)
  - 2D drawing functions : Point, line, triangle, polygon, BLT and pattern drawing
  - 3D drawing functions : Point, line, triangle drawing and hidden surface removal by Z-buffering
  - Special effects : Anti-aliasing, bold/dashed-line processing, alpha blending, Gouraud shading, texture mapping (bilinear filtering, perspective correct) , and tiling
- Display features :
  - Maximum display resolution supported : 1024 $\times$ 768 pixels
  - Color display either with a color palette of 8 Bit/Pixel or directly using 5-bit RGB colors of 16 Bit/Pixel
  - Overlaying four layers of screen, of which two lower layers can be divided into the left and right parts
  - Supporting two 64 Pixel $\times$ 64 Pixel hardware cursors
  - Output of analog RGB and digital RGB signals
  - Capable of superimposing using an external synchronization mode
- Power-supply voltage : Two power supplies at 2.5 $\pm$ 0.2 V, for internal circuits and 3.3 $\pm$ 0.2 V for I/O parts
- Package : PlasticQFP with 256 pins (with a lead pitch of 0.4 mm)
- Process technology : CMOS 0.25 μm

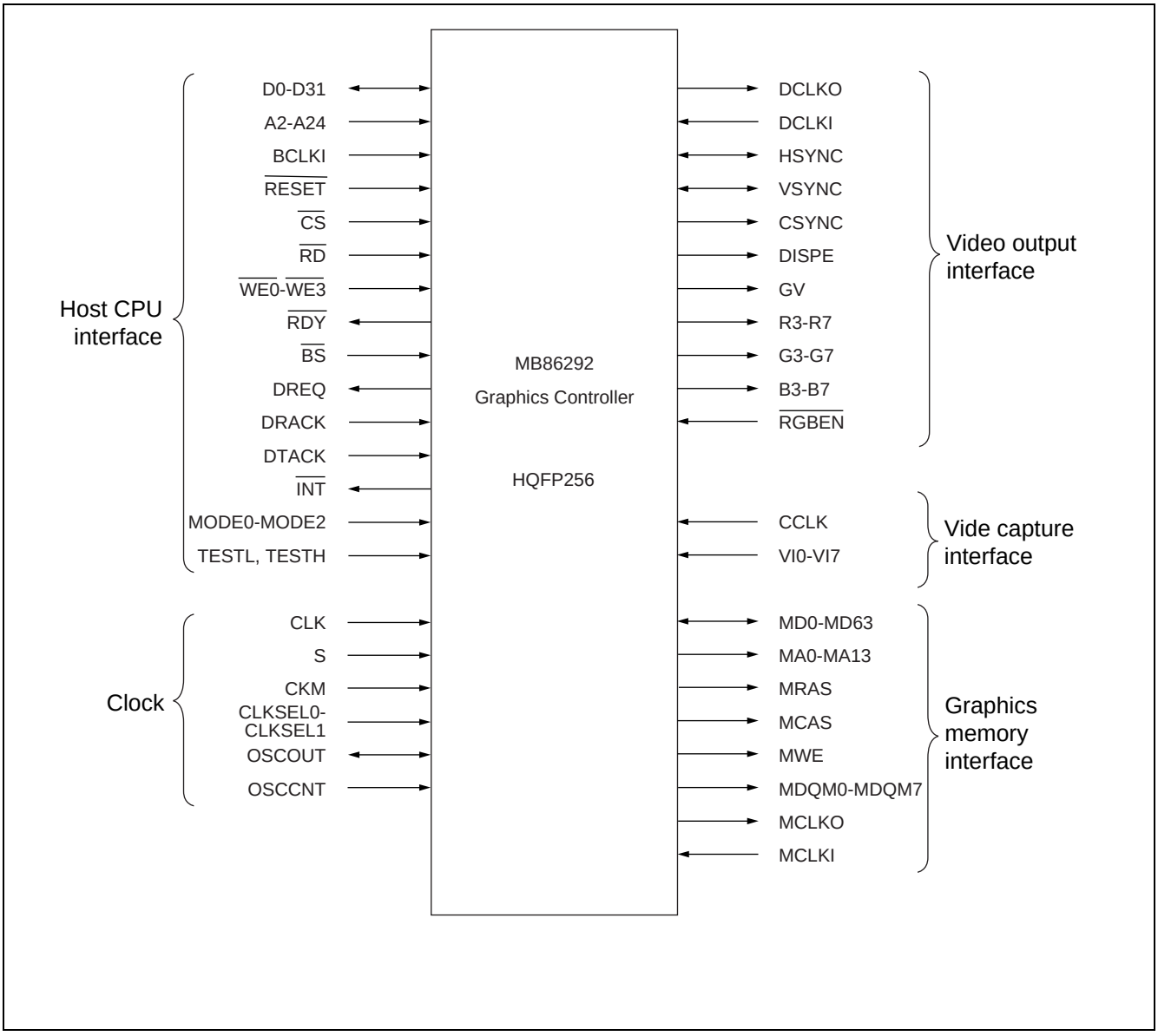
■ PIN ASSIGNMENT



VSS/PLLVSS	: Ground
VDDH	: 3.3 V power supply
VDDL/PLLVDD	: 2.5 V power supply
PLLVDD	: PLL power supply
OPEN	: Do not connect anything.
TESTH	: Input the high level.

Notes :
- The PLLVDD should be separated on the board.
- Insert a bypass capacitor with a superior high-frequency characteristic between the power supply and ground.
  Place the capacitor as near the pins as possible.

■ PIN DESCRIPTION



• Host Interface Pins

Pin Name	Input/output	Function
MODE0-MODE2	Input	Host CPU mode/Ready mode select
$\overline{\text{RESET}}$	Input	Hardware reset
D0-D31	Input/output	Host CPU bus data
A2-A24	Input	Host CPU bus address (Connect A24 to $\overline{\text{MWR}}$ in V832 mode.)
BCLKI	Input	Host CPU bus clock
$\overline{\text{BS}}$	Input	Bus cycle start signal
$\overline{\text{CS}}$	Input	Chip select signal
$\overline{\text{RD}}$	Input	Read strobe signal
$\overline{\text{WE0}}$	Input	D0-D7 write strobe signal
$\overline{\text{WE1}}$	Input	D8-D15 write strobe signal
$\overline{\text{WE2}}$	Input	D16-D23 write strobe signal
$\overline{\text{WE3}}$	Input	D24-D31 write strobe signal
$\overline{\text{RDY}}$	Output Tristate	Wait request signal (“0” for wait state with SH3; “1” for wait state with SH4, V832, or SPARClite)
DREQ	Output	DMA request signal (active low with both SH and V832)
DRACK/DMAAK	Input	DMA request acknowledge signal (Connect this to DMAAK in V832 mode. Active high with both SH and V832.)
DTACK/$\overline{\text{TC}}$	Input	DMA transfer strobe signal (Connect this to $\overline{\text{TC}}$ in V832 mode. SH = active high, V832 = active low)
$\overline{\text{INT}}$	Output	Host CPU interrupt signal (SH = active low, V832 = active high)
TESTH	Input	Test signal

Note : The host interface can connect the MB86292 to the SH4 (SH7750) or SH3 (SH7709) from Hitachi Ltd. the V832 from NEC, or to the SPARClite (MB86833) from Fujitsu without any external circuit in between. (Using the SRAM interface allows the MB86292 to use another CPU.) The host CPU is set by the MODE0 and MODE1 pins as shown below.

MODE1 pin	MODE0 pin	CPU Type
L	L	SH3
L	H	SH4
H	L	V832
H	H	SPARClite

Note : The MODE2 pin can be used to set the Ready signal level to be used upon completion of the bus cycle. To use the MODE2 signal at "H" level, set the software setting to two cycles.

MODE2 pin	Ready signal mode
L	Set $\overline{\text{RDY}}$ signal to “Not Ready” level upon completion of bus cycle.
H	Set $\overline{\text{RDY}}$ signal to “Ready” level upon completion of bus cycle.

Notes : • The host interface transfers data signals at a fixed width of 32 bits.
- There are 23 lines for address signals handled in double words (32 bits) and 32 Mbytes of address space.
- The external bus can be used at an operating frequency of 100 MHz maximum.
- The $\overline{RDY}$ signal at the low level sets the ready state in the SH4 or V832 mode; the signal at the low level sets the wait state in the SH3 mode. Note that the $\overline{RDY}$ signal is a tristate output signal synchronized to the rise of BCLKI.
- The host interface supports DMA transfer using an external DMA controller.
- The host interface generates a host processor interrupt signal.
- The $\overline{RESET}$ pin requires low level input of at least 300 µs after setting "S" (PLL reset signal) to high level.
- Fix the TEST signal at high level.
- In the V832 mode, connect the following pins as specified :

ORCHID Pin Name	V832 Signal Name
A24	$\overline{MWR}$
DTACK	$\overline{TC}$
DRACK	DMAAK

• Video Output Interface Pins

Pin Name	Input/output	Function
DCLKO	Output	Display dot clock signal output
DCLKI	Input	Dot clock signal input
HSYNC	Input/output	Horizontal sync signal output Horizontal sync signal input in external synchronization mode
VSYNC	Input/output	Vertical sync signal output Vertical sync signal input in external synchronization mode
CSYNC	Output	Composite sync signal output
DISPE	Output	Display effective period signal
GV	Output	Graphics/video select signal
R3-R7	Output	Digital video (R) signal output
G3-G7	Output	Digital video (G) signal output
B3-B7	Output	Digital video (B) signal output
$\overline{RGBEN}$	Input	RGB2-0 output/memory bus (MD63-55) select signal

Notes : • The video output interface outputs RGB pieces of five-bit display data by default. It can output RGB pieces of eight-bit display data depending on conditions. R0-2, G0-2, and B0-2 can be output to MD61-MD63, MD58-MD60, and MD58-MD60, respectively, by fixing $\overline{RGBEN}$ to 0. When eight-bit RGB output is selected, only the 32-bit memory bus width mode can be used.
- Using an additional external circuit, the video output interface can generate composite video signals.
- The video output interface can provide display synchronized with external video. The mode for synchronization with the DCLKI signal can be selected as well as the mode for synchronization with a set dot clock as for normal display.
- The HSYNC and VSYNC signals must be pulled up outside the LSI as they enter the input state upon reset.
- The GV signal serves to switch between graphics and video for chroma keying. The pin outputs a low level signal to select video.

• Video Capture Interface Pins

Pin Name	Input/output	Function
CCLK	Input	Digital video input clock signal input
VI0-VI7	Input	Digital video data input

Note : The video capture interface inputs digital video signals in the ITU-RBT-656 format.

• Graphics Memory Interface Pins

Pin Name	Input/output	Function
MD0-MD54	Input/output	Graphics memory bus data
MD55-MD63	Input/output	Graphics memory bus data or RGB0-RGB2 output
MA0-MA13	Output	Graphics memory bus data
MRAS	Output	Row address strobe
MCAS	Output	Column address strobe
MWE	Output	Write enable
MDQM0-MDQM7	Output	Data mask
MCLKO	Output	Graphics memory clock output
MCLKI	Input	Graphics memory clock input

Notes : • The graphics memory interface connects the MB86292 to the external memory used for graphical image data. The interface can directly accept 128-Mbit SDRAM or 64-Mbit SDRAM (with a 16-bit or 32-bit data bus) without any external circuit.
• Memory bus data can be selected between 64 bits and 32 bits. To use 32-bit data, leave the MD32-MD63 and MDQM4-7 pins open in the eight-bit RGB output mode ($\overline{\text{RGBEN}}$ pin = 0) or the MD32-MD54 and MDQM4-7 pins open in the eight-bit RGB output mode ($\overline{\text{RGBEN}}$ pin = 0).
• Connect the MCLKI pin to the MCLKO pin.
• When $\overline{\text{RGBEN}}$ is fixed to 1, MD55-MD63 can be used as graphics memory bus data. When $\overline{\text{RGBEN}}$ is fixed to 0, RGB0-2 is output.

• Clock Input Pins

Pin Name	Input/output	Function
CLK	Input	Clock input signal
S	Input	PLL reset signal
CKM	Input	Clock mode signal
CLKSEL [1 : 0]	Input	Clock rate select signal
OSCOUT*1	Input/output	For connection of crystal oscillator (Reserved)
OSCCNT*2	Input	Crystal oscillator select pin (Reserved)

*1 : Do not connect anything.

*2 : Input the "H" level.

Notes : • The clock input block inputs the clock signal that serves as the basis for the reference clock for the internal operating clock and display dot clock. Usually input 4 Fsc (= 14.31818 MHz for NTSC). The internal PLL generates the internal operating clock signal of 100 MHz and the display reference clock signal of 200 MHz.
• The internal operating clock signal to be used can be selected between the clock signal (100 MHz) generated by the internal PLL and the bus clock BCLKI input to the host CPU interface. Select the BCLKI input to use the host CPU bus at 100 MHz.

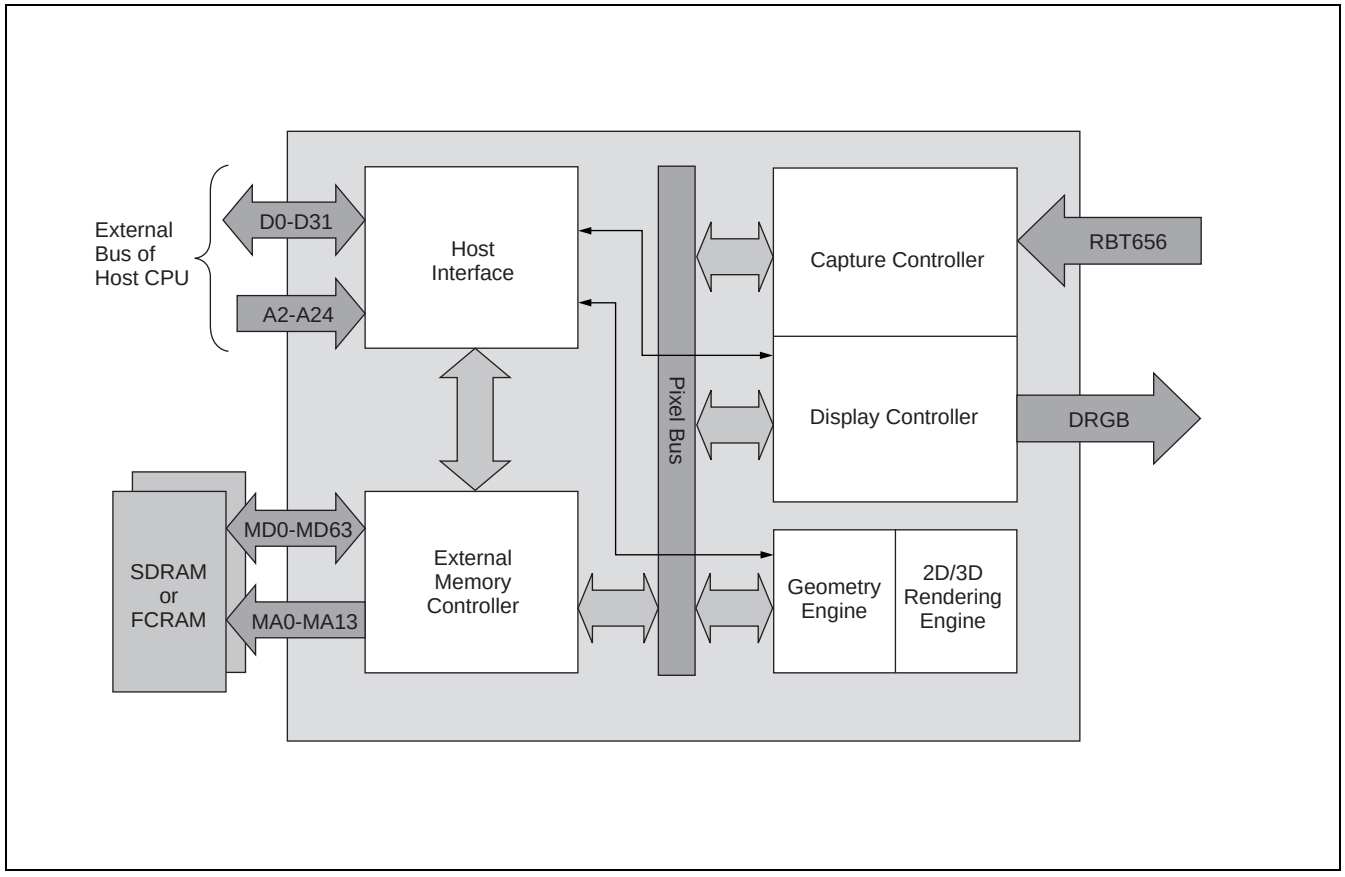
CKM	Clock Mode
L	Select internal PLL output.
H	Select host CPU bus clock (BCLKI).

- Use the CLKSEL pin to select the input clock frequency for using the internal PLL with CKM = L.

CLKSEL1	CLKSEL0	Input Clock Frequency	Multiplier	Display reference clock
L	L	Input 13.5 MHz.	× 15	202.5 MHz
L	H	Input 14.32 MHz.	× 14	200.48 MHz
H	L	Input 17.73 MHz.	× 11	195.03 MHz
H	H	Reserved	—	—

Note : Immediately after turning the power supply on, input a pulse whose low level period is 500 ns or more to the S pin before setting it to high level. After the S signal goes high, input the $\overline{\text{RESET}}$ signal at low level for 300 μs or more.

■ BLOCK DIAGRAM



■ FUNCTION BLOCKS

• Host Interface

This block allows the MB86292 to be connected to the SH3 or SH4 microprocessor from Hitachi Ltd., the V83x microprocessor from NEC, or to the SPARCLite from Fujitsu without any external circuit in between. The block provides an interface to transfer display list and texture pattern data directly from main memory to this device's graphics memory or internal register using the external DMA controller.

• External Memory Controller

This block connects external SDRAM or FCRAM. The data bus can be selected between 64 bits and 32 bits and the maximum operating frequency is 100 MHz.

• Display Controller

This block contains a three-channel, eight-bit D/A converter to output analog RGB signals. The block has eight-bit RGB digital video outputs, allowing an external digital video encoder to be connected. The block supports resolutions of up to XGA (1024×768 pixels), enabling flexible setting.

• Set-up Engine

The on-chip geometry engine executes mathematical operations required for graphics processing precisely using the fronting-point format. The geometry engine executes the required geometry processes selected depending on the drawing mode and primitive type settings up to the final drawing process.

• 2D/3D Rendering Engine

This block draws images in two or three dimensions.

2D drawing
The block provides the anti-aliasing and alpha blending functions to display high-quality images even on a low-resolution LCD.

3D drawing
The block provides true 3D drawing functions such as perspective texture mapping and Gouraud shading.

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Unit
		Min	Max	
Power supply voltage	V_{DDL}*	– 0.5	3.0	V
	V_{DDH}	– 0.5	4.0	
Input voltage	V_I	– 0.5	V_{DDH} + 0.5 (< 4.0)	V
Output current	I_O	– 13	+ 13	mA
Power pin current	I_{POW}	60	60	mA
Ambient storage temperature	Tstg	– 55	+ 125	°C

* : The PLL power supply is included.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Power supply voltage	V_{DDL}*	2.3	2.5	2.7	V
	V_{DDH}	3.0	3.3	3.6	
Input voltage (“H” level)	V_{IH}	2.0	—	V_{DDH} + 0.3	V
Input voltage (“L” level)	V_{IL}	– 0.3	—	+ 0.8	V
Ambient operating temperature	T_A	– 40	—	+ 85	°C

* : The PLL power supply is included.

Notes :
- The VDDL and VDDH power supplies can be turned on or off in either order. Note, however, that the VDDH voltage must not be applied alone continuously for several seconds.
- Do not input the HSYNC, VSYNC, or EO signal with the power-supply voltage not applied. (See “Input voltage” in “■ ABSOLUTE MAXIMUM RATINGS”.)
- After turning the power on, input a pulse remaining at low level for at least 500 ns to the S pin. Then, set the S pin to high level and input the $\overline{\text{RESET}}$ signal held at low level for at least 300 µs.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device’s electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

■ ELECTRICAL CHARACTERISTICS

1. DC Characteristics

(VDDL = 2.5 ± 0.2 V, VDDH = 3.3 ± 0.3, VSS = 0.0 V, Ta = 0 °C to + 70 °C)

Paramater	Symbol	Value			Unit
		Min	Typ	Max	
Output voltage (“H” level) *1	V_{OH}	V_{DDH} – 0.2	—	V_{DDH}	V
Output voltage (“L” level) *2	V_{OL}	0.0	—	0.2	V
Output current (“H” level)	$I_{OH}1$*3	– 2.0	—	—	mA
	$I_{OH}2$*4	– 4.0			
	$I_{OH}3$*5	– 8.0			
Output current (“L” level)	$I_{OL}1$*3	2.0	—	—	mA
	$I_{OL}2$*4	4.0			
	$I_{OL}3$*5	8.0			
Input leakage current	I_L	—	—	± 5	µA
Pin capacitance	C	—	—	16	pF

*1 : Value when –100 µA current flows into output pins.

*2 : Value when 100 µA current flows into output pins.

*3 : Output characteristics of the MD0-63 and MDQM0-7 signal.

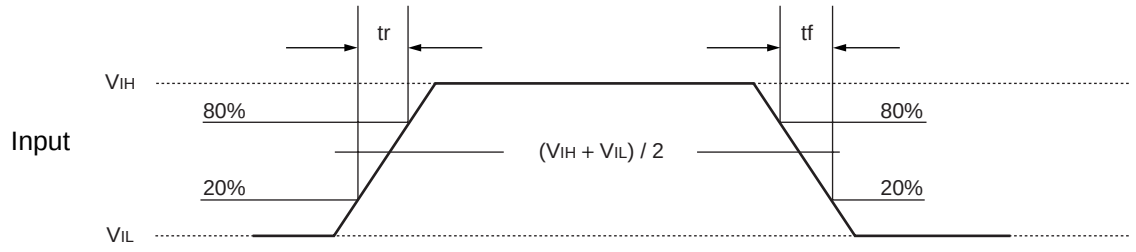
*4 : Output characteristics of the signals other than those in *3 and *5

*5 : MCLKO signal output characteristics

2. AC Characteristics

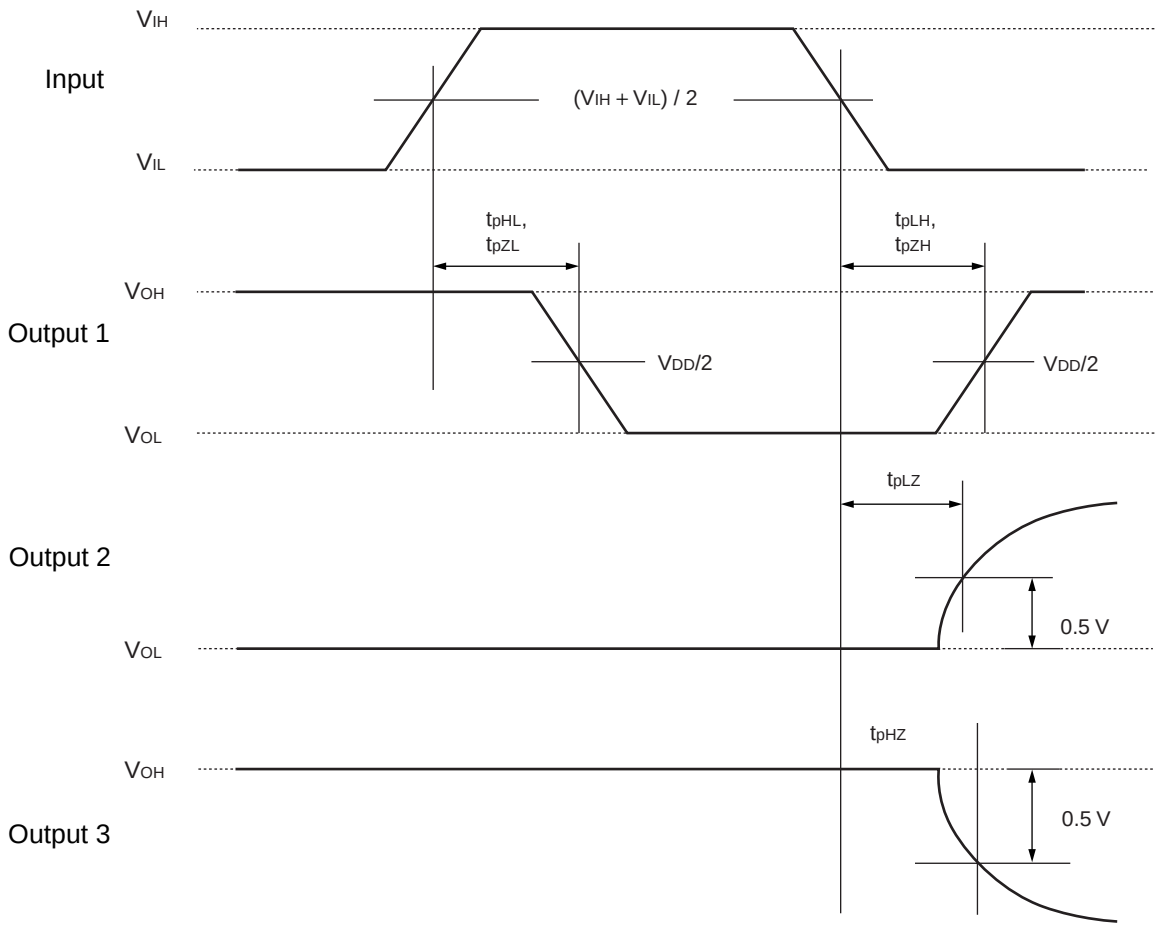
(V_{IH} = 2.0 V, V_{IL} = 0.8 V)

• Input measurement conditions



• tr, tf ≤ 5 ns
• Input measurement standard : (V_{IH} + V_{IL}) / 2

• Output measurement conditions



• Output measurement standard : tpLZ : V_{OL} + 0.5 V
tpHZ : V_{OH} – 0.5 V
Else : V_{DD}/2

(1) Host Interface

• Clock

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
BCLKI frequency	f_{BCLKI}	—	—	—	100	MHz
BCLKI H period	t_{HBCLKI}	—	1	—	—	ns
BCLKI L period	t_{LBCLKI}	—	1	—	—	ns

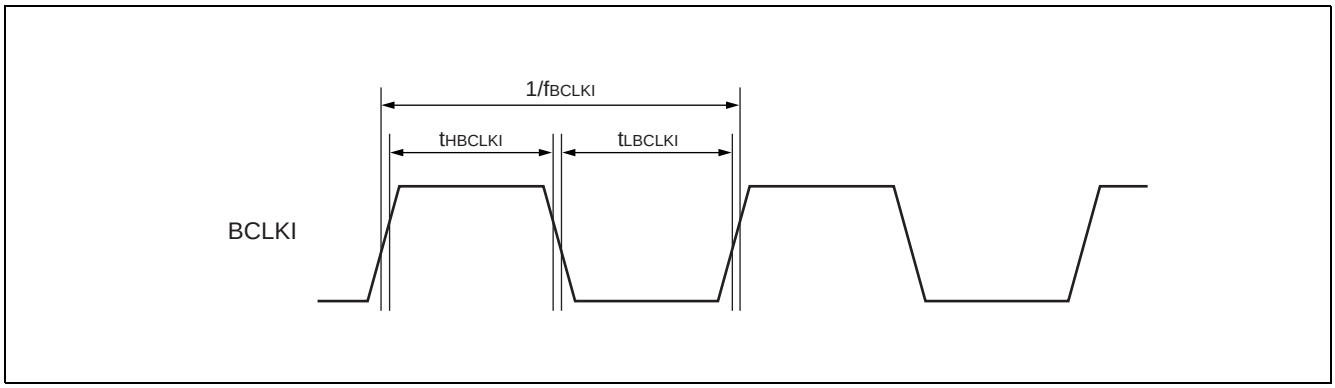
• Host interface signals

(Operating condition : External load of 20 pF)

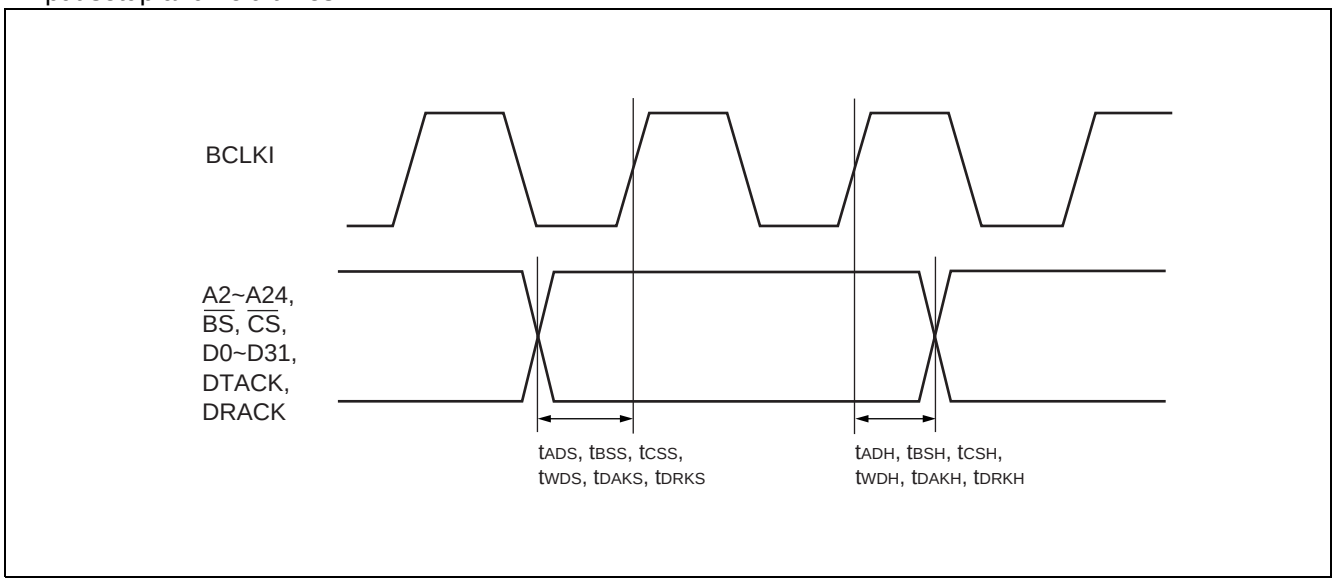
Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Address setup time	t_{ADS}	—	3.0	—	—	ns
Address hold time	t_{ADH}	—	1.0	—	—	ns
$\overline{BS}$ setup time	t_{BSS}	—	3.5	—	—	ns
$\overline{BS}$ hold time	t_{BSH}	—	0.0	—	—	ns
$\overline{CS}$ setup time	t_{CSS}	—	3.5	—	—	ns
$\overline{CS}$ hold time	t_{CSH}	—	0.0	—	—	ns
$\overline{RD}$ setup time	t_{RDS}	—	3.0	—	—	ns
$\overline{RD}$ hold time	t_{RDH}	—	0.0	—	—	ns
$\overline{WE}$ setup time	t_{WES}	—	5.5	—	—	ns
$\overline{WE}$ hold time	t_{WEH}	—	0.0	—	—	ns
Write data setup time	t_{WDS}	—	3.5	—	—	ns
Write data hold time	t_{WDH}	—	0.0	—	—	ns
DTACK setup time	t_{DAKS}	—	3.5	—	—	ns
DTACK hold time	t_{DAKH}	—	0.0	—	—	ns
DRACK setup time	t_{DRKS}	—	4.0	—	—	ns
DRACK hold time	t_{DRKH}	—	0.0	—	—	ns
Read data delay time (to $\overline{RD}$)	t_{RDDZ}	—	2.5	—	8.5	ns
Read data delay time	t_{RDD}	—	4.0	—	10.5	ns
$\overline{RDY}$ delay time (to $\overline{CS}$)	t_{RDYDZ}	—	2.0	—	6.0	ns
$\overline{RDY}$ delay time	t_{RDYD}	—	2.5	—	6.5	ns
$\overline{INT}$ delay time	t_{INTD}	—	2.5	—	7.0	ns
DREQ delay time	t_{DRQD}	—	2.5	—	6.5	ns
MODE hold time	t_{MODH}	*	—	—	20.0	ns

* : Hold time for reset cancellation

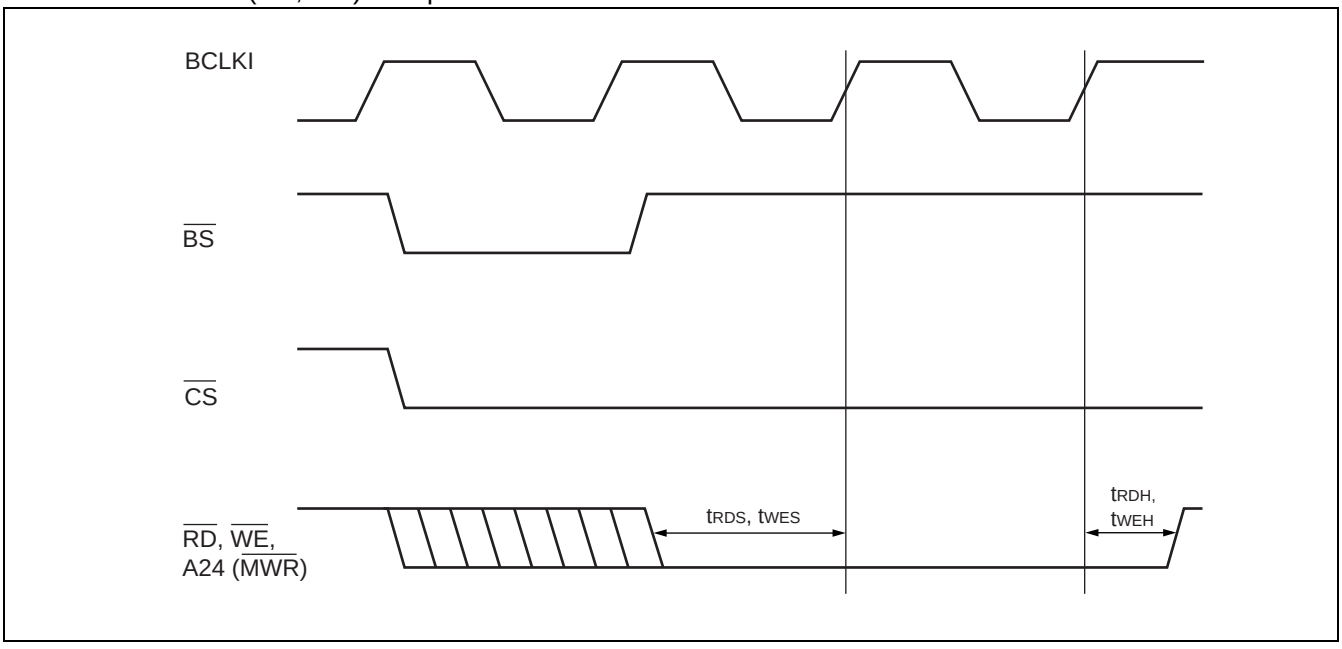
• Clock



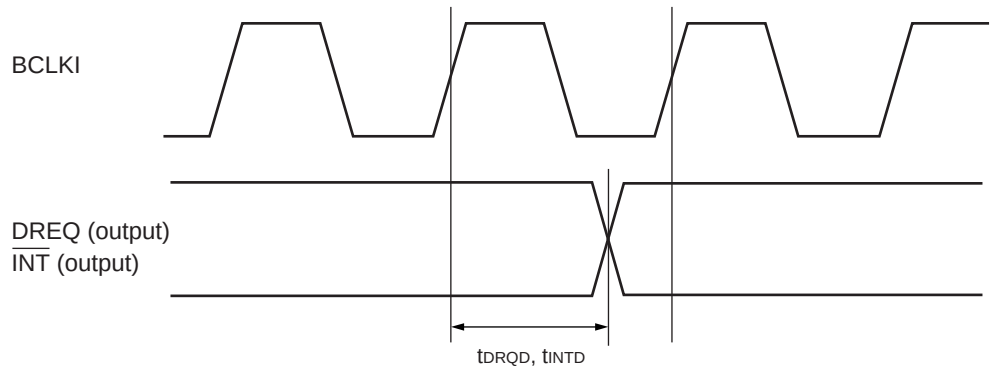
• Input setup and hold times



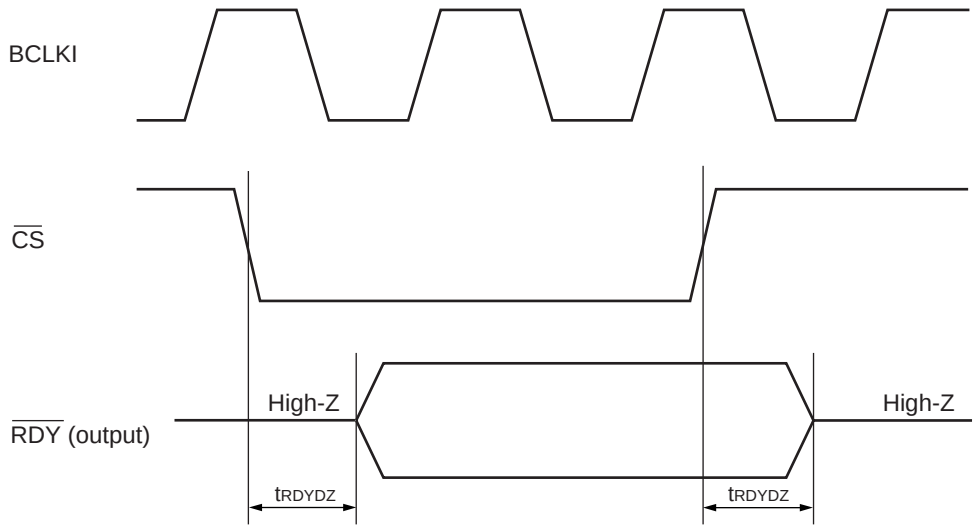
• Read/write enable ($\overline{RD}$, $\overline{WE}$) setup and hold times



• DREQ/$\overline{\text{INT}}$ output delay time

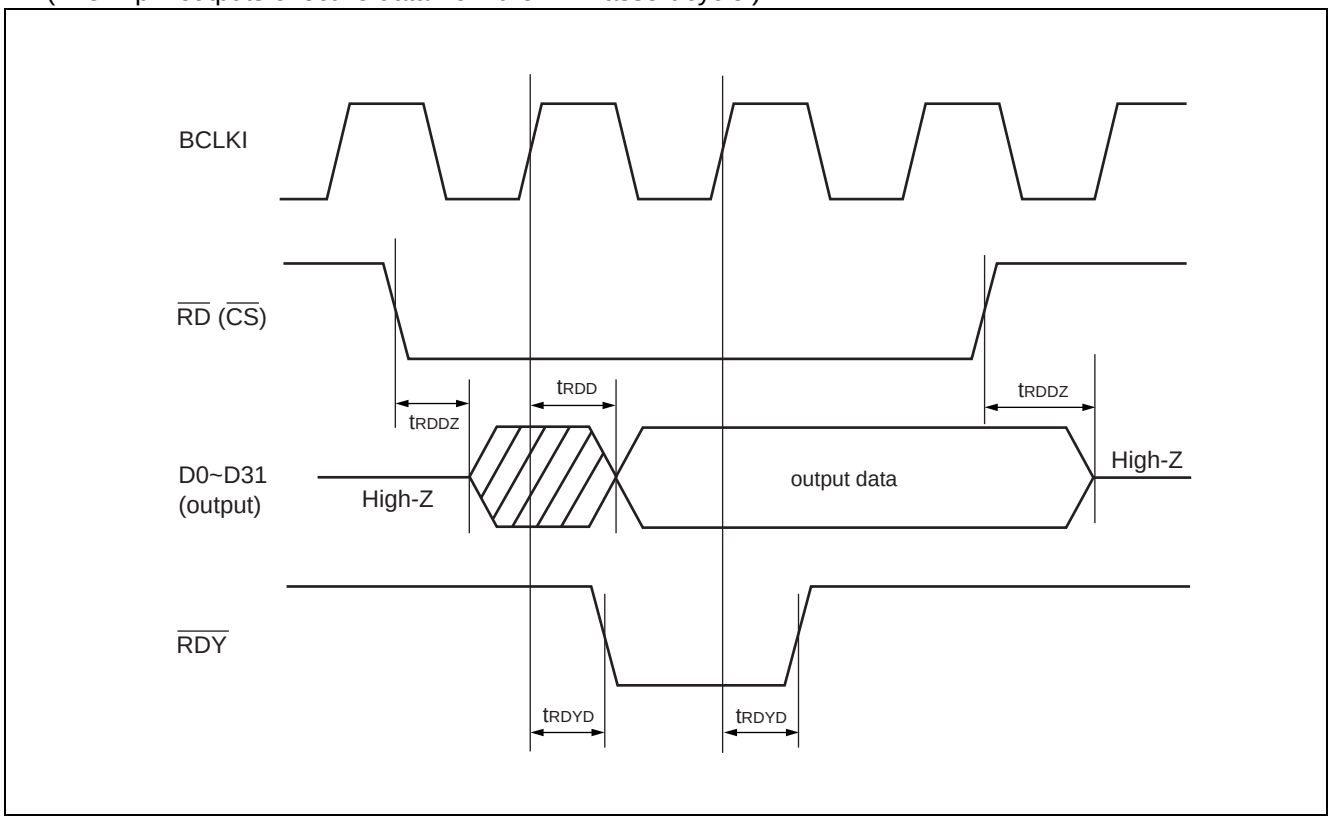


• $\overline{\text{RDY}}$ delay value (with respect to $\overline{\text{CS}}$)

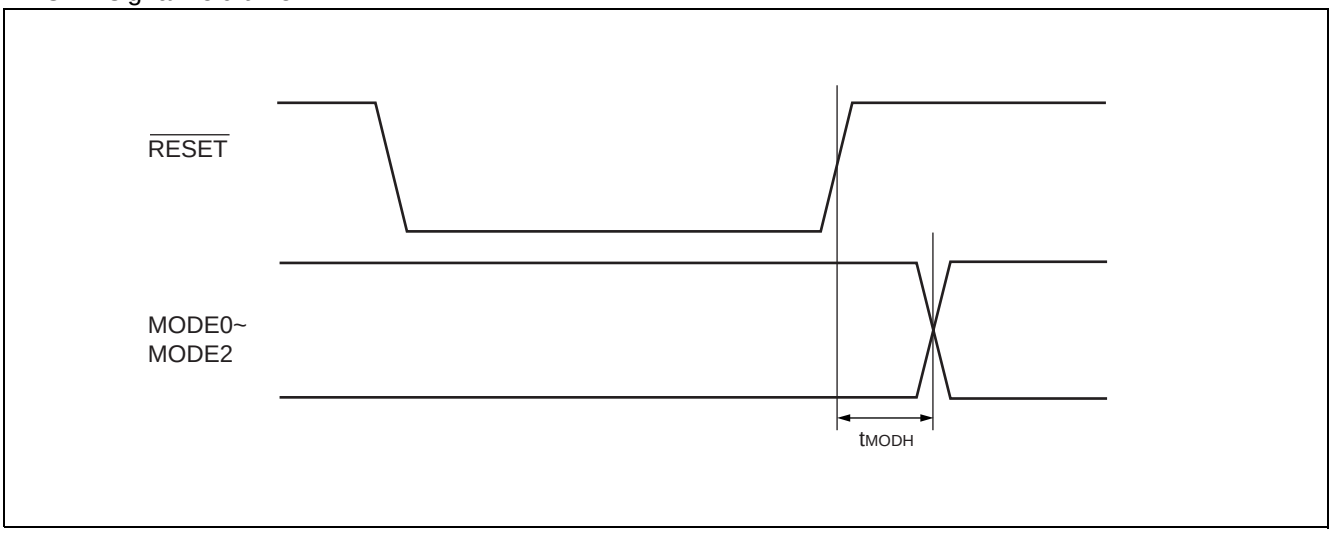


• $\overline{RDY}$, D output delay values

(The D pin outputs effective data from the $\overline{RDY}$ assert cycle.)



• MODE signal hold time



(2) Video Interface

• Clock

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
CLK frequency	f_{CLK}	—	—	14.318	—	MHz
CLK H period	t_{HCLK}	—	25	—	—	ns
CLK L period	t_{LCLK}	—	25	—	—	ns
DCLKI frequency	f_{DCLKI}	—	—	—	67	MHz
DCLKI H period	t_{HDCLKI}	—	5	—	—	ns
DCLKI L period	t_{LDCLKI}	—	5	—	—	ns
DCLKO frequency	f_{DCLKO}	—	—	—	67	MHz

• Input signals

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
HSYNC input pulse width	$t_{WHSYNC0}$	*1	3	—	—	clock
	$t_{WHSYNC1}$	*2	3	—	—	clock
HSYNC input setup time	t_{SHSYNC}	*2	10	—	—	ns
HSYNC input hold time	t_{HHSYNC}	*2	10	—	—	ns
VSYNC input pulse width	$t_{WHSYNC1}$	—	1	—	—	HSYNC cycle

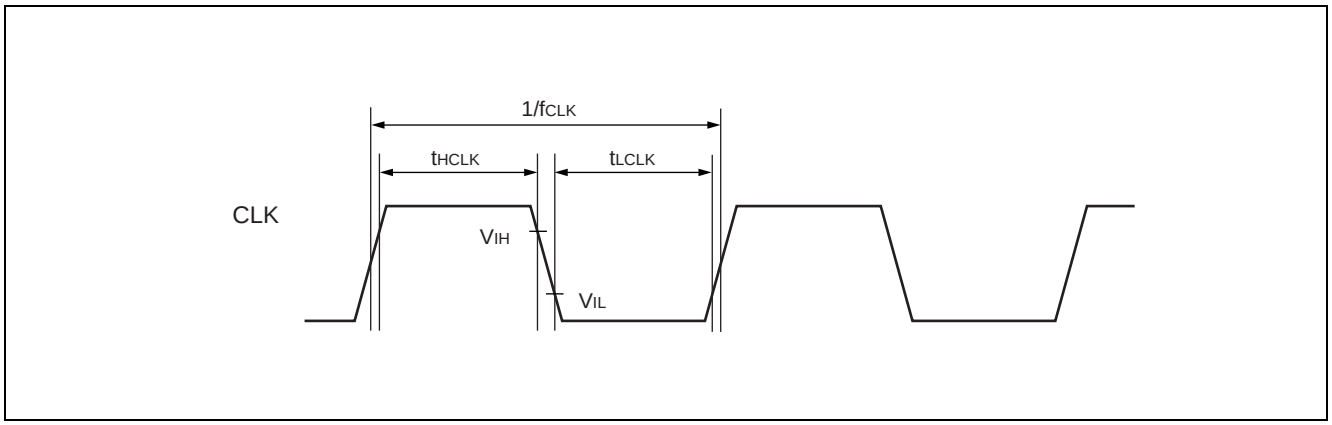
*1 : Applied only in PLL synchronization mode (CKS = 0) . The reference clock is the internal PLL's output with Cycle = 1/ (14 f_{CLK}) .

*2 : Applied only in DCLKI synchronization mode (CKS = 1) . The reference clock is DCLKI.

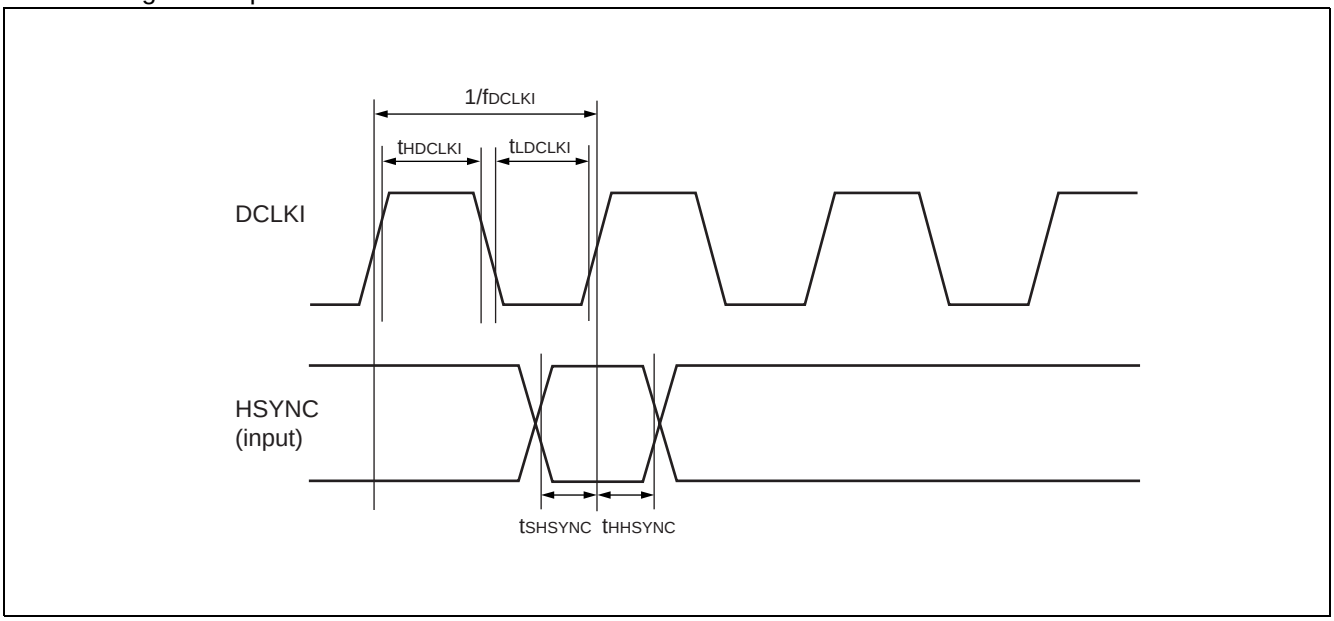
• Output signals

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
RGB output delay time	t_{RGB}	—	2	—	10	ns
DISPE output delay time	t_{DEO}	—	2	—	10	ns
HSYNC output delay time	t_{DHSYNC}	—	2	—	10	ns
VSYNC output delay time	t_{DVSYNC}	—	2	—	10	ns
CSYNC output delay time	t_{DCSYNC}	—	2	—	10	ns
GV output delay time	t_{DGV}	—	2	—	10	ns

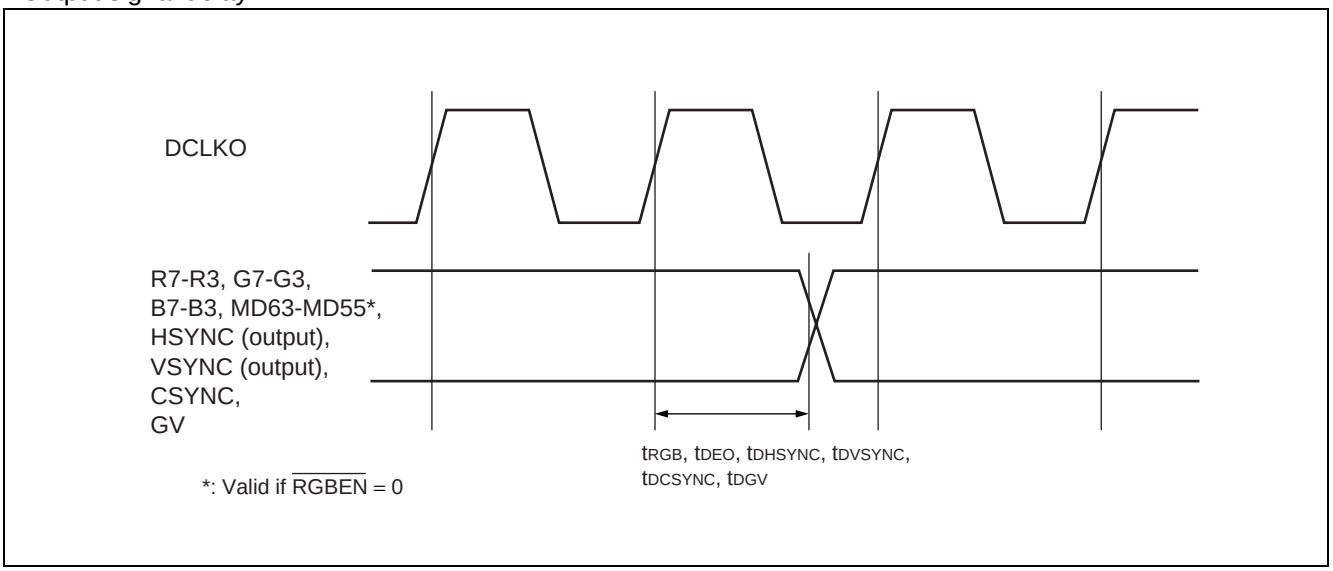
• Clock



• HSYNC signal setup and hold



• Output signal delay



(3) Graphics Memory Interface

• Clock

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
MCLKO frequency	f_{MCLKO}	—	—	—	*	MHz
MCLKO H period	t_{HMCLKO}	—	1.0	—	—	ns
MCLKO L period	t_{LMCLKO}	—	1.0	—	—	ns
MCLKI frequency	f_{MCLKI}	—	—	—	*	MHz
MCLKI H period	t_{HMCLKI}	—	1.0	—	—	ns
MCLKI L period	t_{LMCLKI}	—	1.0	—	—	ns
MCLKI delay to MCLKO	t_{OID}	—	0.0	—	3.5	ns

* : In BUS asynchronous mode, the frequency is half the internal PLL oscillation frequency. In Bus synchronous mode, the frequency is the same as BCLKI.

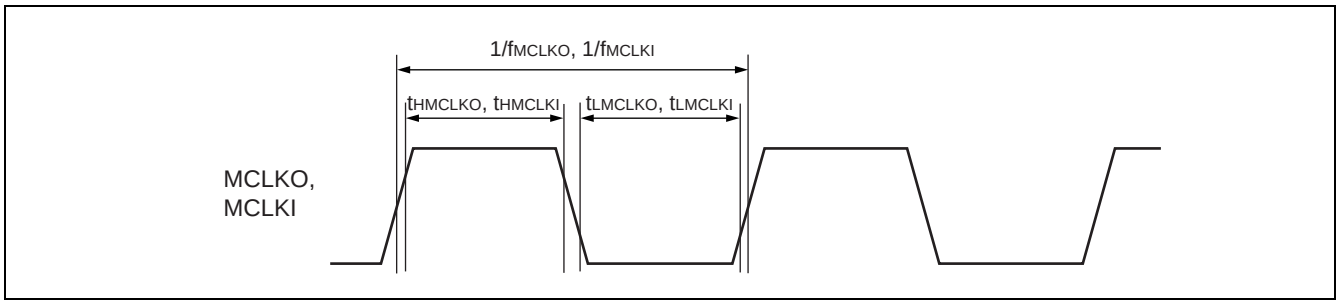
• Input/output signals

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
MA, MRAS, MCAS, MWE setup time	t_{MADS}	*1	3.2	—	—	ns
MA, MRAS, MCAS, MWE hold time	t_{MADH}	*1	1.3	—	—	ns
MDQM data setup time	t_{MDQMDS}	*1	3.2	—	—	ns
MDQM data hold time	t_{MDQMDH}	*1	1.3	—	—	ns
MD output data setup time	t_{MDODS}	*1	3.2	—	—	ns
MD output data hold time	t_{MDODH}	*1	1.3	—	—	ns
MD input data setup time	t_{MDIDS}	*2	3.0	—	—	ns
MD input data hold time	t_{MDIDH}	*2	1.0	—	—	ns

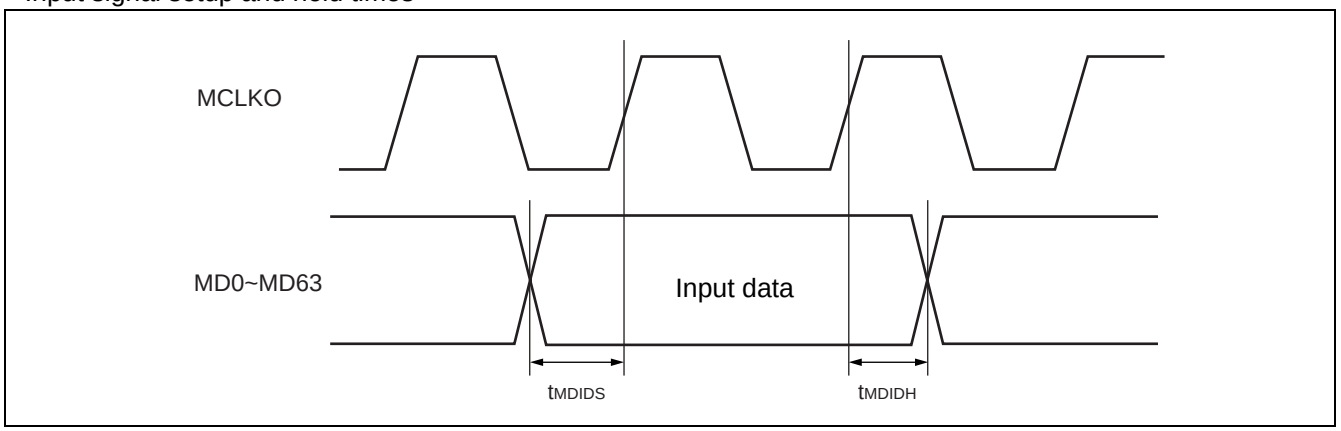
*1 : Setup/hold time with respect to MCLKO

*2 : Setup/hold time with respect to MCLKI

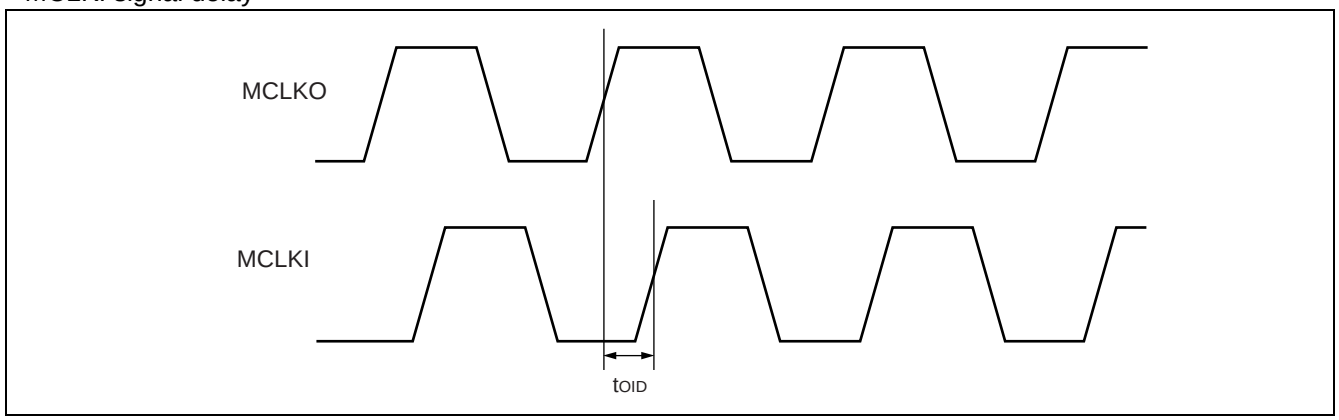
• Clock



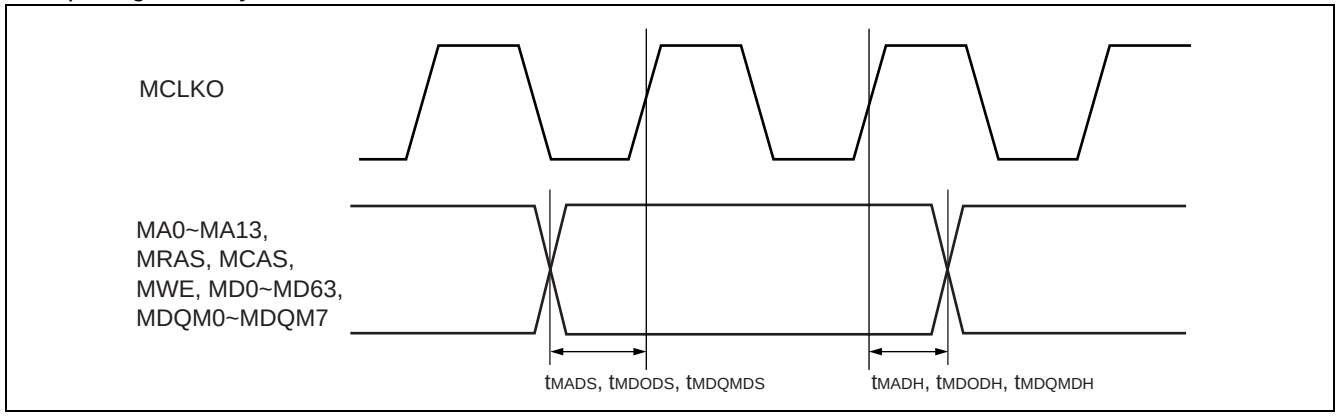
• Input signal setup and hold times



• MCLKI signal delay



• Output signal delay



(4) PLL Standards

Parameter	Value			Remarks
	Min	Typ	Max	
Input frequency	—	14.31818 MHz	—	
Output frequency	—	—	200.45452 MHz	Multiplied by 14
Duty ratio	101.3 %	—	93.1 %	PLL output clock H/L pulse width ratio
Jitter	180 ps	—	− 150 ps	Cycle difference between two consecutive cycles

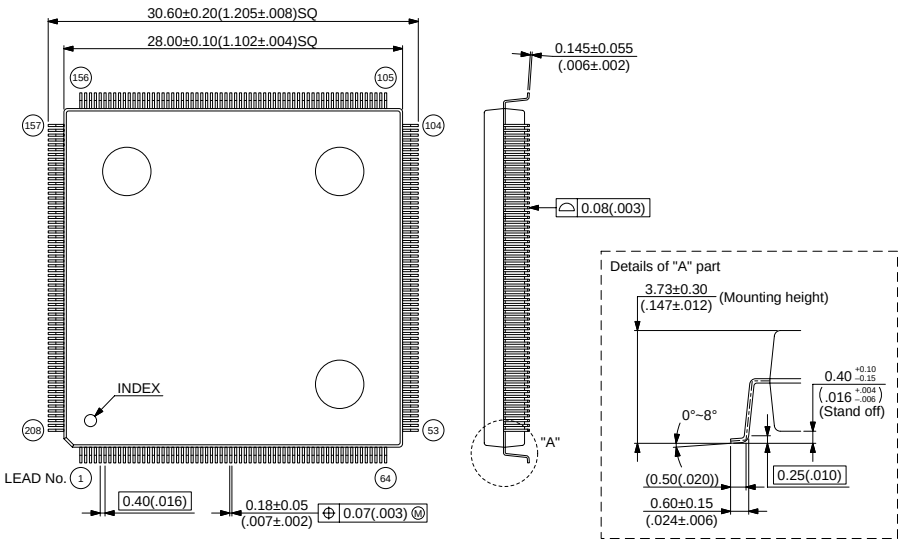
■ ORDERING INFORMATION

Part Number	Package	Remarks
MB86292PFFS-G-BND	256-pin plastic QFP (FPT-256P-M09)	

■ PACKAGE DIMENSION

256-pin plastic QFP
(FPT-256P-M09)

*Pins width and pins thickness include plating thickness.



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